INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN: 2278 – 0211 (Online)

SRRC Filter Implementation As Per DVB-S2 Standard

Sreevidya N
Department Of Telecommunication Engineering
DayanandaSagar College of Engineering, Bangalore, India

H C Sateeshkumar
Department Of Telecommunication Engineering
DayanandaSagar College of Engineering, Bangalore, India

Abstract:

The new bandwidth-efficient DVB-S2 (EN302307) standard, the successor of DVB-S and DVB-DSNG is designed to address the challenges of cost-effectively transmitting high-quality video and advanced services via satellite. This paper focuses on the design and implementation of SRRC filter as part of the Baseband shaping and Quadrature modulation module of DVB-S2 standard for the three rolloff factors 0.20, 0.25, and 0.35. It is a pulse shaping filter which aims at minimising ISI.Direct form symmetric structure of FIR filter is used to design SRRC filter of order 96using MATLAB and FPGA implemented using ALTERA Quartus II.This paper will deliver the results of SRRC filter for different roll-offs along with the performance gain comparisons of DVB-S and DVB-S2 roll-offs.

Key words: *Digital Video Broadcasting – Satellite (DVB-S), Digital Video Broadcasting-Second Generation (DVB-S2), Square Root Raised Cosine (SRRC), Inter symbol Interference (ISI)*

1.Introduction

- DVB-S2 is the second-generation specification for satellite broad-band applications,developed by the Digital Video Broad-casting(DVB) Project in 2003.The system is structured as a toolkit to allow the implementation of the following satellite applications: TV and sound broadcasting, interactivity and professional services, such as TV contribution links and digital satellite news gathering.it has been specified around three concepts: best transmission performance approaching the Shannon limit, total flexibility, and reasonable receiver complexity.

  A number of factors and capabilities of DVB-S2 contribute to exceptional efficiency gains, one such capability on which this paper focuses is a choice of 0.20%, 0.25% and 0.35% spectrum shaping factors.
- Motivation: Digital data transmission through a band-limited channel, leads to Inter-symbol Interference that can pose a serious problem to the quality of reception if left uncontrolled.In DVB-S standard the filter is designed to work for just one rolloff value of 0.35 which poses ISI problem. In this paper we propose a technique for designing SRRC filter based on shaping the baseband response of the system. In time domainband limited communication systems, the transmitted signal should pass baseband pulse shaping signal at the transmitter to limit the signal bandwidth and satisfy Nyquistcriterion. For the pulse shaping SRRC filter, the rolloff factor directly determines the spectrum efficiency.
- Contribution: The SRRC filter is used in wireless transmission to pulse-shape the chip stream output before it is modulated to the RF.It is a Baseband filter designed as part of the Baseband shaping and quadrature modulation module of DVB-S2 standard for the three roll-off factors 0.2, 0.25, 0.35. Selectablerolloff factor supports more efficient utilization of transponder bandwidth by reducing guard band. The spectrum is bandwidth limited in order to avoid interferences with neighbour symbols.

  The smooth characteristics of the raised cosine filter spectrum, makes it possible to design practical filters that approximates the overall desired frequency response. The factor α is called the roll-off factor, it indicates how much bandwidth is being used over ideal bandwidth. The smaller this factor, the more

efficient is the system.The proposed scheme provides flexibility to work with three different rolloff 0.20, 0.25 and 0.35.

- Organization: This rest of the paper is organised as follows. Section II is an overview of the related work, Section III describes the generation of filter coefficients and filter design in MATLAB, Section IV presents the architecture of the filter, Section V describes the FPGA implementation of filter using ALTERA Quartus II, performance analysis of the model is presented in section VI. The last section summarizes this paper.

2.Related Work

ETSI EN 302 307, [1] gives an introduction to the Digital Video Broadcasting: Second generation framing structure, channel coding and modulation systems.It gives brief description of DVB-S2 block diagram and modules as well as its advantages over DVB-S standard.and improvements made in DVB-S2.

Alberto et al., [2] presents the main characteristics of the dvb-s2 systemand has described the main modulation/demodulation algorithms for a modem implementation including receiver synchronization. The framing structure allows for maximum flexibility in a versatile system to work properly on the nonlinear satellite channel.

ETSI EN 300 421, [3] gives an introduction to Digital Video Broadcasting (DVB): Framing structure, channel coding and modulation for 11/12 GHz satellite services. It gives brief introduction about standards and features of DVB-S standard.

Abdolhadi, [4] describes the next generation solution for both SDTV and HDTV distribution system. It is based on the new emerging DVB-S2 standard, which enables much more efficient transmission of digital video in current satellite transponders.

Mohamed et al., [5] discusses an algorithm proposed for modifying values and the number of non-zero coefficients used to represent the FIR digital pulse shaping filter response. With this algorithm, the FIR filter frequency and phase response can be represented with a minimum number of non-zero coefficients. Therefore, reducing the arithmetic complexity needed to get the filter output.

Charan et al., [6] compares and contrasts the performance of a Root Raised Cosine matched filter implemented using hybrid-logarithmic arithmetic with that of standard binary and floating point implementations. It also clarifies that Hybrid-logarithmic

arithmetic is advantageous for FIR digital filters since it removes the necessity for the use of high-speed array multipliers.

Macpherson et al., [7] demonstrates how the modifying of the filter coefficients and taking advantage of non-canonical implementation techniques can yield reduced hardware in FPGA. Using the Root Raised Cosine (RRC) pulse shaping filter required in the 3G uplink reception techniques are compared in terms of DSP system performance and FPGA cost. RRC filter performance is evaluated through simulation of the Adjacent Channel Selectivity (ACS) test. Simulation results were presented and the different hardware structures were evaluated.

Harish et al., [8] explains how a Rectangular Pulse Root Raised Cosine Filter used as the required channel selection filter. The filter was designed to process the output from a modulator suppressing the out of band quantization noise, interfering channels and Operating as a matched filter. Polyphase half-band structures with Distributed Arithmetic based look up table structures was used to minimize the power consumption and increase speed at the cost of area.

Pan et al., [9] proposes low complexity implementation method. Focuses on the implementation of high order square root raised cosine fir filter which is widely used in time domain band limited communication systems as the digital baseband pulse-shaping filter.

Zhang et al., [10] proposes the design of series of square-root-raised-cosine (SRRC) FIR filter with CSD coefficients according to the local search algorithm based upon mini-max error criteria. The simulation results of a baseband system show that two 13-tap SRRC FIR filters with a roll-off factor 0.6 only introduced about 6% peak distortion in the eye pattern. Bit-level pipeline architecture was used to realize the high sampling rate FIR filter.

Jue et al., [11] demonstrates the implementation of visual IP generator for SRRC filter based on Microsoft visual studio 2008.The SRRC IP generated from this work is also compiled and simulated in Altera Quartus II and compared with the Aletra IP code synthesized SRRC filter.

Chia et al., [12] proposes a recursive method for designing the SRRC FIR filters. Using a pair of matched SRRC filters in the transmitter and the receiver in a band limited digital communication system can theoretically achieve zero ISI. In reality, such pair of SRRC filters does not exist. The ISI can be only reduced to some level when both SRRC filters are approximately implemented.

Georgios et al., [13] discusses the application of the adaptive coding and modulation feature of DVB-S2 in the provision of satellite triple play services over an interactive DVB-S2/DVB-RCS network in order to compensate for fluctuations in propagation conditions. A cross-layer resource management system is proposed in order to adapt the system to such fluctuations and improve its overall efficiency.

Bruce et al., [14] demonstrates how the DVB-S2 waveform allows for optimization of the broadcast to support simultaneous transmission of information to specific terminal sets with different aperture sizes, including severely disadvantaged terminals. It also discusses the advantages of the Advanced Coding and Modulation mode for two-way systems and its implementation challenges into the next generation Joint IP Modem Architecture.

3.SRRC Filter Design

ISI is an unavoidable consequence of both wired and wireless communication systems. The ISI arises because of imperfections in the overall frequency response of the system where in the energy of one symbol overlaps with another thus the output of the system is dispersed.

Finite Impulse response (FIR) filter is used to design SRRC filter. FIR filters are one of two primary types of digital filters used in Digital Signal Processing (DSP) applications.The impulse response of this FIR filter is finite and hence practically realizable. Requires no feedback as it is non recursive in nature where the output at any time is a function of input signal at that time and any rounding errors are not compounded by summed iterations hence the same relative error occurs in each step, provides guaranteed stability as all the poles are located at the origin and are with in the unit circle with a perfect linear phase that corresponds to equal delay at all frequencies.

They are simple to implement, suites to multi-rate applications. In practice, all DSP filters must be implemented using finite-precision arithmetic, that is, a limited number of bits and FIR is the best.

Hamming window is used for pulse shaping as part of the design□which is suitable for speech procesing applications as per DVB_S2 standard.□□□

Rolloff factorα, is a measure of the excess bandwidth of the filteri.e. it indicates how much bandwidth is being used over the ideal bandwidth. The smaller this factor, the more efficient is the scheme. The percentage over the minimum required Nyquist bandwidth W is called the excess bandwidth, expressed as

$\alpha = 1\text{-}W/\ Wo$(1)

Where W is the Nyquist bandwidth and Wo is the utilized bandwidth, $W = 1/2T_s$.

The typical rolloffs used for wireless communications range from 0.2 to 0.4. The choice of smaller rolloff leads to smallest bandwidth.

The raised-cosine filter is a filter frequently used for pulse-shaping in digital modulation due to its ability to minimize ISI. The rectangular pulse occupies a large bandwidth so an alternative to rectangular pulse is a modified sinc pulse, which is the raised cosine pulse that reduces the bandwidth and Inter Symbol Interference.

The frequency respone of SRRC filter as defined by DVB_S2 standard is given by Fig 2. In order to determine the coefficients of the filter fdatool is used in MATLAB

$$H(f) = \begin{cases} 1 & \text{for } |f| < f_N(1-\alpha) \\ \left\{\frac{1}{2} + \frac{1}{2}\sin\frac{\pi}{2f_N}\left[\frac{f_N - |f|}{\alpha}\right]\right\}^{1/2} & \text{for } f_N(1-\alpha) \\ 0 & \text{for } |f| > f_N(1+\alpha) \end{cases} \quad (2)$$

Where $f_N = 1/2T_s = R_s/2$ is the Nquist frequency and α is the roll-off factor between 0 and 1.

The filter defined using the above transfer function produces zero-ISI over a low-pass channel. Generally, in Digital Communication Systems, transmit and the receive filters are jointly designed to produce zero-ISI.

MATLAB is used to generate the filter coefficients for filter order 96 using fdatool. The specifications are Response type-Raised cosine, FIR Filter, Hamming Window, Frequencyspecifications F_s-48MHz and F_c -1.7MHz, Rolloff-0.2 or 0.25 or 0.35.Filter coefficients are generated for a selected Rolloff and SRRC filter is designed in MATLAB using these coefficients.

Linear convolution gives the response of the LTI system as a function of the input signal and the unit sample (impulse) response given by Fig 3

$$Y_n = \sum_{k=-\infty}^{\infty} X_{n-k}\ h_k \quad (3)$$

WhereY_n is the output and $X_k$is the input. In each step the output is calculated by shifting the inputs one after the other in sequence.

4.Filter Architecture

The architecture of the filter shown in Fig 3 uses the Direct form symmetric structure of FIR filter. As the symmetric structure is used, by its property the number of coefficients gets reduced from n to n/2 where 'n' is the order of the filter. Thus the number of coefficients gets reduced from 96 to 48. Hence the cost and design complexity is greatly reduced.

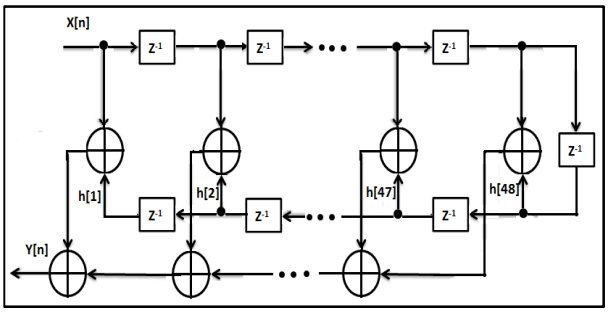

Figure 3: Architecture of the Filter

Adders, multipliers and delay elements are used to build the structure.Input,X[n] is fed to the first delay element as well as to the first adder. The filter coefficients h [1], h [2]….h [48] are given as input to the multipliers. By the property of linear convolution the inputs gets shifted by the delay elements and the output is obtained, Y[n].

5.FPGA Implementation

The SRRC filter structure is implemented using ALTERA Quartus II software for VHDL coding. Cyclone III Family is usedwith FPGA package and device used is EP3C120F780C7. Software provided by Altera is used to optimize and partition a design to fit it into logic cells and route the connections between the cells.

The Quartus II software's physical synthesis optimizations tightly couple the synthesis and fitting processes, and apply silicon-and design-specific timing information during the fitting/place-and-route process to perform additional synthesis optimizations, improving design performance.

Actions	AletraOpenCore Plus	Xilinx IP Evaluation
Functional Simulation	Yes	Yes
Functional verification	Yes-Designs may be compiled in the targeted device	Limited-not all cores are supported.
Program File Generation (hardware verification)	Yes-program files can be generated in designs with OpenCore plus cores	Limited-not all cores are supported.
Hardware Evaluation Without time limit	Yes-hardware evaluation is possible in two modes. Untethered and tethered.	No-only time limited operation is available for supported cores

Table 1: Altera's SOPC Builder Versus XPS

The Altera SOPC Builder is integrated into the Quartus II software and aids designers in building systems using processors and associated peripherals. Altera's OpenCore plus IP evaluation feature has the added advantage of allowing a designer to perform hardware evaluation of the IP without a timeout restriction as compared to Xilinx as shown in Table 1.

The VHDL description of the filter architecture is written where the filter coefficients are given as input to the multiplier blocks and simultaneously feeding the input to the adder and delay elements. The code is simulated and debugged for three set of filter coefficients that correspond to three different rolloff. Test bench is created using Modelsim. Gate level simulation is carried out that produces the output which can be crosschecked with Matlab output. The VHDL code is then loaded into the FPGA kit and output is viewed in Spectrum Analyser.

6.Performance Analysis

The magnitude response of SRRC filter for three different roll-offs 0.35, 0.25 and 0.2 are as shown in the Fig 4, 5 and 6, with different levels of ISI minimization from 0.35 down to 0.2 rolloff.

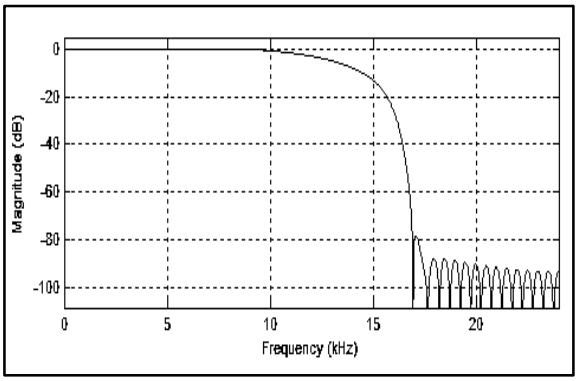

Figure 4: Magnitude response for roll-off of 0.35

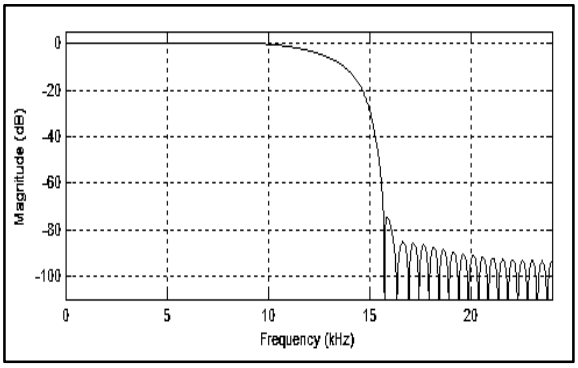

Figure 5: Magnitude response for roll-off of 0.25

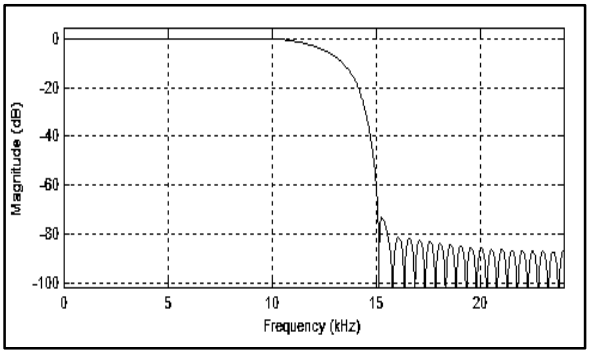

Figure 6: Magnitude response for roll-off of 0.2

DVB-S2 delivers excellent performance, coming close to the Shannon limit, the theoretical maximum information transfer rate in a channel for a given noise level. It shows the improvements in efficiency that DVB-S2 delivers when compared to DVB-S with typical TV broadcast parameters, with gains in the useful bitrate of more than 30% in each case as shown in Table 2 and 3.

Satellite EIRP (dBW)	51	
System	DVB-S	DVB-S2
Modulation & Coding	QPSK 2/3	QPSK ¾
Symbol Rate (Mbaud)	27.5 (α = 0.35)	30.9 (α = 0.2)
C/N (in 27.5MHz)(dB)	5.1	5.1
Useful Bitrate (Mbit/s)	33.8	46 (gain = 36%)
Number of SDTV Programmes	7 MPEG-2 15 AVC	10 MPEG-2 21 AVC
Number of HDTV Programmes	1-2 MPEG-2 3-4 AVC	2 MPEG-2 5 AVC

Table 2: comparison between DVB-S and DVB-S2 for TV broadcasting -0.2 rolloff

Satellite EIRP (dBW)	53.7	
System	DVB-S	DVB-S2
Modulation & Coding	QPSK 7/8	QPSK 2/3
Symbol Rate (Mbaud)	27.5 (α = 0.35)	29.7 (α = 0.25)
C/N (in 27.5MHz)(dB)	7.8	7.8
Useful Bitrate (Mbit/s)	44.4	58.8 (gain = 32%)
Number of SDTV Programmes	10 MPEG-2 20 AVC	13 MPEG-2 26 AVC
Number of HDTV Programmes	2 MPEG-2 5 AVC	3 MPEG-2 6 AVC

Table 3: comparison between DVB-S and DVB-S2 for TV broadcasting -0.25rolloff

The measured DVB-S2 performance gain over DVB-S is around 30% at the same satellite transponder bandwidth and emitted signal power as shown in Table 2 and 3.
DVB-S2 comparison results for three rolloffs is as shown in Fig 7.The output is SRRC filtered signal is fed to the DAC, DAC output after antialiasing is fed to quadrature modulator and the output of Quadrature modulator is an L-band which can be converted to c-band or ku-band as per system requirements.

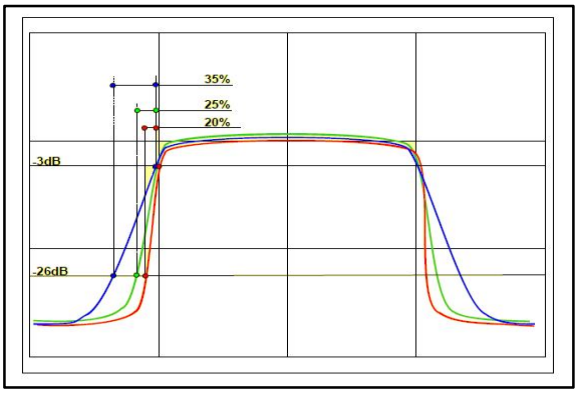

Figure 7: Comparison of Results

The smooth characteristics of the raised cosine filter spectrum, makes it possible to design practical filters that approximates the overall desired frequency response. The response of the SRRC Filter through Spectrum Analyser is as shown in Fig 8.

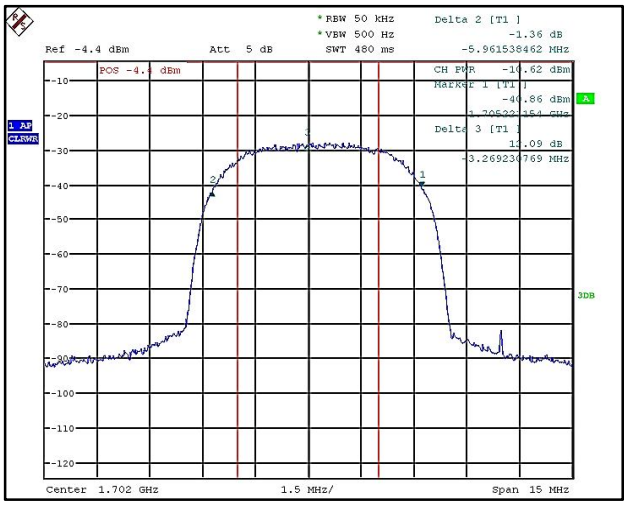

Figure 8: Response of filter through Spectrum Analyser

DVB-S2 achieves a significantly better performance than its predecessors – mainly allowing for an increase of available bitrate over the same satellite transponder bandwidth, as shown in Fig 8.

The conversion process from DVB-S to DVB-S2 is being accelerated, due to the rapid increase of HDTVand introduction of 3D-HDTV.

5.Conclusion

In this paper, the design and implementation of SRRC filter as per DVB-S2 standard is addressed. The proposed scheme provides flexibility to work with three different roll-offs with different levels of ISI minimization which is application dependent.The measured DVB-S2 performance gain over DVB-S is around 30% at the same satellite transponder bandwidth and emitted signal power.

The use of Direct form symmetric structure makes the hardware implementation cost less with lesser number of logic elements.TheAletraQuartus II software's physical synthesis optimizations tightly couple the synthesis and fitting processes and hardware evaluation of the IP without a timeout restriction.

In summary, the proposed implementation of SRRC filter fits the DVB-S2 standard related applications.

6.Reference

1. ETSI en 302 307 "Digital Video Broadcasting (DVB); Second Generation Framing Structure, Channel Coding And Modulation Systems For Broadcasting, Interactive Services, News Gathering And Other Broadband Satellite Applications," v.1.2.1 , European Telecommunications Standards Institute 2009.
2. A. Morello and V. Mignone. "DVB-S2:The Second Generation Standard for Satellite Broad-Band Services" Proc. IEEE, vol.94, no. 1, pp. 210-27, 2006.
3. ETSI EN 300 421 "Digital Video Broadcasting (DVB); Framing Structure, Channel Coding and Modulation for 11/12 GHz Satellite Services," V1.1.2, Aug. 1997;http://www.etsi.org.
4. AbdolhadiAlizadeh, "Feature Analysis of the Second Generation Standard DVB-S2 for Satellite Broad-Band Services" TCSET, 2010.
5. Mohamed Al Mahdi Eshtawie, and Masuri Bin Othman, "An Algorithm Proposed for FIR Filter Coefficients Representation", International Journal of Applied Mathematics andComputer Sciences, Vol 4 No. 1, 2008'
6. Charan Litchfield, Prof. R.J Langley, Peter Lee and Dr. John Batchelor "The Use of Hybrid Logarithmic Arithmetic for Root Raised Cosine Matched Filters in WCDMA Downlink Receivers", Wireless Communications and Networking Conference, 2005 IEEE 200, Vol 1
7. K. Macpherson, I. Stirling, G. Rice, D. Garcia-Alis and R. Stewart "Arithmetic Implementations and Methodologies for 3g Uplink Reception In Xilinx FPGAS" 3G Mobile CommunicationTechnologies, 2002, Third International Conference, 2002.
8. Harish, P.S and Karthik, S. "Root Raised Cosine Filter for A WCDMA Receiver UsingDistributed Arithmetic for Power Optimization and Enhanced Speed" Intelligent SignalProcessing and Communication Systems, Proceedings International Symposium on, 2004.
9. Changyong Pan, Yingying Lu, KewuPeng and Hui Yang. "Low-Complexity Implementation of High Order SRRC Filter" Proc. IEEE, 2009.
10. Zhang Weiliang, Pan Changyong and GuoXingbo, YangZhixing. "Design And FPGA Implementation Of High-Speed Square-Root-Raised-Cosine FIR Filters" IEEE, 2002
11. JueHsuanHsiao, Yi Hua Chen, Chih Hung Tseng, Pang Fu Liu, Kun Feng Lin. "Design and Implementation Of SRRC IP Generator."IEEE, 2011.

12. Chia-Yu Yao and Chiang-JuChien, “The Design Of A Square-Root-Raised-Cosine FIR Filter by a Recursive Method” IEEE, 2005.
13. GeorgiosGardikis and AnastasiosKourtis, “Using DVB-S2 Adaptive Coding And Modulation for the Provision of Satellite Triple Play Services” IEEE Communications Magazine, December 2008.
14. Bruce Bennett AndKensingQuock, “DVB-S2 Technology Development ForDoD IP SATCOM” Military Communications Conference, 2006. MILCOM.