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Design of Efficient Parallel Self Timed Adders in TANNER EDA using GDI Technique

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Abstract:
This paper presents a parallel single-rail self-timed adder for adding multi-bit. In today's world there is a great need for low power design and high area efficient performance. Self-timed adders have the potential to run faster averaged for dynamic data. In existing PASTA system, high fanouts required but which could solve by connecting transistors in parallel manner. Even though which increases the design size. So that power consumption also increased. So here going to implement the new technique called GDI [Gate Diffusion Input]. This new implementation for reduction in power consumption, delay, transistor count more than PASTA. This design includes completion detection unit for the output generation. Simulation for the proposed design have been performed using Tanner Tool v14.11 and verify the practicality and working manner of the proposed approach over existing PASTA design.

Keywords: *PASTA [Parallel Self Timed Adder], Self- Timed Adder, GDI [Gate Diffusion Input].*

1. Introduction

Adders are considered to be the heart of computational circuits and addition has been the core for many complex arithmetic circuits. Thus enabling the researchers to use addition for lot of applications. The rapid advancement in semiconductor technology with the shrinking transistor size towards 16nm has allowed for placement of several billion transistors on a single microprocessor chip [1]. Processors perform addition as the most important operation. Most of the adders have been designed for asynchronous circuits as asynchronous circuits do not assume any quantization of time and some still use synchronous circuits as well. Thus, having free from various problems of clocked (synchronous) circuits. Here we have generated the design of binary adders and concentrated on asynchronous self-timed adders. [1]-[4].

1.1. Self-Timed Adders

Self timed describes the logic circuits that depend on timing assumptions for the correct operation of the circuit. Self-timed adders have the capacity to run faster averaged for dynamic data, that early completion sensing can avoid delay mechanism of synchronous circuits.

Self-timed points to logic circuits that depend on or engineer timing assumptions for the correct operation. These Self-timed adders have the capacity to run faster than the conventional circuit design. This paper presents an asynchronous parallel self-timed adder (PASTA). This design uses half-adders (HAs) with the multiplexers requiring minimum interconnections. Thus, making way for many VLSI implementations.

For independent carry chain blocks PASTA works in a parallel manner. There are four levels of minimization of power dissipation in CMOS based system designs: technology, circuit, architecture and algorithm. Generally choosing appropriate circuit design style 20% to 30 % power can be saved in circuit level. When handling with the increasing challenges of digital circuit's design the GDI Technique is superior.

Self-timed circuit which is a sequential digital logic circuit is not controlled by global clock signal or clock circuit but they often use signals that depict the completion of operation and instructions.

The remainder of this report is organized as follows. Section II provides an information about GDI cell. Section III presents the design of the proposed adder. Sections IV and V implementation and simulation results for the proposed adder and comparison. Section VI draws the conclusion.

2. Basic GDI Cell

Basic GDI cell look as such as inverter in CMOS logic, but functionality is totally different. Figure 1 displays the basic GDI cell, which clearly illustrates the Source of P-type, connected to P pin and NMOS source connected to the N pin.

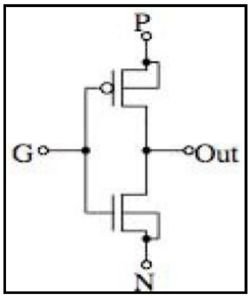


Figure 1: Basic GDI function

N	*P*	*G*	*Out*	*Function*
'0'	B	A	$\overline{A}.B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	A+B	OR
B	'0'	A	A.B	AND
Sel	B	A	$\overline{A}.B+A(Sel)$	Mux
'0'	'1'	A	$\overline{A}$	Not

Table 1: GDI Function

2.1. Pipelined Adders using Single Rail Encoding

The asynchronous Request/Acknowledge handshake can be used to enable the adder block as well as to establish the carry signals flow. These dual-rail signals can represent more than two logic values (invalid, 0, 1) and when a bit operation is completed logic level can be used to generate bit-level acknowledgment.

The carry completion sensing adder is an example of a pipelined adder [8], which uses full adder (FA) functional blocks adapted for dual-rail carry. On the other hand, a speculative completion adder is proposed in [7].

2.2. Delay Insensitive Adders Using Dual Rail Encoding

Delay insensitive (DI) adders are asynchronous adders that assert bundling constraints or DI operations. There are many variants of DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). DI adders use dual-rail encoding and are assumed to increase complexity the carry signals in a chain but rather organize them in a hierarchical tree. Thus, they can potentially operate faster when there is long carry chain. Using dynamic logic or only nMOS designs dual-rail encoding can still be used to produce circuits as efficient as that of the single-rail variants though it doubles the wire complexity. One example where 40transistors per bit is used in DIRCA adder while the conventional CMOS RCA uses only 28 transistors making drastic reduction in transistor count.

- Some design techniques for digital integrated circuit are as below:

a) CMOS design technique: Most of logic gates in VLSI uses standard CMOS circuits with complementary pMOS pull-up networks and nMOS pull-down design. This is because they have low power insensitive to device variations, good noise margin, fast and can be easily designed using any of the tools one among is Cadence. The AC power caused by the charge and discharge of capacitances helps in determining the power consumption of conventional CMOS circuit: Power = CV2f ---- (1) where f is the frequency at which the capacitance charges and discharges. The frequency goes up as does the power consumption when the circuits get faster.

b) Pass Transistor Logic: To reduce the number of transistor required to implement logic an alternative to complementary CMOS is pass transistor logic, which allows the primary inputs to drive source drain terminal and also gate terminal. By adopting a circuit named CPL the complexity of full CMOS pass gate logic can be reduced dramatically. The main intension of using CPL logic is to use only NMOS pass transistor network for the logic operations. Every input signal and its inverse must be provided i.e. inputs are applied in complementary form. Consequently, we get the complimented output which may be used by subsequent CPL. To construct complex Boolean function pass-transistor logic is used which uses fewer transistors. Thus the advantages of lower capacitance by using reduced number of devices. Another advantages due to small node capacitances is high speed. Also reduced number of transistors and lower interconnection effects due to low power dissipation.

c) Dual Pass Transistor Technique: This has twice as the number of transistors as CPL for any particular function. Covering every input vector in the Karnaugh map twice is the logic behind the design of DPL. The design of parallel self-timed adder is carried out using all these above techniques to check for the variation in the efficiency. But the disadvantage of these design is the number of transistor. This paper implements a new low power design technique that solves most of the problems in above digital design. Using only two transistors GDI approach allows implementation of a various logic functions. For design of fast, low power circuits with less number of transistors this method is best suited.

d) GDI technique: The GDI method uses simple cell as shown. This basic GDI cell is the conventional CMOS inverter, but there are some modifications made they are:

i) The three inputs of GDI cell are:

P (input to the source/drain of pMOS),
G (common gate input of nMOS & pMOS),
N (input to the source/drain of nMOS).

ii) In comparison with a conventional CMOS inverter bulks of both nMOS and pMOS are connected to N or P (respectively) and can be biased.

Those functions which cannot be implemented using standard p-well CMOS process can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies. The most complex design that can be implemented with GDI is the MUX design. Traditional CMOS or PTL design requires 8-12 transistors unlike GDI design which requires 2 transistors only.

3. Design of PASTA using GDI

The architecture and theory of PASTA is explained. This adder initially accepts two input operands to perform half adder additions for every bit. Later it keeps iterating using previously generated sums and carry to perform half adder additions continuously till where all carry bits are at zero level.

3.1. Architecture of PASTA

The architecture of the PASTA adder is shown in Figure2. The Req handshake signal is corresponded to selection input for two input multiplexers and will be a single 1 to 0 transition denoted by SEL. Initially it will select the actual operands 'a' and 'b' during SEL = 0 and when SEL = 1 it will switch to feedback/carry paths for subsequent iterations. Multiple iterations are enabled by feedback path from the HAs which continues till the completion of all carry signals to assume zero value.

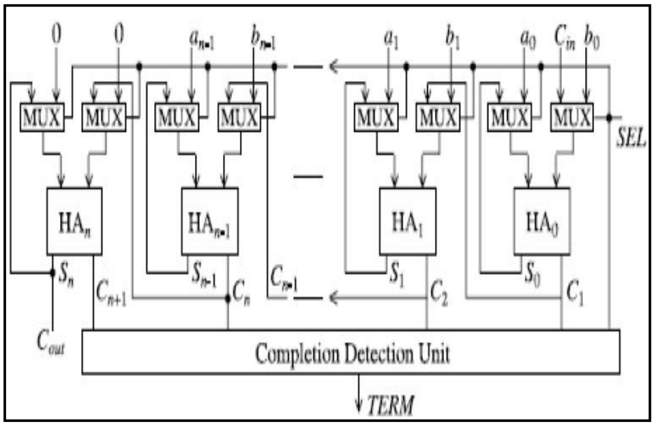


Figure 2: General Block Diagram of PASTA

3.2. State Diagrams

We have Figure3 which depicts the two state diagrams for initial phase and then iterative phase of the above architecture. Each state is depicted by (Ci+1 Si) pair where Si, Ci+1 represent carry out and sum values respectively, considering the ith bit adder block. During the iterative phase i.e. when (SEL = 1), the feedback path through multiplexer block is activated. To complete the recursion, the carry transitions (Ci) is generated various times as needed. During the initial phase, the circuit works as a combinational HA. State (11) cannot appear because of the use of HAs instead of FAs.

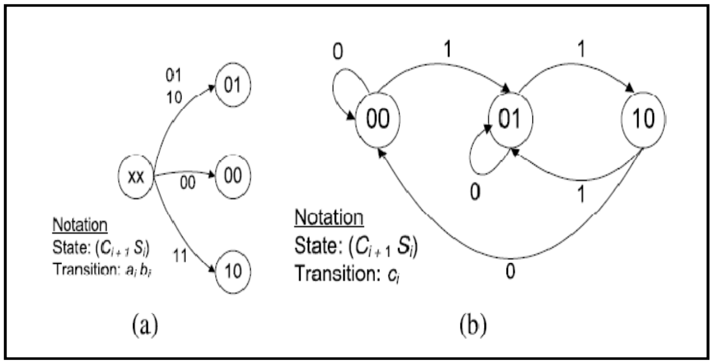


Figure 3: Two states of PASTA

3.3. Recursive Formula for Binary Addition

Let us consider S ji and C ji+1 as sum and carry respectively, at the j th iteration for ith bit. The initial condition (j = 0) for half adder addition is obtained as below:

$S0_i = a_i \oplus b_i$

$C0_{i+1} = a_i\ b_i$ ....(1)

For the recursive addition the j th iteration is obtained by,

$S_{ji} = S_{j-1} \oplus C_{j-1i}$, $0 \le i < n$.......(2)

$C\ j_{i+1} = S_{j-1i}\ C_{j-1i}$, $0 \le i \le n$.......(3)

At kth iteration the recursion is terminated i.e. when the below condition is satisfied:

$C_{kn} + C_{kn-1} + \cdot\ \cdot\ \cdot + C_{k1} = 0$, $0 \le k \le n$........(4)

4. Implementation

For the recursive circuit conventional CMOS implementation is depicted in Figure4. We have used Tanner Tool v14.11 for implementing multiplexers and HA blocks. The SEL will be negated when considering completion detection unit to generate an active high completion signal (TERM). An practical alternative pseudo-nMOS ratio-ed design requiring a large fan-in n-input NOR gate. As all the connections are in parallel the completion detection unit avoids the high fan-in problem. to VDD of this ratio-ed design the pMOS transistor is connected when few nMOS transistors are on simultaneously resulting in static current drain . The negative of SEL signal is also included for the TERM signal in addition to the Ci s, to ensure that during the initial selection phase of the actual inputs the completion cannot be accidentally turned on and in turn preventing the pMOS pull up transistor from being always on.

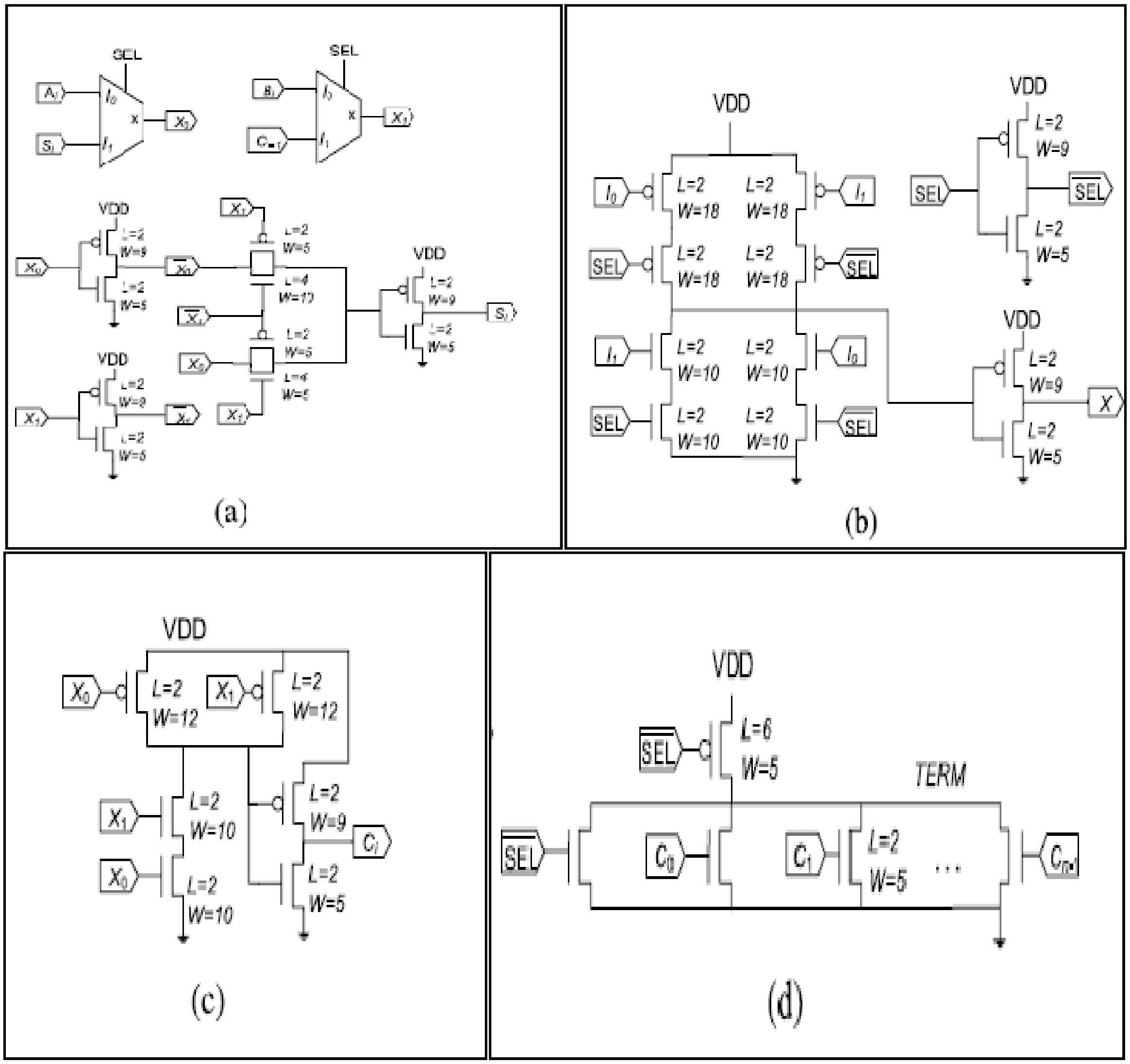


Figure 4: CMOS implementation of PASTA. (a) Single-bit sum module. (b) 2×1 MUX for 1-bit adder. (c) Single-bit carry module. (d) Completion signal detection circuit.

5. Simulation Results and Comparisons

We have generated the output for PASTA using the conventional CMOS technique for two cases of SEL to be either 0 or 1 and designing and comparing with the proposed modified GDI technique for better efficiency as shown in Figure. 5 below.

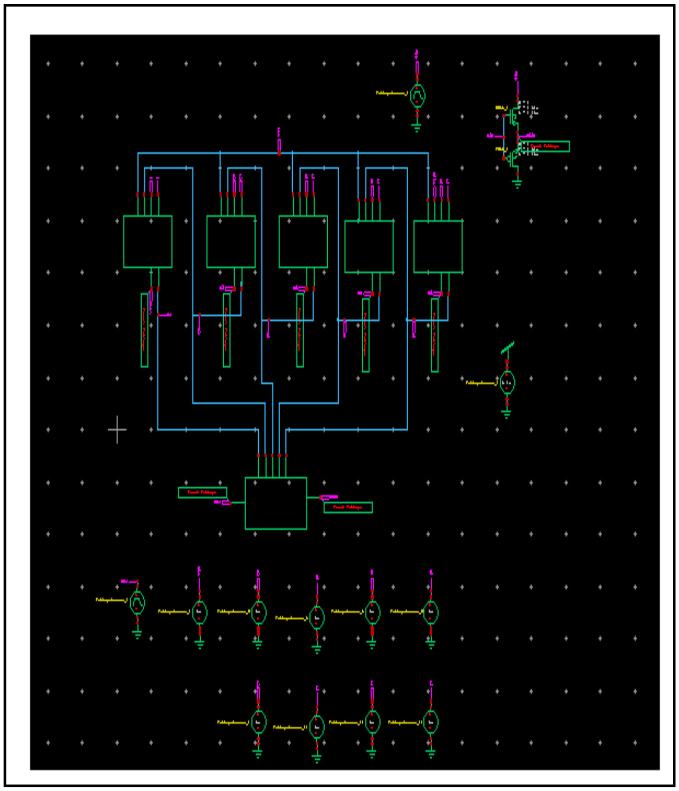
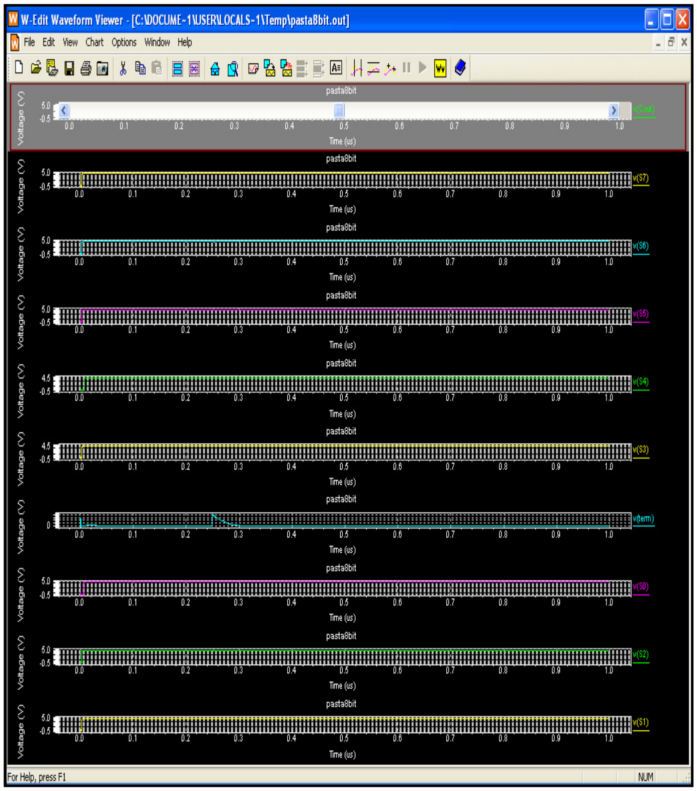


Figure 5: Schematic of PASTA


W-Edit Waveform Viewer - [C:\DOCUME~1\USER\LOCALS~1\Temp\pasta8bit.out]
File Edit View Chart Options Window Help
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Voltage (V)
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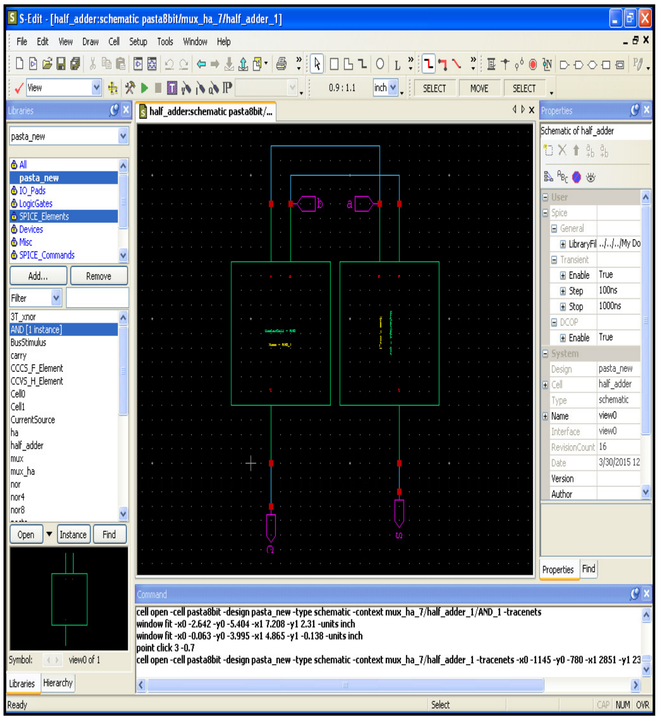
Figure 6: Proposed pasta with new xor



Schematic of half_adder

User
Spice
General
LibraryFil ../../../My Do
Transient
Enable True
Step 100ns
Stop 1000ns
DCOP
Enable True
System
Design pasta_new
Cell half_adder
Type schematic
Name view0
Interface view0
RevisionCount 16
Date 3/30/2015 12
Version
Author

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cell open -cell pasta8bit -design pasta_new -type schematic -context mux_ha_7/half_adder_1/AND_1 -tracenets
window fit -x0 -2.642 -y0 -5.404 -x1 7.208 -y1 2.31 -units inch
window fit -x0 -0.063 -y0 -3.995 -x1 4.865 -y1 -0.138 -units inch
point click 3 -0.7
cell open -cell pasta8bit -design pasta_new -type schematic -context mux_ha_7/half_adder_1 -tracenets -x0 -1145 -y0 -780 -x1 2851 -y1 23
```

Figure 7: Single stage of PASTA[GDI]

The same above architecture was implemented using GDI, Recursive techniques for various combinations and compared the trade-offs like power, delay and frequency. The result was also initially implemented with 180nm technology as the base and later was design using 90nm and 45nm technology and was compared with the standard 180nm technology.

FUNCTION	GDI	Recursive
INVERTER	2	2
AND	2	6
OR	2	6
XOR	4	16
MUX	2	12
HA	6	10

Table 2: Comparison of transistor count

Power at	GDI(W)	Recursive (W)
Average	2.550e-001	1.267e-001
Maximum	6.810e+002	2.092e+003
Minimum	0.003e+000	1.683e-005

Table 3: Comparison of Power

GDI	Recursive
49.98M	50.0M

Table 4: Comparison of frequency (Hz)

GDI	Recursive
73.8P	83.2P

Table 5: Comparison of delay (sec)

6. Conclusion

An efficient adder PASTA was implemented using GDI technique in order to get better performance. For independent carry chains the circuit works in a parallel manner. Over random input values logarithmic average time performance is achieved. We also obtained practical and efficient completion detection unit for this proposed adder. We could obtain the power to be reduced by 20% to 30 % which contributes for a greater efficiency. For Basic logic gates GDI technique was implemented and comparisons were made with recursive approach. The result showed that the GDI technique gave a better and efficient output and a best technique for power reduction, frequency and delay. Various other analysis like DC, AC, noise, senc was carried out to establish a better output in all cases.

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