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Reduction of Common Mode Voltage in Induction Motor Drives Using Various Scalar Based PWM Techniques

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Abstract:

This paper presents reduced Common-Mode Voltage Pulse width modulation (RCMV-PWM) algorithms for the three-phase voltage source inverter driven Induction motor. PWM methods are reviewed and their pulse patterns and common mode voltage patterns illustrated. However, the Space Vector PWM (SVPWM) algorithm gives more Common Mode Voltage (CMV) variations due to the usage of zero voltage vectors. Moreover, the conventional SVPWM algorithm needs the angle and sector information for the calculation of switching times, which increases the complexity of PWM algorithm. Hence, to reduce the complexity involved in the PWM and CMV variations various PWM algorithms have been developed using the concept of imaginary switching times of carrier based scalar approach. In the proposed approach, by adding a unique zero sequence signal to the phase voltages, the modulating signals are derived. Then by comparing the modulating signals with triangular signals, the gating pulses for the various PWM algorithms are derived. As the proposed PWM algorithms did not use the zero states, these results in reduced CMV variations. To validate the proposed algorithms, several numerical simulation studies have been carried out on scalar controlled induction motor drive. Finally, the simulation results have to be compared with the existing methods.

Keywords: Common Mode Voltage, SPWM, SVPWM, Scalar approach, DPWM, AZSPWM.

1. Introduction

In the past DC motors were widely preferred since control of a DC motor is easy and its speed can be Controlled by changing its Terminal voltage. However, they have disadvantages against AC induction motors such as their initial and maintenance costs. AC motors are economical but it is impossible to control an AC motor efficiently by directly feeding it from the AC grid. Therefore, Adjustable Speed Drives (ASD) were developed. Nowadays the adjustable speed induction motor drives becoming very popular in many industrial applications due to their rugged construction and reliable operation. Three-phase Voltage Source Inverters (VSIs) are widely utilized to drive AC motors with high motion control quality and energy efficiency. Hence in order to obtain the controllable supply from the inverter, recently the PWM algorithms are introduced. However, there is a large load star point to the center of the dc-bus of the VSI (V_{no} in Fig.1) potential and can be expressed as [6] variety of PWM methods that exhibit unique performance characteristics and the choice and utilization of a specific PWM method among many is not a simple task. A detailed survey on various PWM algorithms is studied in [1]. PWM mostly involves the standard Continuous PWM (CPWM) methods such as the Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM), and the Discontinuous PWM (DPWM) methods. However, the performance characteristics of the recently developed Reduced Common Mode Voltage PWM (RCMV-PWM) methods are also studied [2].

In the standard three-phase two-level Voltage Source Inverter (VSI) with diode rectifier front-end, which is shown in fig.1. The CMV is defined as the potential of the star point of the load with respect to the power line ground (V_{ng}) shown in Fig.1. Which is expressed as $V_{ng} = (V_{no} + V_{og})$. Since V_{og} being much smaller and slowly varying signal compared to

V_{no} , the V_{og} term can be neglected. Therefore, the CMV of the inverter is equal to $V_{ng} = V_{no}$. This is defined as the

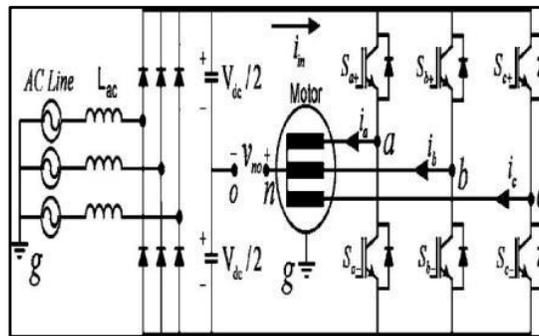


Figure 1: Three phase VSI fed induction motor with diode rectifier front end

Follows: The inverter pole voltages are given by,

$$V_{ao} = V_{an} + V_{no} \quad (1)$$

$$V_{bo} = V_{bn} + V_{no} \quad (2)$$

$$V_{co} = V_{cn} + V_{no} \quad (3)$$

By adding above three equations since, the instantaneous phase voltages are zero i.e. $V_{an} + V_{bn} + V_{cn} = 0$. Then the above equation reduces to,

$$V_{no} = V_{ng} = (V_{ao} + V_{bo} + V_{co})/3. \quad (4)$$

When the induction motor is fed from a 3-phase balanced supply, the CMV is zero. Since the VSI cannot provide sinusoidal voltages and has discrete output voltages synthesized from fixed dc-bus voltage V_{dc} , always VSI exhibits the CMV variations. The amplitude of the CMV is always different from zero and may take the values of $\pm V_{dc}/6$ or $\pm V_{dc}/2$, will depend on the inverter switching states selected. All conventional CPWM and DPWM methods exhibit high CMV characteristics that pose problems in the application field. At switching frequencies above several kilohertz, excessive CMV with sharp edges can result in high Common Mode Currents (CMC). In motor drive applications, this may lead to motor bearing failures, electromagnetic interference noise that causes nuisance trip of the inverter drive, or interference with other electronic equipment in the vicinity. In the application field, such problems have increased recently due to increasing PWM frequencies and faster switching time and CMV reduction techniques have gained importance. Passive or active filters can be utilized to suppress the effect of the CMV of two-level inverter [7]. Also, a three-level inverter could be employed to decrease the CMV from the source [7]. However, all these methods involve external/additional hardware, and thus, they significantly increase the drive cost and complexity. An alternative approach is to modify the PWM pulse pattern of the classical two-level inverter. Hence, nowadays, many researchers focused their interest on the development of various PWM algorithms [2] for the CMV effects to mitigated at no cost. In the survey, various PWM pulse-pattern-modification based CMV reduction methods have been reported. To be classified as reduced CMV PWM (RCMV-PWM) methods such as Active-Zero State PWM (AZSPWM), Remote-state PWM (RSPWM), Near state PWM (NSPWM) these are the most successful representatives. In all these methods the maximum CMV is reduced from $\pm V_{dc}/2$ of the conventional

PWM methods to $\pm V_{dc}/6$, and also with this type PWM switching the switching loss also reduced. But while in conventional CPWM such as SPWM, SVPWM, and DPWM are the methods with maximum CMV varies between $\pm V_{dc}/2$ to

$\pm V_{dc}/6$ these variations are due to the usage of zero voltage vectors. Therefore, it is necessary to eliminate usage of zero voltage vectors this is achieved in RCMV-PWM methods [4].

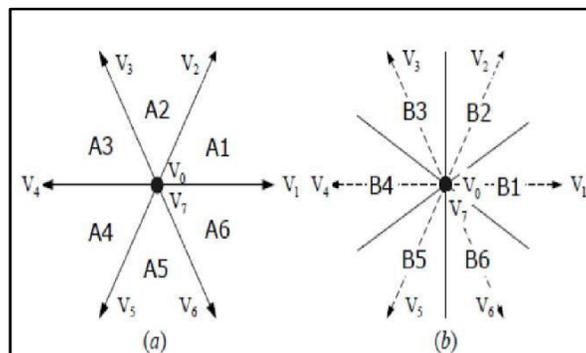


Figure 2: Voltage space vectors of A-type and B-type regions

When implementing the PWM methods and analyzing the VSI output voltages, the space vector approach can be utilized. Since it is two-level VSI there are eight possible voltage vector states are available, out of these voltage vectors, six of them (V1, V2, V3, V4, V5, and V6) are active voltage vectors, and two of them (V0 and V7) are zero voltage Vectors and (A1, A2, A3, A4, A5, A6) are six-sectors with each sector 60°. The active voltage vectors result in non-zero line-to-line voltage at least between two phases and the zero voltage vectors result in zero line-to-line voltage between all the phases. The sequence of the voltage vectors is selected based on a specified performance criterion. Each PWM method utilizes different voltage vectors and sequences and the utilized voltage vectors alternate throughout the vector space [3].

From TABLE.1, it can be concluded that the CMV may take the values $\pm V_{dc}/6$ for the active states and $\pm V_{dc}/2$ for zero states. Hence for the reduction of CMV, the zero states should be avoided.

Switching states	Inverter Pole Voltages			Vng= Vno (CMV)
	Vao	Vbo	Vco	
V0 (000)	-Vdc/2	-Vdc/2	-Vdc/2	-Vdc/2
V1(100)	Vdc/2	-Vdc/2	-Vdc/2	-Vdc/6
V2(110)	Vdc/2	Vdc/2	-Vdc/2	Vdc/6
V3(010)	-Vdc/2	Vdc/2	-Vdc/2	-Vdc/6
V4(011)	-Vdc/2	Vdc/2	Vdc/2	Vdc/6
V5(001)	-Vdc/2	-Vdc/2	Vdc/2	-Vdc/6
V6(101)	Vdc/2	-Vdc/2	Vdc/2	Vdc/6
V7(111)	Vdc/2	Vdc/2	Vdc/2	Vdc/2

Table 1: Pole Voltage and CMV Generated for Various Switching States

2. Realization of Space Vector PWM

The Space Vector Pulse Width Modulation (SVPWM) refers to a special switching sequence of the upper three power devices of a three-phase voltage source inverters (VSI) used in application such as AC induction motor drives. It is a more sophisticated technique for generating sine wave that provides a higher voltage to the motor. Space Vector PWM (SVPWM) method is an advanced; computation technique intensive PWM method and possibly the best techniques for variable frequency drive application. In SVPWM technique, where the complex reference voltage vector is processed as a whole. Although SVPWM is more complicated than sinusoidal PWM. The space vector PWM is realized based on the following steps:

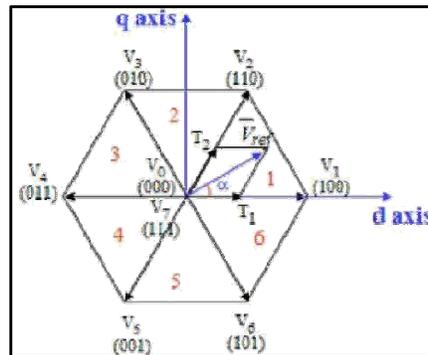


Figure 3: SVPWM switching vectors and sectors selection

The reference voltage vector (Vref) is sampled at equal intervals of time, Ts referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different time durations with in a sampling time period such that the average vector produced over the sampling time period is equal to the sampled value of the Vref, both in terms of magnitude and angle. It has been established that the vectors to be used to generate any sample are the zero voltage vectors and the two active voltage vectors forming the boundary of the sector in which the sample lies. As all six sectors are symmetrical for the required reference voltage vector, the active and zero voltage vectors times can be calculated as in (5), (6) and (7).

$$T1 = (2\sqrt{3}/\pi) * Mi * \sin(60^\circ - \alpha) * Ts \quad (5)$$

$$T2 = (2\sqrt{3}/\pi) * Mi * \sin(\alpha) * Ts \quad (6)$$

$$Tz = Ts - (T1 + T2) \quad (7)$$

Where Mi is the modulation index and Tz total zero

voltage vector time equally divided between V_0 and V_7 and distributed symmetrically at the start and end of each sampling time period. Thus, SVPWM uses 0127-7210 in Sector-I, 0327-7230 in sector-II and so on [5]. Since SVPWM algorithm needs the angle and sector information for the calculation of switching times, which increases the complexity of PWM algorithm. Hence, to reduce the complexity involved in the PWM and CMV variations various PWM algorithms have been developed using the concept of imaginary switching times of carrier based scalar approach.

3. Generalized Scalar Based Pwm

Based on the implementation technique, PWM methods are defined as scalar or space vector techniques. In the proposed scalar approach, by adding the zero sequence signal to the instantaneous phase voltages, the modulating signals are generated. Then the modulating signals are compared with a triangular carrier wave (V_{tri}) peak will be $(\pm V_{dc}/2)$ and the intersection points determine the switching instants for switches is shown Fig.4.

Assume a set of three phase voltages as given in,

$$V^*_{in} = V_{ref} \cos(\alpha - 2(r-1)\pi/3) \tag{8}$$

Where V^*_{in} is reference signal for $i = a, b, c$. w.r.t $r = 1, 2, 3$.

By adding a zero sequence signal to the above instantaneous phase voltages (V_zs), the modulating signals (V^{**}_{in}) can be derived as,

$$V^{**}_{in} = V^*_{in} + V_zs \tag{9}$$

where V_zs is the zero sequence signal, which is given as ,

$$V_zs = (V_{dc}/2) * (2k_0 - 1) - k_0 V_{max} + (k_0 - 1) V_{min} \tag{10}$$

Where V_{max} and V_{min} are maximum and minimum values of V^*_{in} and in this approach k_0 is constant value varying between 0 and 1.

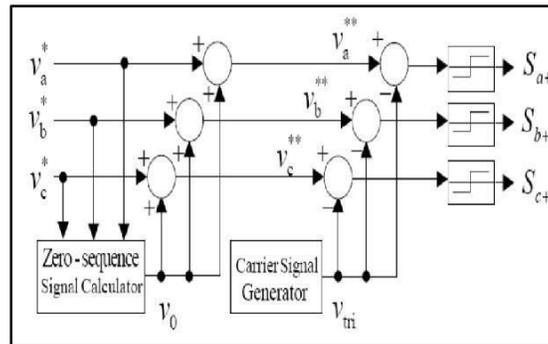


Figure 4: block diagram of the conventional scalar PWM method employing zero-sequence signal injection

The injection of a zero-sequence signal simultaneously shifts all the reference waves up or down with the same amount (with respect to the carrier wave). Therefore, the average value of line-to-line voltages in one carrier period is not affected. But the positions of the output line-to-line voltage pulses are varied with the zero-sequence signal injection. Therefore, it significantly influences the harmonic distortion, voltage linearity, and switching loss characteristics. With a proper zero-sequence signal injection infinite PWM methods are obtained. Usually one common carrier triangle wave will be used in the scalar approach. But in order to obtain the pulse pattern of AZSPWM two carrier waves (V_{tri} and $-V_{tri}$) must be utilized. SVPWM, AZSPWM, methods are CPWM methods with the same zero-sequence signal. Likewise, DPWM method with the same zero-sequence signal and modulation wave. Even though the modulation wave is the same, using different triangular waves makes these PWM methods different and performance characteristics such as CMV, current/voltage ripple and voltage linearity differ [4].

4. Switch Logic Signal, Output Voltage and CMV Patterns for Various PWM Methods

The performance characteristics of a PWM method are primarily dependent on the modulation index M_i , that is defined as,

$$M_i = |V_{ref}| / (2/\pi) * V_{dc} \tag{11}$$

Where V_{ref} is magnitude of instantaneous phase-voltage fundamental component [2].

Based on the modulation signal, conventional PWM methods are classified as the Continuous PWM (CPWM) (SVPWM, SPWM, etc.) method and the DPWM (DPWM1,2, etc.) method. The pulse pattern of the CPWM and DPWM methods involves utilization of at least one of zero voltage vector V_0 and V_7 during each PWM cycle. The switch pulse pattern of the SVPWM method ($t_0=t_7$) is shown

in Fig. 5(a) in such patterns i.e., (CPWM and DPWM methods) yield high common mode voltage ($\pm V_{dc}/2$). Hence, several PWM pulse patterns that yield reduced common mode voltage have been reported. These, and several low common mode voltage methods reported in this approach will all be grouped under the name of RCMV-PWM methods.

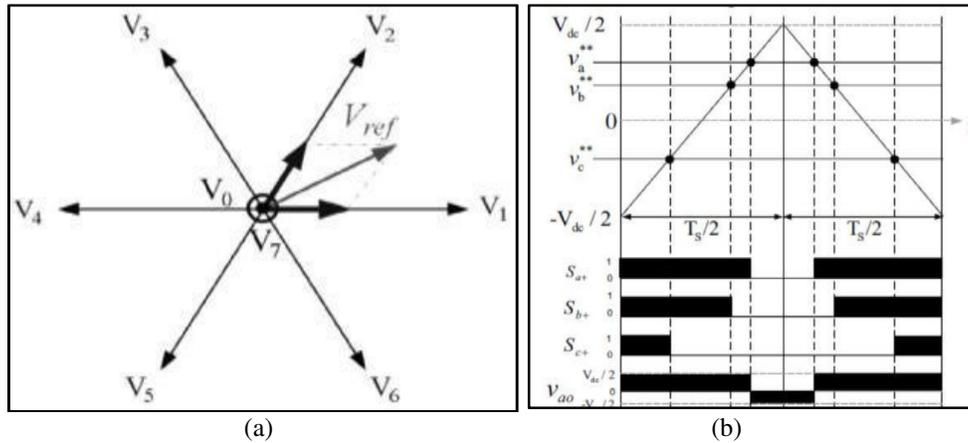


Figure 5: (a) voltage space vectors, and (b) SVPWM modulating signals, switch logic, phase and Line-line voltage and CMV pulse pattern

In DPWM1 utilize two active vectors adjacent to the reference voltage vector. While only one of the zero states (V_0 or V_7) and one switch is retained in a fixed state for a full PWM cycle, for every 60° , the active vectors change, but the zero state and their locations are retained. Thus switching losses are decreased by 33% compared to SVPWM.

In SVPWM utilize two active vectors adjacent to the reference voltage vector and the two zero vectors with equal time duration ($t_0=t_7$) in each PWM cycle.

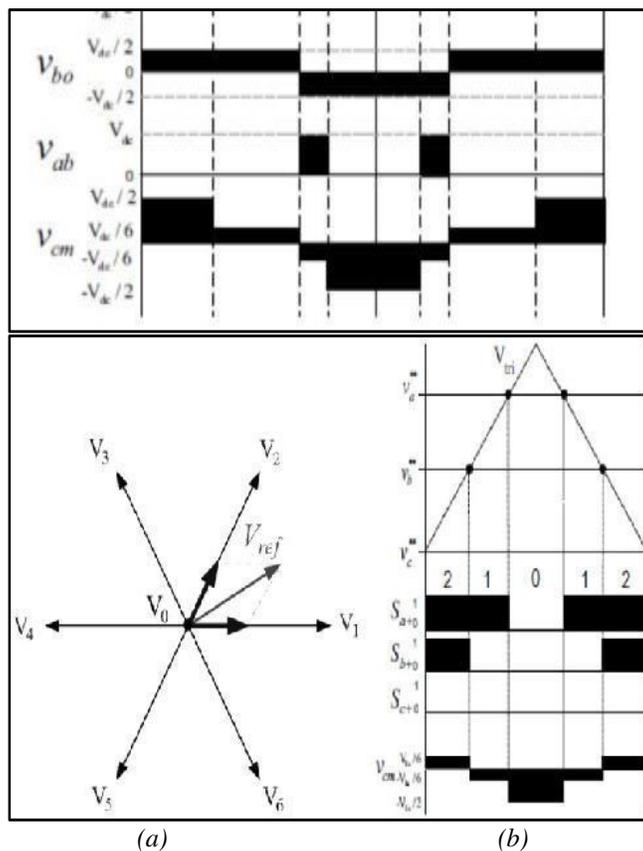


Figure 6: (a) voltage space vectors, and (b) DPWM1 pulse pattern and CMV pattern

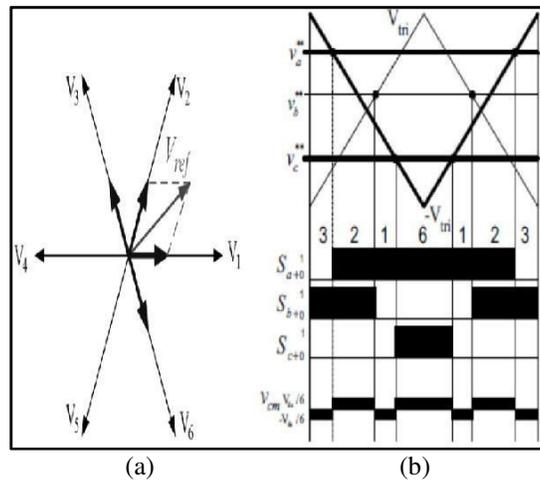


Figure 7: (a) voltage space vectors, and (b) AZSPWM pulse pattern and CMV pattern

In AZSPWM utilize the same active vectors as in SVPWM. However, instead of the real zero voltage vectors (V_0 and V_7), two active opposite voltage vectors with equal time duration are utilized to create an effective zero vector. For example, in A1 region, the V3-V6 pair is utilized since these vectors are adjacent to the V1-V2 vectors [3].

The pulse patterns and the resulting CMV for the specific regions of the voltage vector space is shown above. As absorbed from the above figures, in these RCM-PWM methods, the inverter zero states are avoided and resulting in low CMV ($\pm V_{dc}/6$).

In each PWM method, with specific performance optimization criterion, the voltage vectors are selected, and their sequences depend on the region of the reference voltage vectors which is defined in Fig. 2(a) and (b). The utilized voltage vectors and their sequences for the conventional and RCMV-PWM methods are given below in [2] Table II.

SVPWM	A1		A2		A3		A4		A5		A6	
	7210-	0127	7230-	0327	7430-	0347	7450-	0547	7650-	0567	7610-	0167
DPWM1	A1	B2	A2	B3	A3	B4	A4	B5	A5	B6	A6	B1
	210-012	723-327	430-034	745-547	650-056	761-167						
AZSPWM	A1		A2		A3		A4		A5		A6	
	3216-	4321-	5432-	6543-	1654-	2165-						
	6123	1234	2345	3456	4561	5612						

Table 2: Region-Dependent Vector Patterns of Various Pwm Methods

5. Simulation Results and Discussions

To prove the performance and verify the results of proposed PWM algorithms, the simulation studies have been carried out on 4-kW, 400-Vrms line-line, four-pole,50-Hz, 1430- rpm induction motor that is driven from a PWM-VSI is simulated. the constant switching frequency is taken as 5kHz. The steady state results during the no-load condition at modulation index of $M_i = 0.78$.

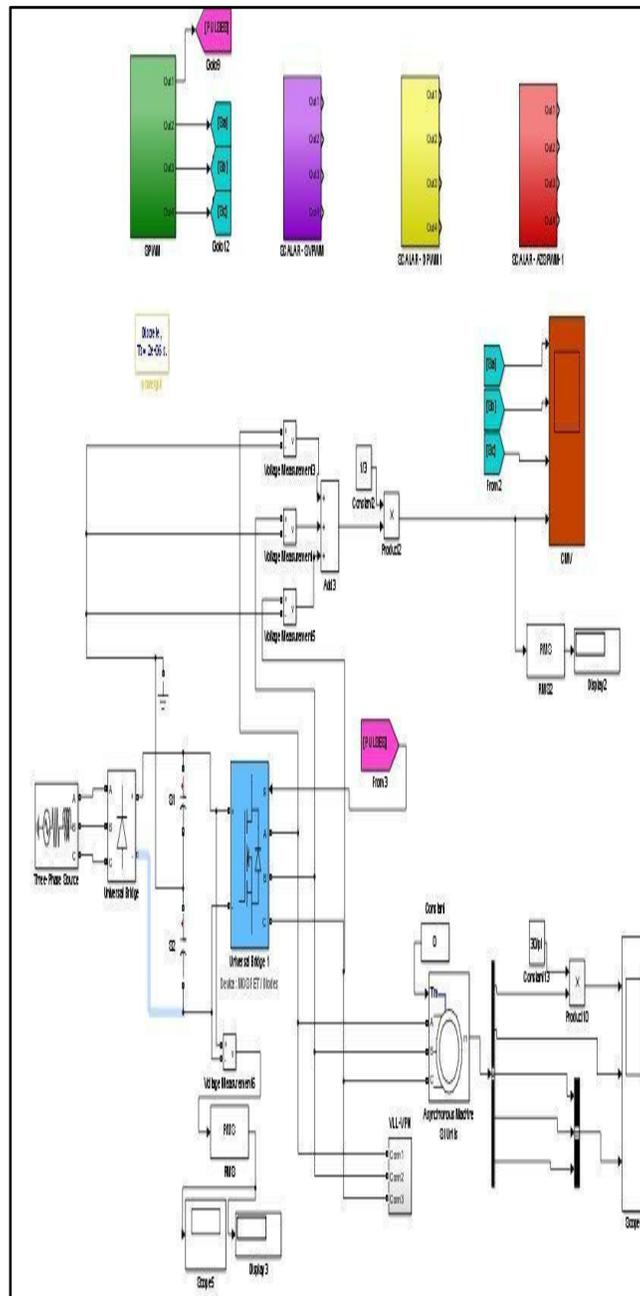
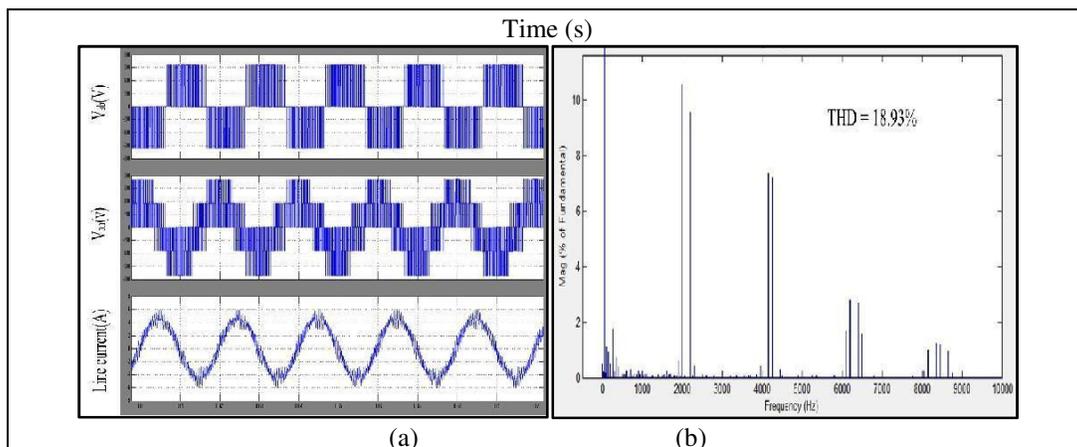


Figure 8: Simulink model of inverter fed induction motor drive with various PWM techniques



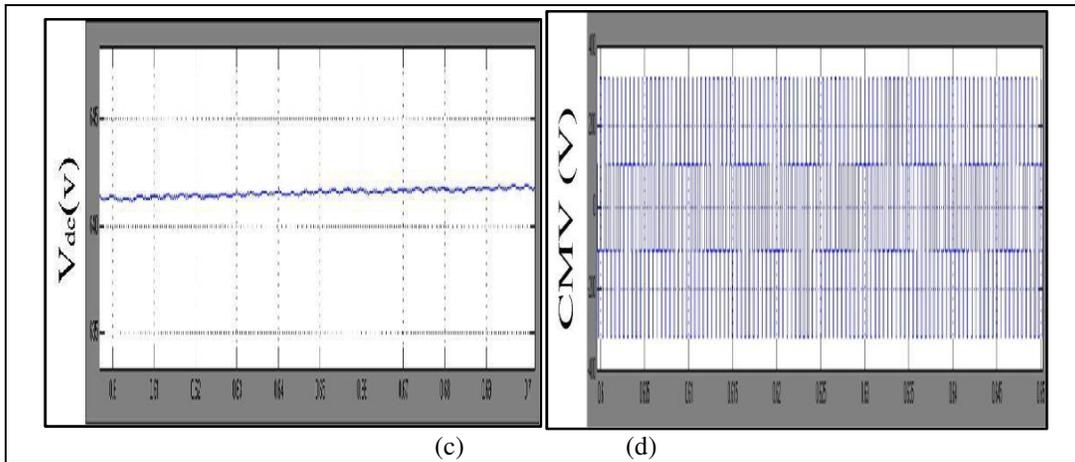


Figure 9: (a) steady state plots for SPWM algorithm based induction motor drive. (b) Harmonic spectra of line current (c) DC voltage. (d) CMV variations

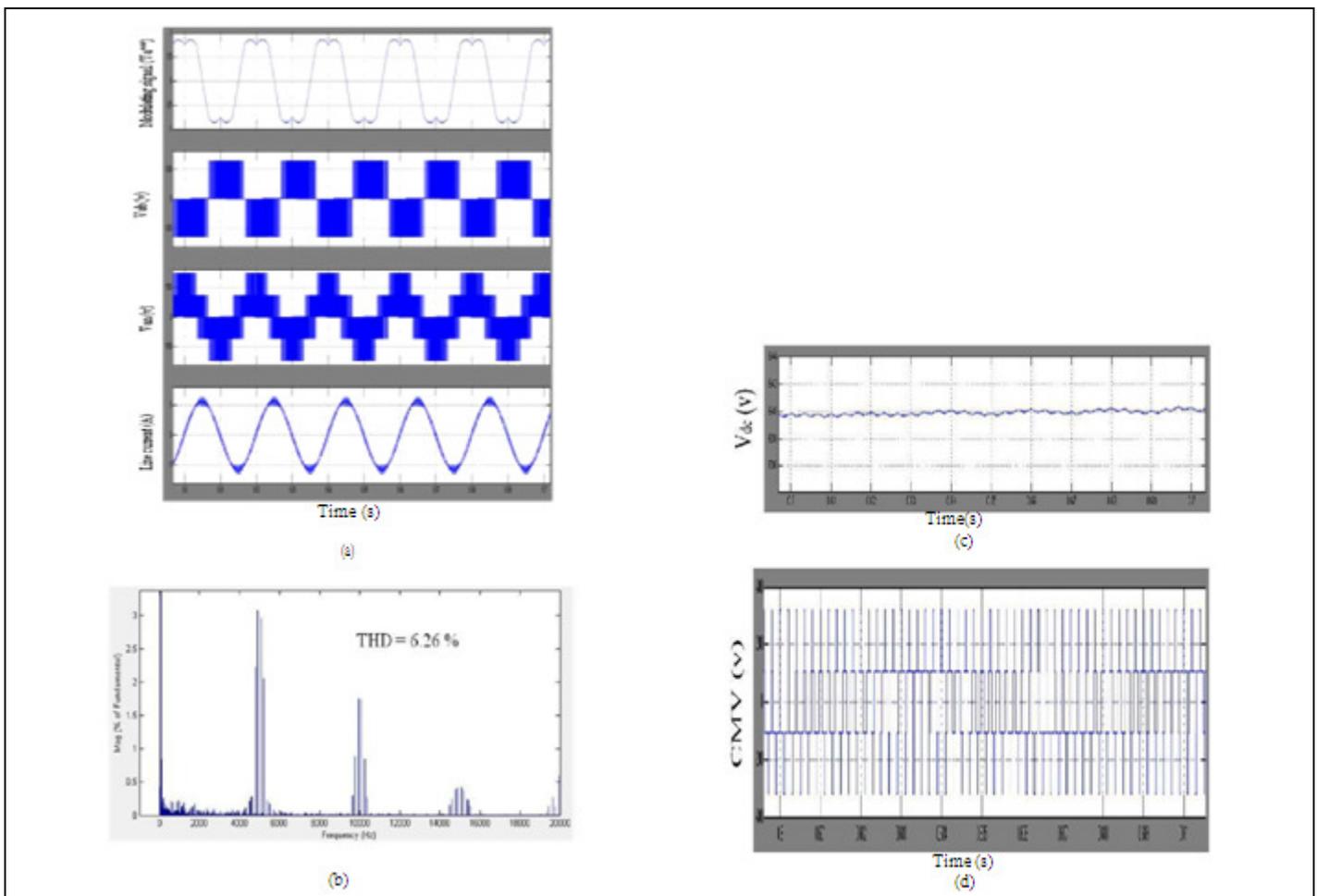


Figure 10: (a) steady state plots for SVPWM algorithm based induction motor drive. (b) Harmonic spectra of line current (c) DC voltage. (d) CMV variations

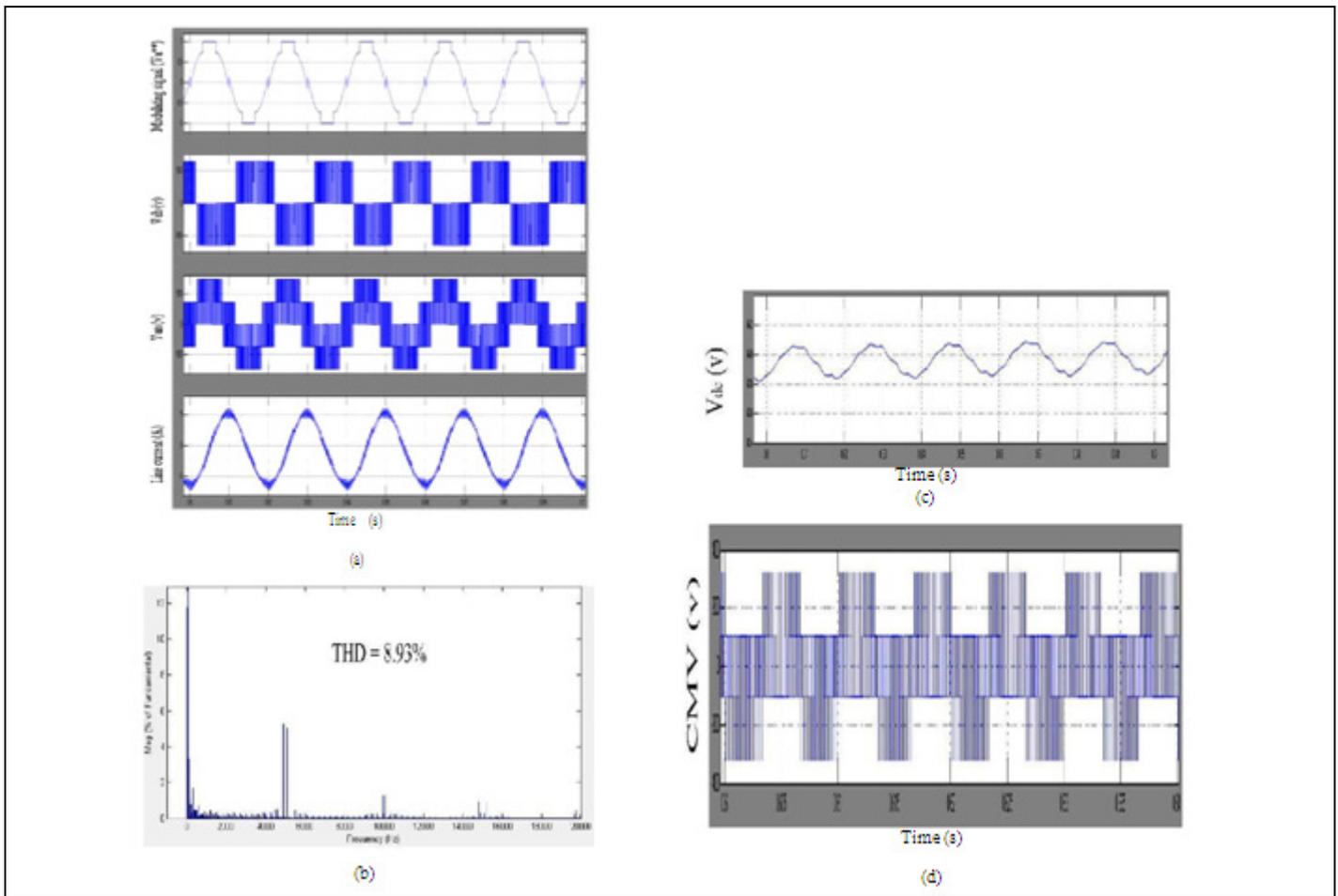


Figure 11: (a) steady state plots for DPWM1 algorithm based induction motor drive. (b) Harmonic spectra of line current (c) DC voltage (d) CMV variations

reduce the complexity of the PWM algorithm, a simplified scalar based approach has been presented in this paper. To evaluate the performance of the proposed approach based PWM algorithms, simulation studies have been carried out and results have been carried out and results were presented.

From the results it can be observed that the SVPWM and DPWM algorithm gives large common mode voltage variations between $\pm V_{dc}/2$. But, the proposed AZSPWM algorithm gives the reduced CMV variations between $\pm V_{dc}/6$. Moreover, it can be observed that the proposed AZSPWM algorithm give opposite pulses in line to line voltages, which causes the increased harmonic distortion in the line current.

	SPWM	SVPWM	DPWM	AZSPWM
Voltage Linearity	0 – 0.78	0 – 0.91	0 – 0.91	0 - 0.91
CMV	HIGH	HIGH	MODERATE	LOW
THD	18.93%	6.26%	8.93%	10.21%

Table 3: Performance Comparision of Various Pwm Methods

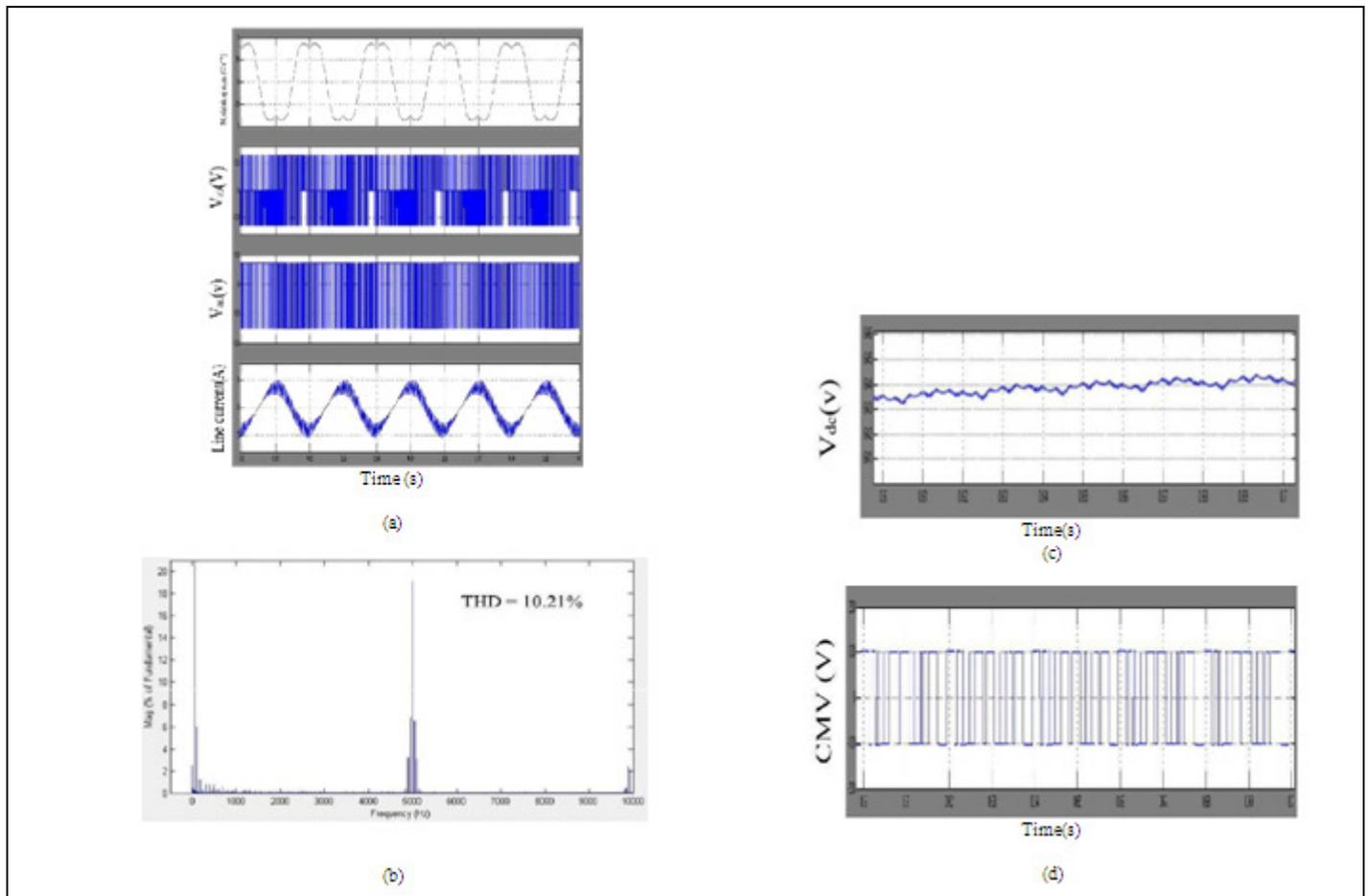


Figure 12: (a) steady state plots for AZSPWM algorithm based induction motor drive.
 (b) Harmonic spectra of line current (c) DC voltage (d) CMV variations

6. Conclusion

The classical SVPWM, DPWM and AZSPWM require the calculation of angle and sector calculation. This increases the complexity of the PWM algorithm. Hence, to

7. References

- i. H. V. D. Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," in Conf. Rec. IEEE IAS Annu. Meeting, 1986, pp. 244–251.
- ii. A.M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," IEEE Trans. Power Electron., vol. 14, no. 1, pp. 49–61, Jan. 1999.
- iii. P. Ram Mohan, T. Bramhananda Reddy, and M. Vijaya Kumar, "Simple and efficient high-performance PWM algorithm for induction motor drives" Journal of Electrical Engineering, vol. 11, edition.4. pp. 23-30.2011.
- iv. N.O. Çetin and A.M. Hava, "Scalar PWM Implementation
- v. Methods for Three-phase Three-wire Inverters," ELECO 2009, 6th International Conference on Electrical and Electronics Engineering, 5-8 November 2009, Bursa, Turkey, pp. 447-451.
- vi. Devisree Sasi and Jisha Kuruvilla. P "Modelling and Simulation of SVPWM Inverter fed PMBLDC motor Drive", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 5, May 2013.
- vii. B.K. Bose, "Modern Power Electronics and AC Drives".
- viii. Jayant M. Parkhi, R.K. Dhattrak, "Reduction of Common Mode Voltage in Ac drives Using Multilevel Inverter", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 3, Issue 4, Aug 2013, pp. 212-218.