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Implementation of Low Power and Area Efficient Novel Interleaver for WLAN Applications

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Abstract:
Wireless communication is one of the most important research area in communication field. WLAN and WiMAX are emerging standards for wireless broadband communication system. Orthogonal Frequency Division Multiplexing (OFDM) is used to speed up data transfer and to reduce adverse effects such as inter symbol interference(ISM) and Inter Channel Interference (ICI) is used in OFDM. An Interleaver is based on finite state machine (FSM) for modeling multimode addressable generator. The proposed method works for all code rates and modulation techniques used in IEEE.802.16e. As per the IEEE.802.16e standard the interleaver can be performed by 2 permutation steps. But the implementation becomes difficult because of floor function. The proposed method works with minimum loss of logic cells and flips flops compared to existing approaches.

Keywords: *WiMAX, address generator, OFDM, ICI, FSM, ISI*

1. Introduction

Gradual increase in use of internet has dragged the quest of broadband wireless access (BWA). BWA has been emerged as the last mile access solution and challenging competitor to the 3G technology [1]. Its popularity has been increased as it provides alternating solution to digital subscriber line (DSL). BWA systems have evolved as the solution for the persistent demand of these multimedia services. It provides enhancement in multimedia data services and quality of service. It supports simultaneous voice, data and multimedia services to a large group of subscribers without the need for DSL or cable modem. High processing speed, flexibility, turnaround time (TAT) are the basic requirements of broadband wireless access. These requirements make the designers to choose reconfigurable hardware platform like field programmable gate array (FPGA).

WiMAX is an emerging industry consortium standard for wireless broadband networking. It is based on wireless metropolitan area networking (WMAN) standards. It offers a rich set of features with flexibility in terms of deployment options and potential service offerings. The WiMAX physical layer is based on orthogonal frequency division multiplexing, which offers good resistance to multipath and allows WiMAX to operate in Non Line of Site (NLOS). WLANs are used to connect wireless users to a fixed LAN in corporate environments.

A major WLAN application will be in the public sector where WLAN can be used to connect a user to the backbone network. Airports, hotels, high-rising offices, city centres will be the target area for such public WLAN usage. It is becoming evident that WLANs will play a greater role in future. A popular vision of future generations of telecommunications systems suggests that it will be an amalgamation of high data-rate wireless wide area networks and newly standardized WLANs. However systems of the near future will require WLANs with data rate of greater than 100 Mbps. Standards mentioned can be implemented efficiently in FPGA**.** A product such as WiMAX implemented on FPGA can easily be upgraded by making necessary changes in the Hardware Description Language (HDL) code. In addition, the TAT of FPGA based circuit is much shorter compared to Application Specific Integrated Circuit (ASIC).

The main function of a communication system is to transmit information from source to destination with sufficient reliability. The error correction codes (ECC) play a very important role in modern digital communication systems. Interleaving is a technique that can be used in digital communications systems to enhance the error correcting capabilities of block codes. Interleaving is an important and powerful technique to combat burst of errors for FEC coded signal. This technique is traditionally used to reduce the bit error rate (BER) of digital transmission over a burst channel. The Interleaver subsystem rearranges the encoded symbols over multiple code blocks. This effectively spreads out long burst noise sequences so they appear to the decoder as independent random symbol errors which are manageable burst errors.

2. System Description

IEEE 802.16e based WiMAX physical layer is described in Figure.1. In this system, the input binary data stream obtained from source is randomized in order to prevent a long run of 1s and 0s, which causes timing recovery problem at the receiver. Pseudo random binary sequence is being used in which randomization is done by modulo 2 addition of the data with the output of the PBRS itself. The randomized data bits are thereafter encoded using Reed Solomon encoder followed by convolutional encoder. In conventional block Interleaver bits received from the encoder are stored row wise in the Interleaver memory. The moment the memory is completely filled, the bits are read column by column manner. After that interleaving data comes to map-per block in which modulation takes place. The resulting data symbols are used to construct OFDM symbols by inverse Fourier transform (IFFT). Cyclic prefix is used to reduce ISI.

In the receiver side inverse blocks are applied which perform DFT, de-mapping, de-interleaving, decoding and derandomization operations respectively to get the original data sequence.

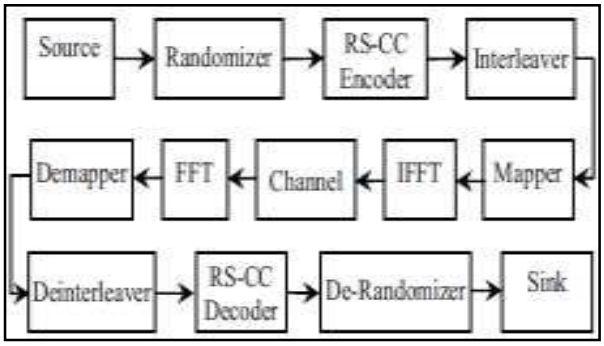

Figure 1: WiMAX physical layer[1]

3. Related Work

Khater et al. [6] In this paper, have implemented and evaluated a novel design for the hardware of the multi-mode Interleaver block used in the OFDMA mode of the IEEE 802.16e standard.

Upadhyayal et al. [8] in this paper an efficient technique that utilizes embedded shift register in Interleaver to model convolutional Interleaver using a hardware description language**.** It required more Interleaver word length and delay.

Eric Tell et al. [9] suggest architecture for a multi-mode block Interleaver that is suitable for the IEEE 802.11a and 802.11g standards. The proposed implementation is based on a special matrix memory to which data is written as rows but read out as columns.

Sghaier et al. [10] have described a look up table based method for address generation of the Interleaver used in IEEE 802.11eWLAN by designing a ROM from single port distributed RAM using VHDL.

R van nee et al. [11] in this paper described that in address generator RAM-1 at the beginning receives the read address and RAM-2 gets the write address with write enable signal of RAM-2 active. After a particular memory block is read / written up to the desired location, the status of select changes and the operation is reversed.

I S Misra et al. [8] in this paper efficient technique is proposed to design a finite state machine based WiMAX multimode Interleaver using hardware description language and hardware model implemented on FPGA.

4. Proposed Method

In WiMAX the block Interleaver used has different interleaving pattern for different code rates and modulation schemes [1]. Various Interleaver depths are required to incorporate various code rates and modulation schemes. The first step is to ensure that the adjacent coded bits are mapped onto nonadjacent sub carriers, which provides frequency diversity and improves the performance of the decoder. Adjacent coded bits are alternately mapped to less and more significant bits of the modulation constellation to avoid long run of lowly reliable bits.

Ncbps (Number of coded bits per sub-channel) defines the block size corresponding to the number of coded bits per allocated sub-channels per OFDM, d represents number of columns of the block Interleaver which is chosen to be 16 for WiMAX. mk is the output after the first level of permutation and k varies from 0 to Ncbps -1. jk is the output after second level of permutation. s is defined as s=Ncpc/2, where Ncpc is the number of coded bits per sub-carrier. (1, 2, 4 or 6 for BPSK, QPSK, 16-QAM or 64-QAM respectively [2]). The Interleaving is done with first and second level of permutation using the equations below.

$$mk = \left(\frac{Nbps}{d}\right) * (k\%d) \lfloor k/d \rfloor \quad \ldots\ldots\ldots\ldots\ldots (1)$$

$$jk = s * \lfloor mk/s \rfloor + (mk + Ncbps - \lfloor (d * mk)/Ncbps \rfloor \% s \quad \ldots\ldots\ldots\ldots\ldots (2)$$

Where % and $\lfloor \quad \rfloor$ signify modulo and floor functions respectively.

The hardware model of OFDM based WLAN Interleaver consists of two sections: address generator and Interleaver memory as shown in Figure. 2. The address generator is basically the simultaneous implementation of (1) and (2) which is the write address along with provision for generation of read address for Interleaver memory. Block Interleaver uses two memory blocks out of which one memory block is written and the other is read based on the value of select (sel) signal.

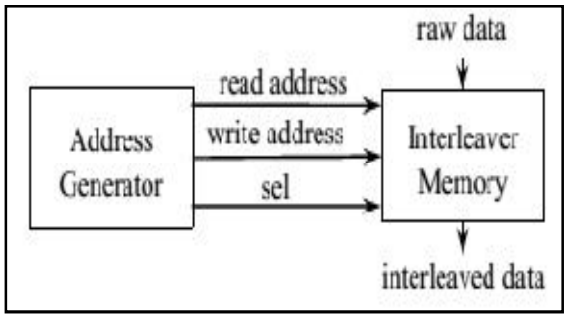

Figure 2: WiMAX physical layer [2]

4.1. Address Generator

Table I lists first 32 write addresses of the Interleaver for all four modulation types obtained by evaluating (1) and (2). Careful examination of the write addresses reveals that the subsequent addresses are not equally spaced for all the cases. Within a particular modulation scheme, the increment values follow a fixed type of pattern. In case of BPSK and QPSK (with s = 1) the increments are linear, having value 3 and 6 respectively. 16-QAM and 64-QAM have nonlinear increments, e.g. 13, 11 and 20, 17, 17 respectively.

Ncbps=48	0	3	6	9	12	15	18	21
BPSK	24	27	30	33	36	39	42	45
code rate=1/2	1	4	7	10	13	16	19	22
	25	28	31	34	37	40	43	46
Ncps=96	0	6	12	18	24	30	36	42
QPSK	48	54	60	66	72	78	84	90
code rate=1/2	1	7	13	19	25	31	37	43
	49	55	61	67	73	79	85	91
Ncps=192	0	13	24	37	48	61	72	85
16-QAM	96	109	120	133	144	157	168	181
code rae=1/2	1	12	25	36	49	60	73	84
	97	108	121	132	145	156	169	180
Ncps=48	0	20	37	54	74	91	108	128
64-QAM	145	162	182	199	216	236	253	270
Code rate=1/2	1	18	38	55	72	92	109	126
	146	163	180	200	217	234	254	271

Table 1: 32 bit Address generation of different modulation schemes and Interleaver depths and code rates [3]

Modulation	Mod type	Code Rate	Interleaver depth	ID	Increment value	Spaced equally
BPSK	00	½	48			y
QPSK	01	½	96	000		Y
		¾	144	001		Y
		½	192	010		Y
		½	288	011		Y
		½	384	100		Y
		¾	432	101		Y
		½	480	110		Y
		½	576	111		y
16-QAM	10	½	192	000		n
		¾	288	001		n
		½	384	010		n
		½	576	011		n
64-QAM	11	½	288	X00		n
		2/3	384	X01		n
		¾	432	X10		n
		½	576	X11		n

Table 2: Increment values of addresses of various modulation Scheme and the interleaver depth

In Table II the spacing between the generated written addresses of various interleaving depth have been shown The address generation block is described in the figure.3. It permits all the code rates and modulation scheme used in IEEE802.16e. It is a combination of bulk of circuitry. In the first level generation 8 muxes are used to implement unequal increment of addresses used in 16-QAM and 64-QAM modulations. The selection is controlled by T-flip-flop and MOD-3 counter for four muxes of 16-QAM and last four muxs of 64-QAM respectively. In level two the top most mux contains eight input lines each of seven bits with equal increment of address of

different Interleaver depth. The input to the second and third muxs in level 2 is from the first level muxes outputs of 16-QAM and 64-QAM respectively. The level third contains one of the increment values from each mux of the level 2 and increment address of BPSK signal. Second level is controlled by 3 bit selection line, connected all the three muxs. 7-bit output from the third level mux acts as one of the inputs to the 10-bit adder after zero padding. The other input of the adder is from accumulator which holds the previous address. In the existing system the adder is carry save adder after addition a new address is written in the accumulator. The read addresses are generated using 10-bit up counter. The counter is reset when it reaches the terminal count for the desired modulation scheme.

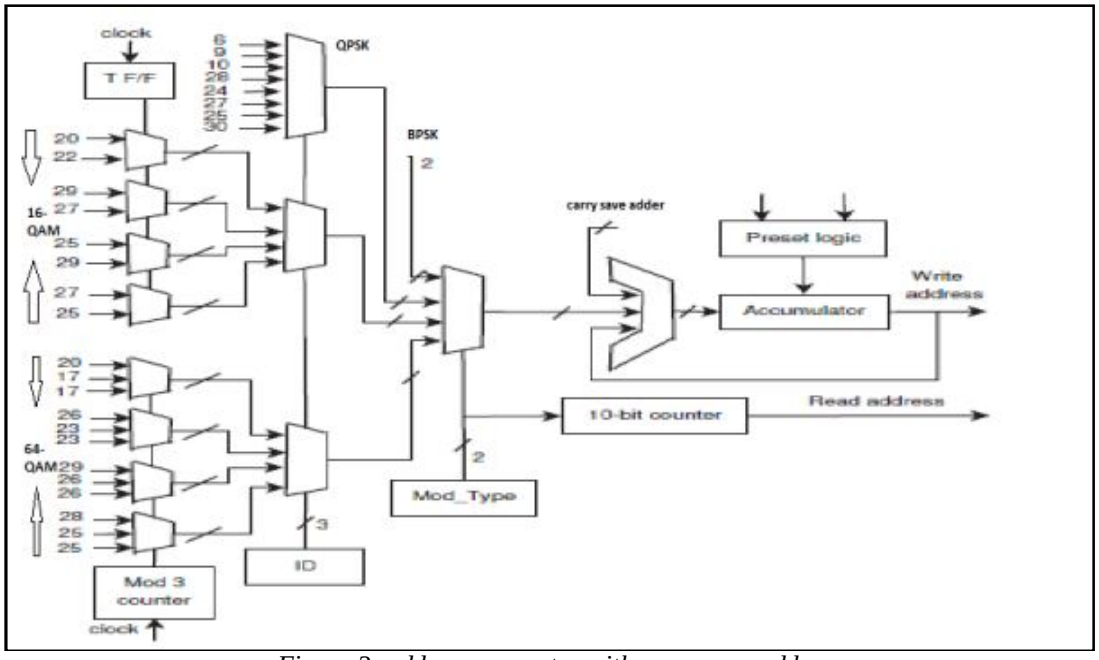

Figure 3: adderss generator with carry save adder

In the proposed address generator Figure 4 the carry select adder reduces area and power as compared with the carry save adder. Carry select adder improves the performance of the proposed designs in terms of delay, area, power and their products.

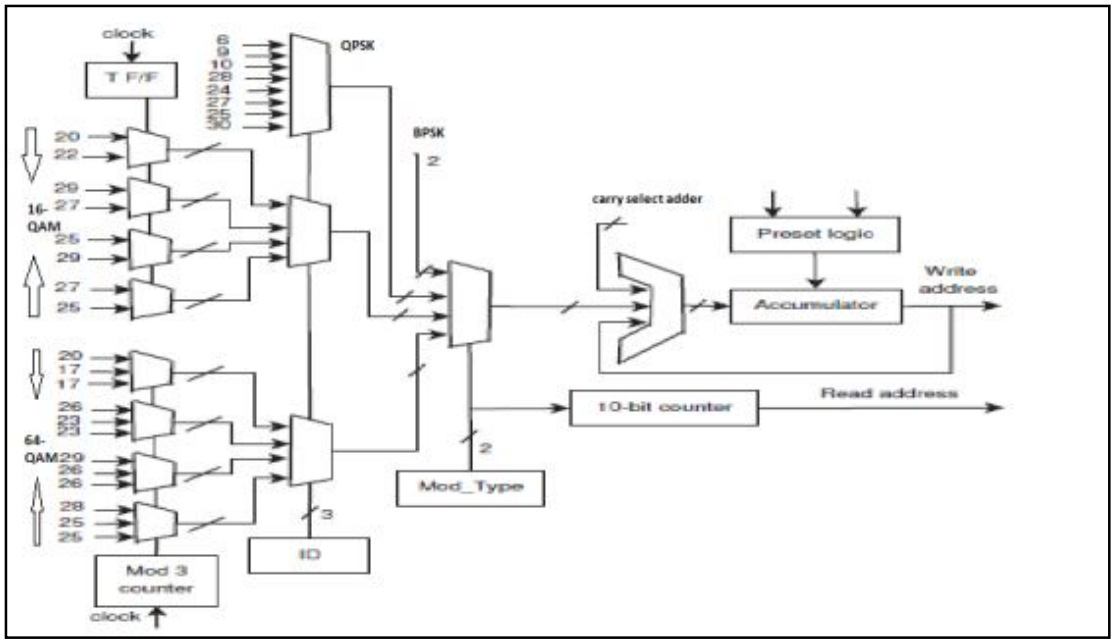

Figure 4: Address generator with carry select adder

4.2. Preset Logic as Finite State Machine (FSM)

It is basically a hierarchical FSM. This block contains a 4-bit binary counter and it keeps the track of end of states during every iteration. The FSM enters into the first state with CLR=1. Based on the value of modulation type (00, 00, 10 and 11) it makes

transition to one of the next level states such as for QPSK 0 to 7, for 16-QAM and 64-QAM 0 to 3 respectively as shown in Figure.5. The different states signify one of the Interleaver depths.

From these states it switches to next level of states based on the values of interleaving depth. When FSM finishes the terminal value of first iteration, this is 90 for BPSK; it loads the accumulator with the initial value of one for next iteration. After completing first iteration of the 16 addresses it will go to clr state. The process is repeating until the next modulation scheme of different Interleaver depth is encountered. Pre-set logic is controlled by clear and pre-set state.

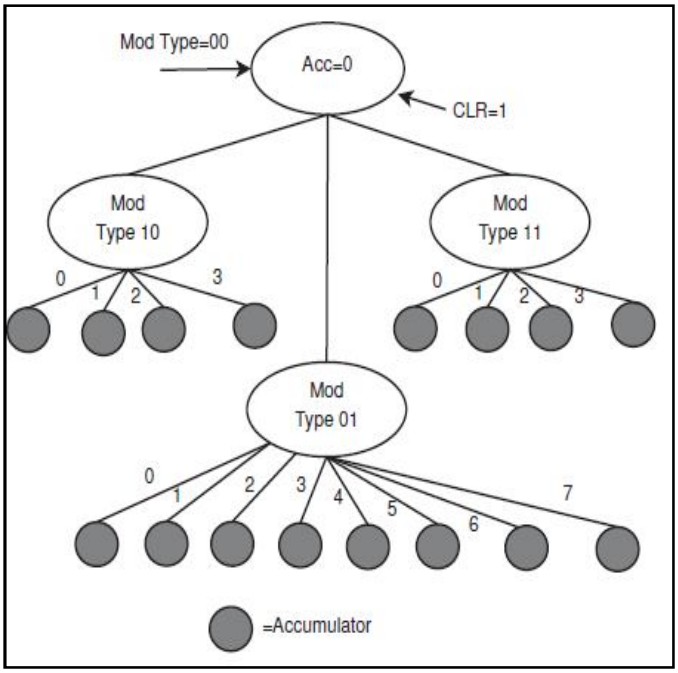

Figure 5: FSM with clr=1[1]

4.3. Interleaver Memory Block

The Interleaver memory block comprises of two memory modules (RAM-1 and RAM-2), three muxs and an inverter as shown in Figure. 6. In block interleaving when one memory block is being written the other one is read and vice-versa. Each memory module receives either write address or read address with the help of the mux connected to their address inputs (A) and sel line. RAM-1 at the beginning receives the read address and RAM-2 gets the write address with write enable (WE) signal of RAM-2 active. After a particular memory block is read or written up to the desired location, the status of sel changes and the operation is reversed. The mux at the output of the memory modules routes the interleaved data stream from the read memory block to the output.

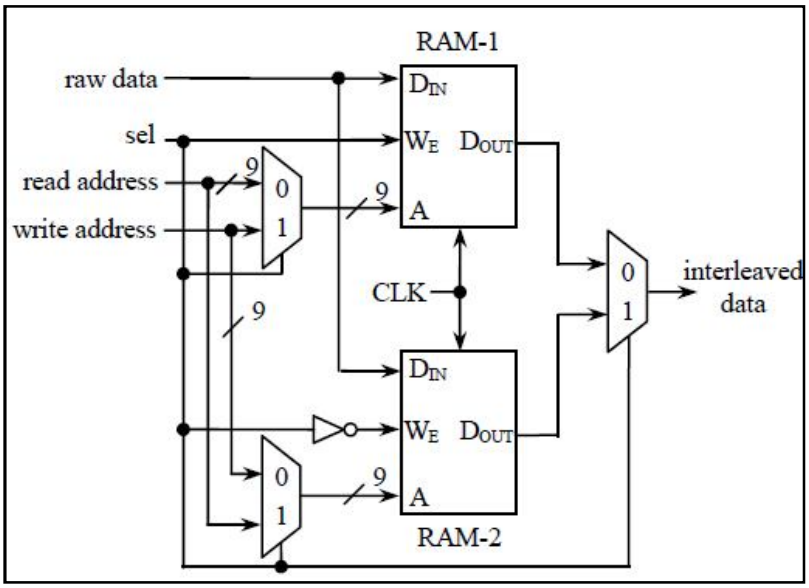

Figure 6: Interleaver memory block[1]

5. Result and Analysis

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	121	5472	1%
Number of Slice Flip Flops	35	10944	0%
Number of 4 input LUTs	185	10944	1%
Number of bonded IOBs	23	240	9%
Number of FIFO16/RAMB16s	2	36	5%
Number of GCLKs	1	32	3%

Table 3: Device utilization for existing system

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	91	5472	1%
Number of Slice Flip Flops	29	10944	0%
Number of 4 input LUTs	175	10944	1%
Number of bonded IOBs	23	240	9%
Number of FIFO16/RAMB16s	2	36	5%
Number of GCLKs	1	32	3%

Table 4: device utilization for proposed system

From the Table 3 and 4 device utilization of the proposed system uses minimum no slices, FFs, LUTs, IOBs, so area and power of the proposed system is reduced.

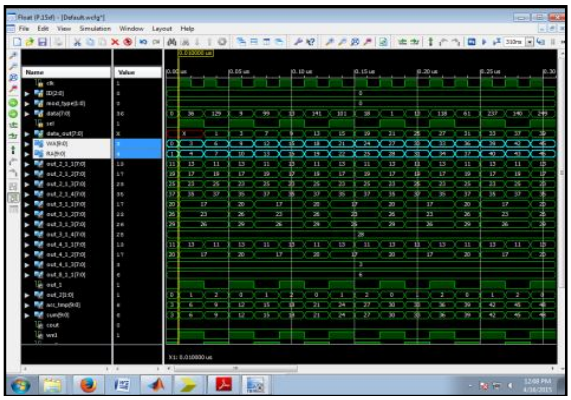

Figure 7: Simulation results for BPSK modtype-00

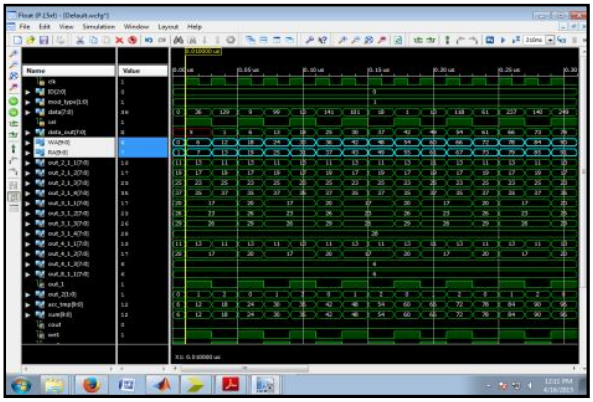

Figure 8: Simulation results for QPSK modtype-01

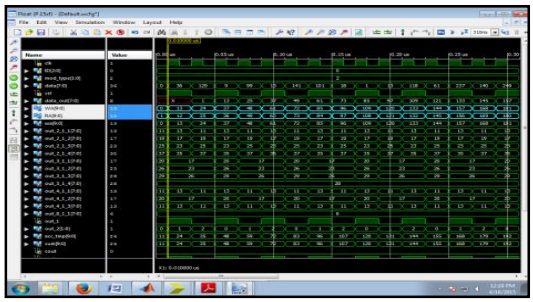

Figure 9: Simulation results for 16-QAM modtype-10

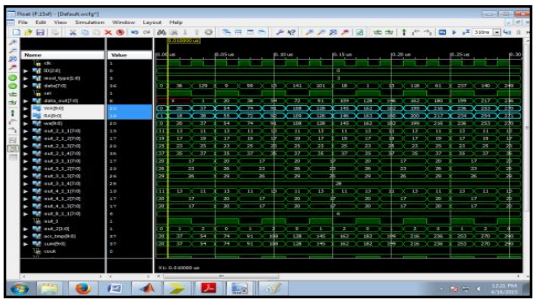

Figure 10: Simulation results for 64-QAM modtype-10

Simulation results of the proposed Interleaver for OFDM based WLAN is presented in the form of timing diagram in Figure. 7. It is obtained using Xilinx 14.7. In Table 4, BPSK modulation scheme (mod_typ=00) has been shown. It shows the increment values of read and write address similarly in the figure 8, 9 and 10 for QPSK (mod_type=01), 16-QAM (mod_type=10) and 64-QAM (modtype=11) have been shown.

6. Conclusion

Interleaver with efficient address generator is implemented, with satisfies all code rates and modulations schemes used in IEEE.802.16e. In the address generator block the carry save adder and the carry select adder is used and compare the results of both the adders. Address generator with carry select adder will consumes low power and area. Xilinx 14.7 is used to generate the address generator. The number of logic cells has got reduced. It helps in reduction in area consumed in the carry select adder compare to carry save adder. It also provides the reconfigurable solution for development of WiMAX.

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