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Implementation of High Throughput and Reduced Complexity LDPC Decoder using Message Passing Algorithm

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Abstract:
In LDPC codes there is a tradeoff between decoder performance and decoder complexity. In order to overcome this problem a message passing algorithm for decoding LDPC codes is proposed in this paper. This algorithm is based on both hard and soft decision decoding techniques. The proposed algorithm for LDPC decoder has been implemented and tested on Xilinx vertex 5 FPGA, this implemented decoder can achieve a throughput of 23.2Gbps and also reduces the decoder complexity such as hardware resources.

Keywords: *LLR, SPA, BFA, FPGA*

1. Introduction

The Low density parity check codes were first invented by Gallager in 1962.They were not popular for a few decades since its introduction due to the tradeoff between high implementation complexity and decoding performance. However, they gain popularity after it was formally reintroduced by Mackay and Neal in 1997. LDPC codes have emerged as one of the most popular forward error correcting technique that can achieve a bit error rate performance close to the Shannon limit. LDPC codes belong to the class of block codes, they are represented by sparse parity check matrix H, which consists of very small no of non- zero elements. LDPC codes have several advantages over turbo codes such as better bit error rate performance, low signal to noise ratio, reduced implementation complexity and inherent code structure that supports a high degree of parallelism and flexibility for designing a LDPC decoder for various applications. LDPC forward error correction codes have gained a wide popularity and acceptance among the modern wireless communication systems such as WLAN WiMAX and digital video broadcasting-second Generation (DVB-S2).

Several algorithms with varying complexity and performance have been proposed for LDPC decoding, but achieving a balanced trade-off between decoding performance (such as throughput and BER) and implementation complexity still remains a potential problem.

The sum, product algorithm is based on soft decision decoding achieves best decoding performance but with high complexity. Bit flip algorithm is based on the hard decision decoding it has less complexity, but suffer from poor decoding performance. To overcome this problems, low complexity LDPC decoding algorithm is proposed to achieve a tradeoff between decoding performance compared to fully hard decision algorithm and less implementation complexity compared to fully soft decision algorithm. This algorithm involves the simple hard decision message passing technique at check nodes and variable node involves the soft inputs and performs the distinct operations to improve the decoding performance. The algorithm has been implemented on FPGA and the LDPC decoder performance is analyzed.

The remaining paper is organized as follows. The overview of LDPC codes is discussed in section II. The section III describes the proposed algorithm followed by the experimental results in section IV. Finally, Section V includes the conclusion of the paper.

2. Overview of LDPC Codes

LDPC codes belong to the class of block codes, they are represented by parity check matrix (PCM) H, it is a sparse matrix, it consists of very few number of non -zero elements.

The sparseness of PCM determines the decoding complexity and the minimum distance of the code. LDPC matrix is described by various parameters which are briefly described here. An encoded message is known as codeword consists of the useful information bits and redundant bits. The code rate is the ratio of length of the useful information bits and length of the codeword bits. Depending upon the code rate value the redundant bits are added to the information bits. The number of non-zero elements in each row and column is collectively known as degree of distribution. If the degree of distribution in each row and column is same means, then the matrix is said to be regular matrix, otherwise it is an irregular matrix an example of irregular matrix is as shown in figure (1).

$$H = \begin{bmatrix} 1&0&0&1&0&0&0&0&0&0&0&0 \\ 1&0&0&1&1&0&0&0&0&0&0&0 \\ 0&1&0&0&1&1&0&0&0&0&0&0 \\ 0&0&1&0&0&1&1&0&0&0&0&0 \\ 0&0&1&0&0&0&1&1&0&0&0&0 \\ 0&1&0&0&0&0&0&1&1&0&0&0 \\ 1&0&0&0&0&0&0&0&1&1&0&0 \\ 0&1&0&0&0&0&0&0&0&1&1&0 \\ 0&0&1&0&0&0&0&0&0&0&1&1 \end{bmatrix}$$

Figure 1: A length 12 rate ¼ irregular LDPC matrix

The H matrix can be represented graphically by using Tanner graph. A regular (2,3) parity check matrix with 9-bit code length is shown in figure 2 (a) and the corresponding Tanner graph representation of the parity check matrix H is shown in figure 2(b).

$$H = \begin{bmatrix} 1&0&0&1&0&0&1&0&0 \\ 0&1&0&0&1&0&0&1&0 \\ 0&0&1&0&0&1&0&0&1 \\ 1&0&1&0&0&0&0&1&0 \\ 0&1&0&1&0&0&0&0&1 \\ 0&0&0&0&1&1&1&0&0 \end{bmatrix}$$

Figure 2(a): A length 9 bit rate 2/3 regular LDPC matrix

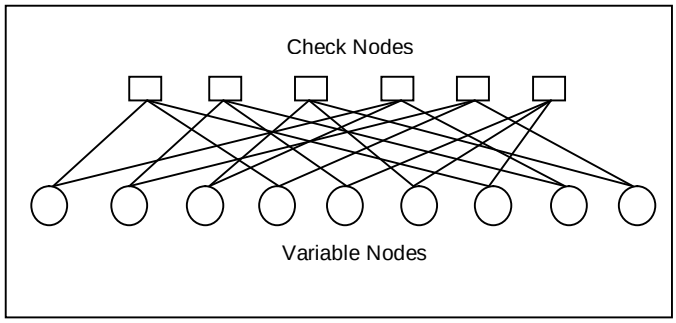

Figure 2(b): Tanner graph representation of LDPC matrix

The decoding of LDPC codes involves the passing of messages between variable nodes and the check nodes along the connected edges in the tanner graph. Each of the nodes in the tanner graph is works in isolation with the information available on the connected edges only. This class of decoding algorithms is called as message passing algorithm. This decoding algorithm involves the passing of the messages between the nodes for a fixed number of iterations or till the parity is satisfied. Hence such algorithm is often called as iterative algorithms.

3. LDPC Decoding Algorithms

The BFA has low implementation complexity, but poor performance and SPA has high implementation complexity but it can achieve good decoding performance. The main aim of the proposed decoding algorithm is to achieve a trade of between the implementation complexity and decoding performance of the above two algorithms. The check node and variable node operations of the proposed MPA are presented next.

3.1.Check-Node operation

The complexity of message passing algorithm is depends upon the length of the extrinsic message and check node operation. These aspects are particularly important in case of hardware implementation of large LDPC codes. In order to reduce the complexity of MPA, the check node consists of a simple parity check operation (eq.1).

$$C_k = V_1 \oplus V_2 \bigoplus \ldots\ldots \oplus V_l \qquad \forall l \neq k \qquad (1)$$

Where l, k = 1, 2, ...degree of check node

3.2. Variable Node Operation

The variable node operation in message passing algorithm is based on the soft decision decoding, which requires LLR as a soft input. These LLRs are passed over to the variable node, this variable nodes (V) perform the sum operations on the input LLR's and computed messages are passed along the connected edges to check nodes (C). The variable node directly operates on the hard decision bit received from the check nodes. For example, at a variable node if binary '0' is received from the check node, it is added to the LLR value, if it's binary '1' means this will add to the LLR (eq.5). After this operation the updated LLR value is sent across to the respective connected check nodes for parity check as in equation (eq.6). The process is repeated until the parity check is satisfied or the maximum iteration is reached.

Initial (at iteration 0):

$$V_n = LLR_n \quad (2)$$

Subsequent iterations:

$$X_i = 0, \quad if \ C_i = 0 \quad (3)$$

$$X_i = 1, \quad if \ C_i = 1 \quad (4)$$

$$V_n = V_n + \sum X_i \quad (5)$$

$$V_i = sign(V_n - X_i) \quad (6)$$

Where n= 1,2, ...number of variable nodes

i= 1,2, ... degree of variable node

The structure of the variable node and check node for message passing algorithm is as shown in figure (3).

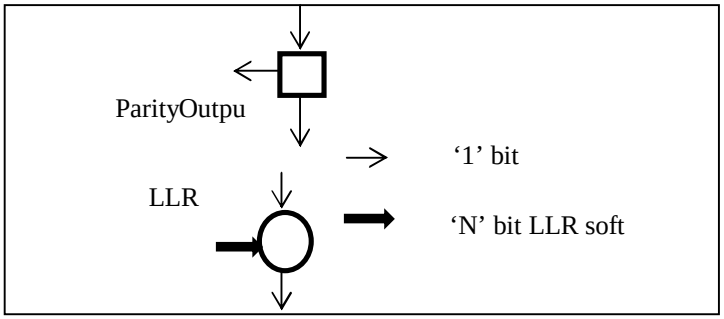

Figure 3: Decoding node structure

4. FPGA Implementation

4.1. Design procedure

A hardware model of the decoder is developed using the Verilog and synthesized using Xilinx synthesis tool. The block diagram of LDPC decoder as implemented is shown in figure 4.The decoder consists of a global 'Clock' and synchronous 'Reset' inputs. The maximum number of iterations is determined by the value applied at the 'Maxiter' input. The LLRs are applied at the 'Log_LikeHood_Ratio' input. After decoding process is completed the output is obtained at the 'Decod_Op'. The RTL schematic of LDPC decoder, check node unit and variable node unit is as shown in figure 5-7.

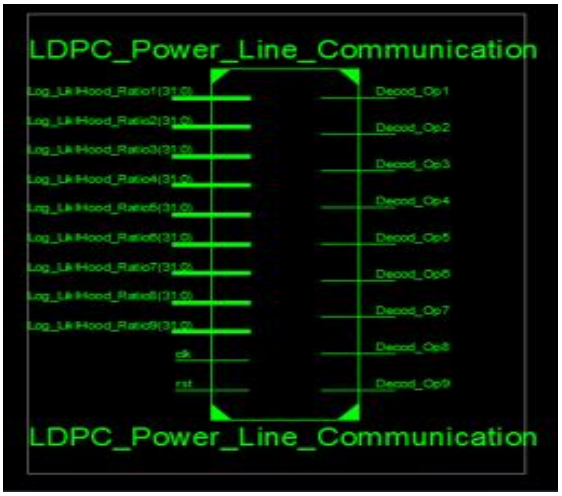

Figure 4: Block diagram of the designed LDPC decoder

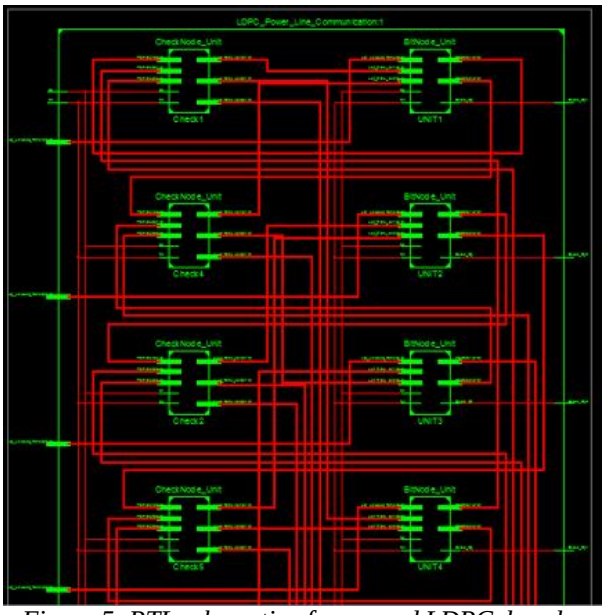

Figure 5: RTL schematic of proposed LDPC decoder

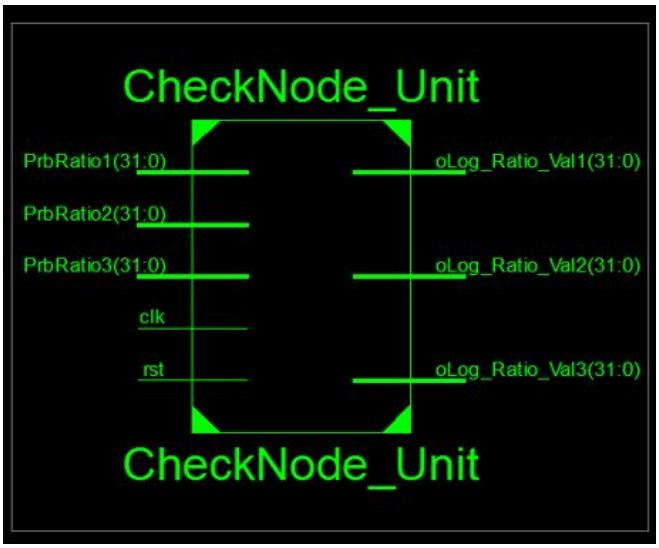

Figure 6: Check Node unit

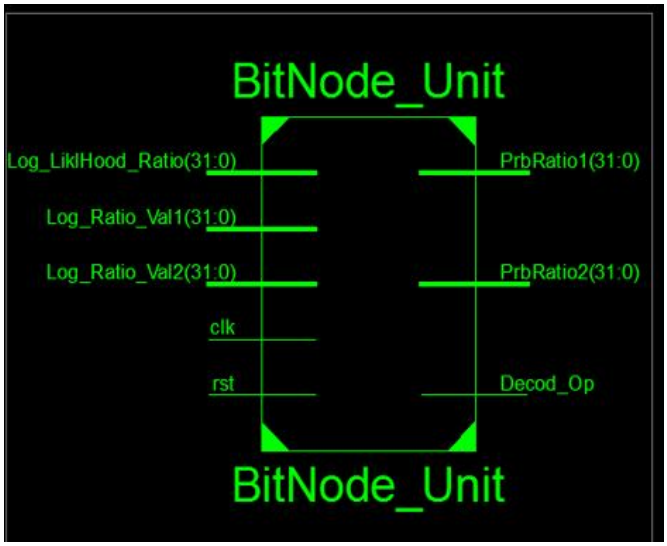

Figure 7: Variable Node unit

4.2. Implementation results

The LDPC decoder is implemented on a XILINX Vertex 5 FPGA (XC5VLX110T). Maximum iterations is set to 10, the simulation result is as shown in figure 8. The FPGA device utilization summary of the proposed message passing algorithm of LDPC decoder and comparison with the other sum product and bit flip algorithm of LDPC decoder is as shown in table 1.

Figure 8: Simulation results

Resources	MPA	SPA	BFA
Devices	Xilinx Vertex 5 (XC5VLX110T-3FF1136)		
LDPC Code	2/3 rate (2,3) regular code	½ rate (3,6) regular code	
Slices	9493	15684	1396
LUTs	31359	58787	3577
Registers	1641	12443	2069
Clock	48.323MHz	128MHz	190MHz

Table 1: FPGA Device utilization summary

The throughput of the LDPC decoder is calculated using the formula shown in equation (5)

$$T = \frac{\text{rate} \times \text{codelength} \times f_{max}}{N_{it} \times \theta}$$

Where f_{max} is the maximum operating frequency of the decoder obtained from FPGA implementation, N_{it} is the number of decoding iterations and θ is the number of clock cycles required to complete one iteration.

5. Conclusions

A message passing algorithm for LDPC decoding has been presented in this paper. High precision soft LLR inputs is used for variable node operation, hence it enhances the performance of decoder. The algorithm has been implemented on FPGA and the result shows that the requirements of hardware resources are less. The decoder achieves a throughput of ~23.2Gbps.

6. References

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