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Comparative Analysis of 1-Bit Full Adder Designs

Anjali Mann
Student, Department of ECE, Maharaja Surajmal Institute of Technology, New Delhi, India
Jitesh Chawla
Student, Department of ECE, Maharaja Surajmal Institute of Technology, New Delhi, India
Yashveer Singh
Student, Department of ECE, Maharaja Surajmal Institute of Technology, New Delhi, India
Geetanjali Sharma
Assistant Professor, Department of ECE, Maharaja Surajmal Institute of Technology, New Delhi, India

Abstract:
A full adder circuit is one of the basic building blocks of a digital design. In general, it is made by CMOS technology. In the CMOS technology the basic full adder is built by 42 transistors. So, the transistor count is very high. The average power consumption and delay are very high. The decrease in the transistor count reduces the average power, delay and noise. In this article, the comparison in terms of power consumption of different types of one bit full adders is considered. This paper discusses the evolution of full adder circuits in terms of lesser power consumption, higher speed. Starting with the most basic 42 transistor full adder and then gradually studied full adders consisting of as less as 10 transistors. For the purpose of comparative analysis of 1-bit different adder designs, 45nm technology is used with TANNER EDA tool.

Keywords: *Full adder, CMOS circuit, transmission gate, Hybrid PTL/CMOS*

1. Introduction

Today there are a growing number of portable applications requiring small-area low-power high-throughput circuitry. Therefore, circuits with low power utilization are to be the most important candidates for design of microprocessors and system mechanism. The battery technology does not advance at the same rate as the microelectronics technology and there is an imperfect quantity of power available for the mobile systems. The goal of extending the battery lifespan of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not essentially imply low energy. To execute an arithmetic operation, a circuit can be obtained through very low power by clocking at very low frequency, but it may take a very long time to complete the operation [1]. An adder is one of the most critical components of a processor which determines its throughput, and for address generation in case of memory or cache access. The full adder performance would affect the system as a whole. In this paper, we propose a comparative analysis of full adders implemented using various techniques. Power minimization is one of the primary concerns in today's VLSI design methodologies because of two reasons, one is the long battery operating life requirement of portable devices and second is due to the increasing number of transistors on a single chip leading to high power dissipation. In VLSI applications, 1-bit full adder cell is the fundamental gate used in many arithmetic circuits like adders and multipliers. Thus, increasing the performance of the full adder block leads to the enhancement of the overall system performance [3], [4]. A full adder has three input and two output blocks in which the outputs are the addition of three inputs. Basic fundamental units used in various circuits such as parity checkers, compressors and comparators are full adders [5].

Many logic styles have been used in past for designing the full adder circuits. Standard static CMOS full adder with pull up and pull-down networks used 42 transistors. Hybrid of CMOS and pass-transistor logic (PTL) with 30 transistors show better driving capability but consumes large power. Transmission gate CMOS adder (TGA) was based on transmission gates and used 20 transistors. Main disadvantage of TGA was that it requires double transistors that of pass transistor logic for implementations same logic function. A transmission function full adder (TFA) was based on transmission function theory and used 14 transistors. A full adder cell implemented using XOR design and multiplexer used 14 transistors with elimination of the direct path to power supply were reported.

The rest of the paper is organized as follows. Section II describes the truth table and equation. Section III elaborates the different types of full adder circuits. Section IV is followed by simulation result. Finally, section V concludes the work.

2. Truth Table and Equation

A one-bit full adder is a combinational circuit that performs the arithmetic sum of three bits. It consists of three inputs *a, b* and c_{in} and two outputs *S* and C_{out} [3] as illustrated in figure 1. The truth table of the full adder is listed in Table 1. Expressions for *S*

and C_{out} are given in Equation (2.1) and Equation (2.2)

$S = a \oplus b \oplus c_{in}$ 2.1

$C_{out} = a.b + b.c_{in} + c_{in}.a$ 2.2

a	b	c_{in}	$cout$	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1: 1-bit Full Adder Truth Table

3. Different Types of Full Adder Circuits

In this section, different types of full adder circuits are discussed.

3.1. Basic Full Adder Circuit using CMOS

The adder cell (Figure 1.) uses 42 transistors based on standard CMOS topology. Due to the high number of transistors, its power consumption is high. Large PMOS transistor in pull up network results in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was high noise margins and thus reliable operation at low voltages [6].

3.2. Basic Full Adder Circuit using Hybrid PTL/CMOS

The adder cell (Figure 1.) uses 30 transistors based on standard CMOS and Pass Transistor Logic.The EX-OR is implemented using PTL and the basic gates such as AND and OR are implemented using CMOS. The Hybrid of the two techniques results in decrease in area. Due to lesser number of transistors as compared to only CMOS logic, its power consumption and delay are less.

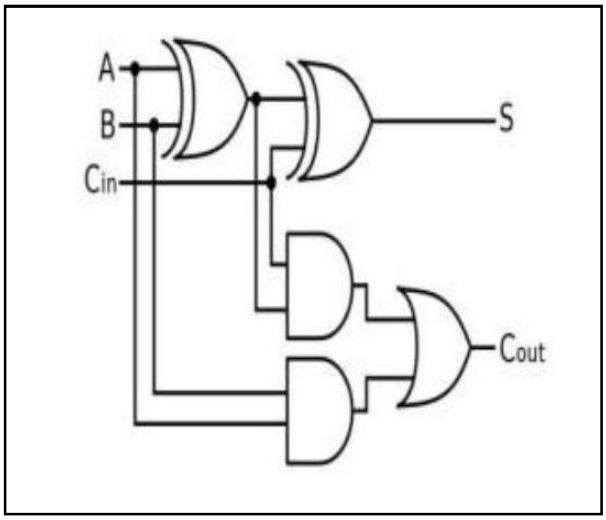

Figure 1: Basic Full Adder Circuit

3.3. NAND replacement Full Adder using CMOS [36T]

The basic gates of the basic full adder were replaced with NAND gate. This means, the AND and OR gates of basic full adder design were replaced with NAND gates (Figure 2.). This resulted in a reduced transistor count. Due to lesser number of transistors as compared to basic, full adder implementation using CMOS logic, its power consumption and delay are less.

3.4. NAND replacement Full Adder using Hybrid PTL/CMOS [24T]

The basic gates of the basic full adder were replaced with NAND gate. This means, the AND and OR gates of basic full adder design were replaced with NAND gates (Figure 2.). Since this resulted in a reduced transistor count, implementation using Hybrid PTL/CMOS resulted in even lesser transistors.

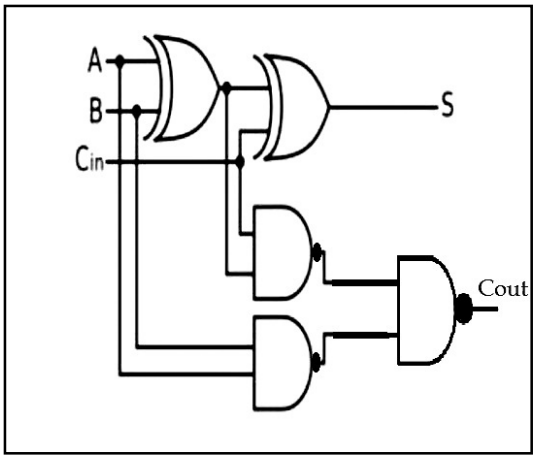

Figure 2: NAND replacement Full Adder

3.5. NAND Gate implementation of Full Adder using CMOS [36T]

The logic of full adder is implemented using NAND gates, which reduce the transistor count. (Figure 3.)

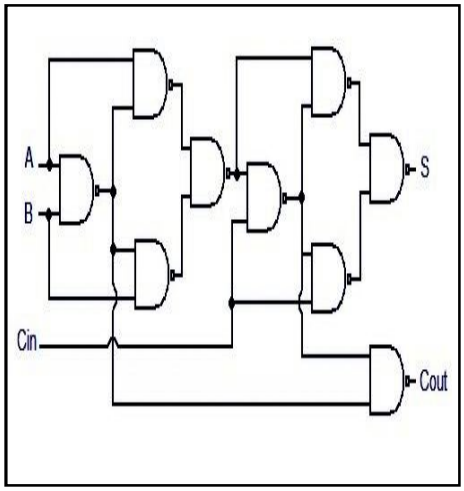

Figure 3: NAND implementation of Full Adder

3.6. NOR Gate implementation of Full Adder using CMOS [48T]

The logic of full adder is implemented using NOR gates, which reduces transistor count as seen in Figure 4.

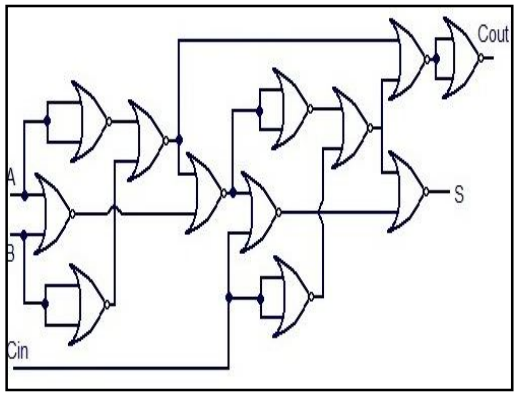

Figure 4: NOR implementation of Full Adder

3.7. Conventional CMOS Full Adder Circuit

The adder cell uses 28 transistors based on standard CMOS topology (Figure 5.). Due to lesser number of transistors as compared to basic, full adder design, its power consumption is less. The large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power. One of the most significant advantages of this full adder was high noise margins and thus reliable operation at low voltages.

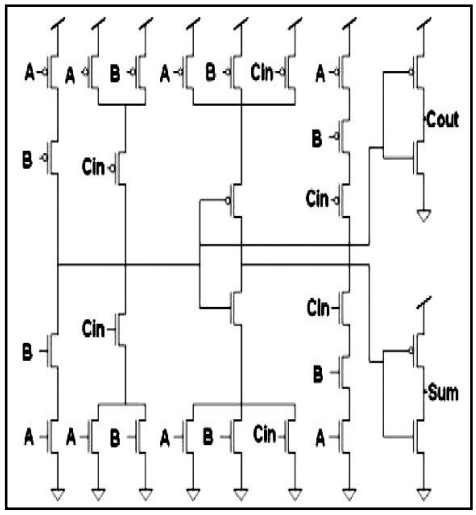

Figure 5: Conventional CMOS Full Adder

3.8. XOR-XOR and MUX using CMOS

The below circuit (Figure 6.) of full adder using 2 XOR gates and 1 multiplexer is implemented using Transmission Gate Logic which is made of 44 transistors. Though a large number of transistors as compared to all other circuits, but comparatively lesser power consumption than basic full adder using CMOS (Figure 1.).

3.9. XOR-XOR and MUX using CMOS and TG

An optimized design (Figure 6.) is highly desirable at the circuit level to avoid large power dissipation, large delay and to achieve sufficient output level. Here, an energy efficient single bit full adders with 18 transistors using 6T XOR gate, inverter and 4T 2:1 multiplexer blocks(TG style) have been presented., which shows better results in term of power consumed. There is a decrease in delay and thus decrease in power delay product (PDP).

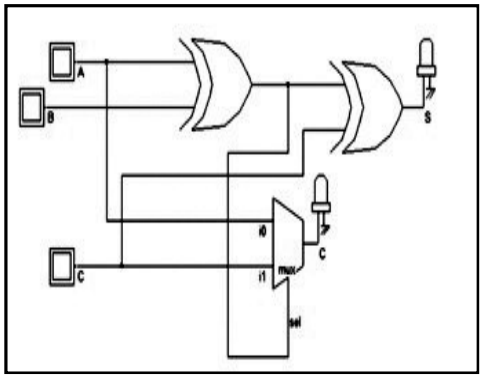

Figure 6: XOR-XOR and MUX implementation of Full Adder

3.10. XOR-XOR and MUX using PTL

An improvement in the implementation of (Figure 6.) at circuit level has resulted in low power consumption and lesser delay. Here, an energy efficient single bit full adder with 16 transistors using six transistor XOR gate, inverter and multiplexer blocks using pass transistor logic have been presented in Figure 7.

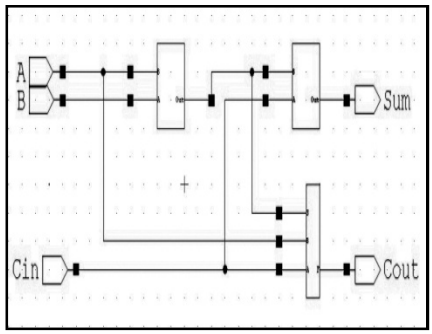

Figure 7: XOR-XOR and MUX Full Adder

3.11. Full Adder using Transmission Gate [TG]

20 Transistor transmissions produce buffered outputs of proper polarity for both sum and carry. (Fig.8). In this circuit 2 inverters are followed by two transmission gates, which act as 8-T XOR. Subsequently 8-T XNOR module follows, where, 4 transistor XOR in the next stage is inverted to produce XNOR. These XOR and XNOR are used to generate sum; **cin** and *Cin* are multiplexed, which can simultaneously used to generate sum and cout. The power dissipation in this circuit is more than the 28T adder. However, with the same power consumption, it performs faster [8].

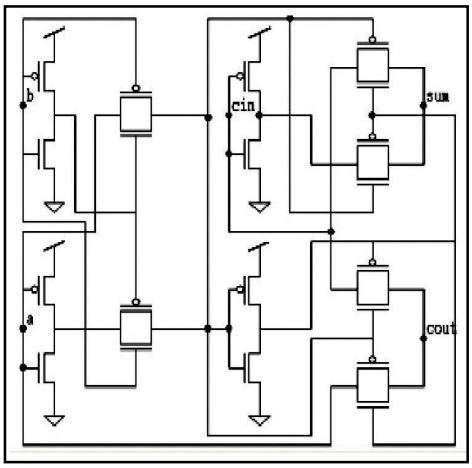

Figure 8: 20T Full Adder using TG

3.12. 10T Full Adder using CMOS

The basic advantage of 10T full adders is a smaller area and lower power utilization (Figure 9.). It becomes more not easy and even obsolete to keep full output voltage swing operation as the design with fewer transistor count and lower power utilization is pursued. In pass transistor logic the output voltage swing may be degraded due to the threshold voltage defeat problem. The reduction in voltage swing leads to lower power consumption, but may also lead to slow switching in the case of cascaded operation such as ripple carry adder. A low VDD operation the corrupted output may even cause break down of circuit. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions [7]. The elimination of the path to the ground reduces the total power use by reducing the short circuit power.

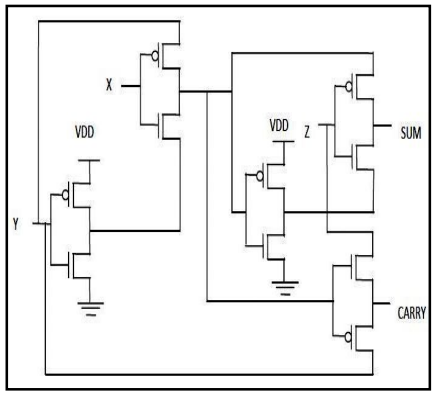

Figure 9: 10T Full Adder using CMOS

3.13. 10T Full Adder using TG

A 10T full-adder is shown in Figure 10. It is incorporation of CMOS and TG techniques and it has 10 transistors in its structure. This full-adder has the least number of transistors among all full-adders in this paper, moreover, it has a very low propagation delay, but its problem is high consumption power as compared to other circuit except 10T CMOS Full Adder.

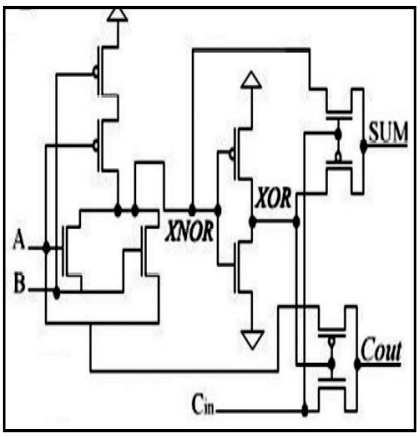

Figure 10: 10T Full Adder using TG

4. Results and Discussions

The basic full adder with 42T in CMOS, 30T in Hybrid PTL/CMOS, conventional full adder using CMOS with 28T, 16T, 14T and 10T are all simulated using TSpice and 45Nnm CMOS technology. The delay parameter is calculated from the time that the clock signal reaches 50% of the supply voltage level, to the time that the output reaches the same voltage. The average power consumption during all the transitions is considered as the power consumption parameter. Finally, the power-delay product (PDP) is the multiplication of the maximum delay and the average power consumption.

4.1. Tables

The results are shown in Table 2 depicting the average power consumed for all the full adder circuits and Table 3 depicts the power delay product (PDP) for the full adder circuits. The voltages we have worked on are 0.6v, 0.8v, 1v and 1.2v.

TECHNIQUES	0.6V	0.8V	1.0V	1.2V
BASIC_FULLADDER CMOS (TC-42)	0.6304 e-006	2.046 e-006	5.073 e-006	10.279 e-006
BASIC_FULLADDER HYBRID (TC-30)	0.5689 e-006	1.773 e-006	4.905 e-006	10.93 e-006
FA_USING_CMOS NAND_REP (TC-36)	0.4864 e-006	1.6631 e-006	5.054 e-006	11.377 e-006
FA_USING_HYBRID NAND_REP (TC-24)	0.4900 e-006	1.295 e-006	4.0861 e-006	9.725 e-006
NAND_GATE_FA (TC-36)	0.5379 e-006	1.1241 e-006	3.184 e-006	7.5630 e-006
NOR_GATE_FA (TC-48)	0.5812 e-006	1.2210 e-006	3.5105 e-006	8.1700 e-006
CONVENTIONAL_ CMOS(TC-28)	0.2663e-006	1.066 e-006	3.1136 e-006	7.4542 e-006
CONVENTIONAL_ HYBRID (TC-16)	0.3144 e-006	0.9564e-006	2.818 e-006	6.492 e-006
2XOR&2:1MUX USING_CMOS (TC-44)	0.5400 e-006	1.857 e-006	4.687 e-006	10.190 e-006
2XOR & 2:1 MUX USING_CMOS&TG (TC-18)	1.8602 e-006	2.8605 e-006	0.1818 e-006	0.4483e-006
2XOR&2:1MUX USING_PTL (TC-16)	0.3079 e-006	0.9435 e-006	2.836 e-006	13.80 e-006
FA_USING_TG (TC-20)	0.0437 e-006	0.1248 e-006	0.5781 e-006	1.597 e-006
10T CMOS	0.347 e-006	1.069 e-006	2.949 e-006	6.468 e-006
10T TRANSMISSION GATE	0.1296 e-006	0.3862 e-006	1.1798 e-006	2.971 e-006

Table 2: Power consumed for all full adder circuits

TECHNIQUES	0.6V	0.8V	1.0V	1.2V
BASIC_FULLADDER CMOS (TC-42)	38.30 e-015	1116.09 e-015	2122.03 e-015	31520 e-015
BASIC_FULLADDER HYBRID (TC-30)	603.71 e-015	1912 e-015	5371.9 e-015	11982.55 e-015
FA_USING_CMOS NAND_REP (TC-36)	29.544 e-015	94.134 e-015	74.132 e-015	284.76 e-015
FA_USING_HYBRID NAND_REP (TC-24)	24.015 e-015	54.10 e-015	83.11 e-015	196.29 e-015
NAND_GATE_FA (TC-36)	31.98 e-015	00079.191 e-015	190.05 e-015	213.20 e-015
NOR_GATE_FA (TC-48)	51.92 e-015	71.01 e-015	202.52 e-015	452.12 e-015
CONVENTIONAL_ CMOS(TC-28)	5.719 e-015	13.73 e-015	58.18 e-015	190.9 e-015
CONVENTIONAL_ HYBRID (TC-16)	20.10 e-015	38.93 e-015	71.0136 e-015	2581.2 e-015
2XOR&2:1MUX USING_CMOS (TC-44)	10.61 e-015	75.59 e-015	113.80 e-015	768.88 e-015
2XOR&2:1 MUX USING_CMOS&TG (TC-18)	2.2806 e-015	43.625 e-015	1.178 e-015	2.929 e-015
2XOR&2:1MUX USING_PTL (TC-16)	19.83 e-015	38.40 e-015	71.43 e-015	552.41 e-015
FA_USING_TG (TC-20)	0.8043 e-015	0.2996 e-015	1.3884 e-015	3.8353 e-015
10T CMOS	10.718 e-015	16.10 e-015	60.3 e-015	132.2 e-015
10T TRANSMISSION GATE	15.161 e-015	22.077 e-015	43.58 e-015	23.688 e-015

Table 3: Power Delay Product (PDP) for all full adder circuits

5. Conclusion

From the analysis of the above various types of Full Adder Circuits. It can be concluded that the average power is low for Full Adder using Transmission gate logic with 20T. The Power Delay Product is also low for Full Adder using Transmission gate logic with 20T. Full Adders are the heart of any digital and data processing application like specific integrated circuit (ASIC) is its data path. At the heart of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Addition is the most basic arithmetic operation; and an adder is the most fundamental arithmetic component of the processor. This paper presents the implementation of various types of Full Adders using MOSFET and concluded that the Full Adder using Transmission gate logic with 20T circuit is fit for delay and power centric design.

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