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Design of Low Power Level Shifter for Multi Supply Voltage System Using MTCMOS

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Abstract:
In this paper, a low leakage multi-Vth level shifter is designed for robust voltage shifting from sub threshold to above threshold domain using MTCMOS technique and sleep transistor. MTCMOS is an effective circuit level technique that improves the performance and design by utilizing both low and high threshold voltage transistors. Leakage power dissipation has become a main concern for VLSI circuit designers. In this a "sleep transistor" approach is preferred which reduces the leakage power while saving exact logic state. The new low-power level shifter using sleep transistor compares with the previous work for different values of the lower supply voltage. When the circuits are individually analyzed for power consumption at 45nm and 90nm CMOS technology, the new level shifter offers significant power savings up to 78% as compared to the previous work. Alternatively, when the circuits are individually analyzed for the minimum propagation delay, speed is enhanced by up to 23% with our approach to the circuit. All the simulation results are based on 45nm and 90nm CMOS technology and simulated in Cadence tool.

Keywords*: Level shifter (LS), Multi-Supply Voltage, multi-threshold CMOS (MTCMOS), sleep transistor, low power, sub-threshold Operation*

1. Introduction

In modern VLSI technology, SOC design has the building blocks of component (analog, digital, mixed single chip). Each component of a chip has operated at proper power supply voltages. Complex integrated circuits operating with supply voltages as low as 0.5V. Level shifter is needed when the signal passes from low level logic to high level logic. So the level shifter can be placed between these two voltage domains (low-to-high). Level shifters are also an important circuit component in multi voltage systems and have been used in between core circuits and I/O circuit.

Multi supply voltage domain technique is emerging as an effective method to reduce both dynamic and leakage powers in today's system-on-chips [ix]. The use of multiple supply voltages to reduce energy consumption is a very commonly used technique in CMOS circuits, and then the dynamic power of a CMOS circuit is directly proportional to the square of its supply voltage [viii]. Multiple thresholds and transistor sizing can be combined with voltage scaling to get more power savings. When using multiple supply voltages in a circuit we might need to convert the voltage level from one value to another voltage level, with level shifters. This approach consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas noncritical sections work at a lower power supply voltage (VDDL) to improve power efficiency. For extremely low-power applications, the presence of circuit sections operating in the sub threshold regime is a valuable option [vii], [viii].

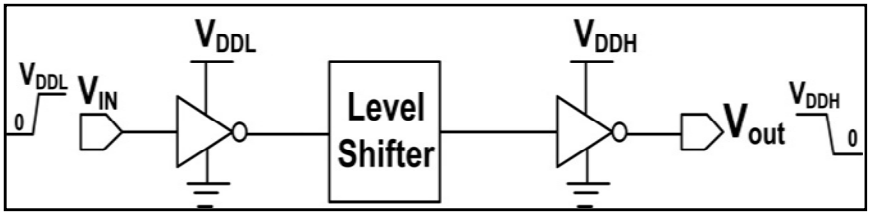

Figure 1: Level Shifter

The differential cascade voltage switch is the level shifter circuit. The multiple threshold CMOS circuit is acting in low voltage and high voltage domain. If the low voltage domain directly drives a high voltage domain leads to product failure and speed will affects greatly. Multi threshold CMOS LS used to reduce the leakage power and increase the speed of the level shifter circuit [i].

Power consumption of CMOS consists of dynamic and static components. Dynamic power consumption is when transistors are switching and static power consumption is regardless of transistor switching. One of the main reasons causing the increase in leakage power is the increase of sub threshold leakage power. When technology scales down, supply voltage also scales down simultaneously. The Sub threshold leakage power increases exponentially as threshold voltage decreases.

Key challenges in the design of efficient multiple-supply circuits are minimizing the cost of the level conversion between different voltage domains while maintaining the overall robustness of the design. For such a purpose, level shifter (LS) circuits have to be used. Traditionally, level shifter circuits were used to allow chip core signals to be transmitted to the outside world through the pad ring, which often operated with different voltage levels. More recent techniques were emerged which allows for the increased use of voltage islands within chips.

To down-convert from a higher voltage (within the oxide breakdown limits) to a lower voltage domain, CMOS inverters are usually adequate [i], [ii]. On the other hand, more complex LS topologies are required to up-convert signals from the lower to the higher power supply domain [xiv]. This issue is particularly compounded when the VDDL is lowered below the transistor threshold voltage. In fact, in such a case, balancing the input section driving capability of the LS with sections of the circuit working at the VDDH voltage level requires proper design techniques [i], [ii]. In standby mode sleep transistors are used as switches to shut off power supplies to parts of a design. A sleep transistor is referred to either a PMOS or NMOS high VTH transistor that connects permanent power supply to circuit power supply. The sleep transistor is managed effectively by a power management unit, to switch on and off power supply to the circuit. The Sleep transistor PMOS is used to switch VDD supply [ii-iv], [xvi].

This paper deals with a novel low-power LS designed to convert near-threshold or sub-threshold voltages to above-threshold voltage levels. When implemented with the cadence 45nm and 90nm CMOS technology, the new design successfully converts input voltages as low as 0.4 V to the 1.8V nominal output voltage.

This paper is organized as follows. Section II provides briefly gives a review of existing work. Section III presents the proposed level shifter circuit and its operation. And Section IV shows simulation results, simulation waveforms and performance comparison of power. Finally, in Section V conclusions are drawn.

2. Related Work

The traditional LS topology is the differential cascade voltage switch (DCVS) circuit, as shown in Figure 2. The DCVS-LS behaves as a ratioed circuit and there is a contention between transistors.

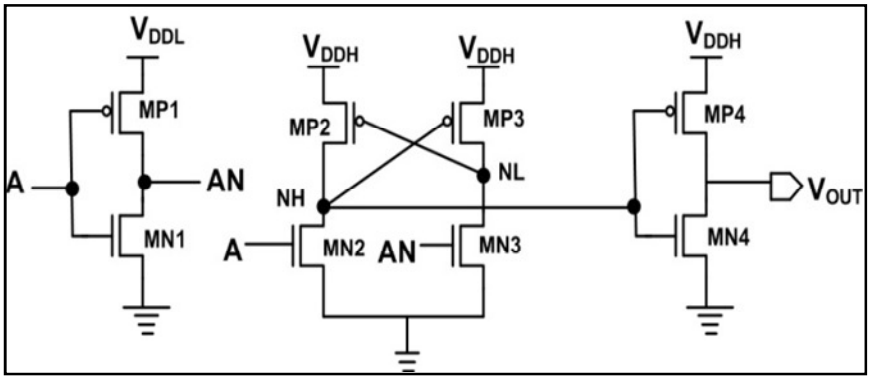

Figure 2: Conventional DCVS Circuit

As a consequence, pull-up and pull-down strengths need to be properly balanced to ensure correct functionality. This requirement is difficult to achieve in practice when input signals have sub-threshold voltage levels [i]. The main drawback of the Differential cascade voltage switch circuit leads large power penalties. So we need to require multiple powers switching to generate intermediate high voltage devices Level shifter with Multi threshold CMOS technique. It does not contain the intermediate power line.

In [ii] Authors used a new sub threshold to above-threshold LS circuit based on a Wilson current mirror. The circuit doesn't have a static current path between the supplies and therefore offers reduced static power dissipation. In this respect, the level shifter behaves similar to common CMOS logic gates in sub threshold. NMOS to PMOS ration is required to make LS operate correctly at low voltage. Due this results large bandwidth of NMOS transistors, so this circuit is not suitable for sub threshold to an above threshold level shifting. In [iii] Authors used demonstrated a sub threshold level shifter that is fabricated in 130nm process. Conversion range of the circuit is used reliably up converter to 1.2V. The advantage of this design is the number of PMOS transistor is tied to VDD. So it can easily weaken the pull up network. The main drawback of this circuit is it contains only two stages, both stages uses only cross coupled differential inverter. So it requires more leakage power consumption.

In [iv] Authors used in this checked in the context of translating the signals from sub threshold levels to traditional CMOS levels. Three level shifter circuits using body ties to adjust the drive strength of the transistors. However, this technique is only practical in

SOI CMOS, as individual body connections are needed for each transistor. In bulk CMOS technologies, isolated p-wells would be needed, requiring additional manufacturing steps and leading to the high area overhead. Another disadvantage is that there are still static current paths through the forward-biased source bulk diodes. All six circuits were calculated in terms of power, performance.

In [vii] presented two novel sub threshold logic families. Both VT-sub-CMOS and sub-DTMOS logic families show the superior robustness and tolerance to temperature and process variations than that of regular sub threshold CMOS logic. VT-sub-CMOS logic can be readily implemented in twin-well process technology, but it requires additional circuitry for stabilization. To convert the circuit from 200mV to 1.2V, it consists of three intermediate stages of conversion between two voltage domains. The major drawback of the circuit is increasing the power dissipation.

The possibility of exploiting a dynamic threshold MOS (DTMOS) configuration to implement the NMOS devices of the conventional DCVS circuit was explored by Chavan *et al.* [iv]. The resulting LS topology uses pull-down devices that, when turned on, exhibit improved drive strengths with respect to the pull-up networks. Unfortunately, owing to individual body connections needed for each transistor, this technique is easily practicable only in SOI CMOS.

In [i] Authors used as differences between the new architecture and the conventional DCVS, Shown Figure 3 A high to low transition of the main input causes MP4 to turn ON and causes MP6 device in the saturation region. This creates a voltage drop (i.e., VTH, MP6) across MP6 terminals that produce a correspondent bulk source voltage drop on MP4. The reduced voltage level of the source terminal of MP4 limits its V_{GS}, and also weakens the MP4 action. All the above effects and reduce the disputation on the node NH, thus allowing faster discharging to be achieved.

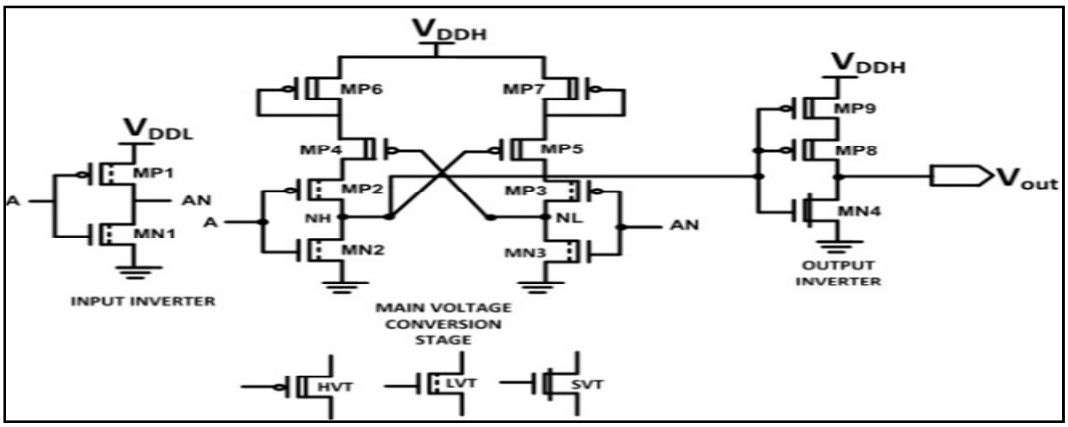

Figure 3: Conventional Level Shifter

When MP4 is turned ON, the MP5 is therefore turned OFF. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 ON. For this, MP5 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current. The diode-connected MP7 device minimizes the leakage current, also by increasing the threshold voltage of MP5. In fact, MP7 causes the source of transistor MN4 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect.

The above described circuit differs from those adopted in other LS designs that use diode-connected transistors [iii]. Since MP6 limits the output range of the main conversion stage to [0V, VDDH – VTH], an output inverter connects to node NH, to assure a rail-to-rail conversion. The pull-down of such an inverter uses normal 1v device, whereas its pull-up is designed by using an (HVT) (high threshold voltage) PMOS transistors stack, thus limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high. Opposite and considerable threshold voltage variations on MP6 and MP8-MP9 can cause the latter transistors to go in weak inversion, thus increasing the static power dissipation. It has taken more power consumption. So it overcomes to propose LS using MTCMOS.

3. Proposed Level Shifter

The novel multi VTH level shifter is described in this section. This level shifter uses a multi VTH CMOS technology in order to eliminate static DC current, and it helps to reduce the power. According to fig.4, consists of an input inverter, a main voltage conversion stage (MP1-MP6, MN1-MN2), an output inverting buffer (MP7-MP8, MN3) and sleep transistor (MP9). To increase the strength of the pull-down network of the main voltage conversion stage, it was also designed by using low-Vth 1V transistors, pull up network and sleep transistor are designed by high-Vth 1Vtransistors. This multi threshold CMOS is used to reduce power.

The current flowing through the nodes NH and NL at the beginning of their high to low transition could be of concern. Because sub Vth dominates modern device off state leakage due to the low Vth is used. Thus, to reduce this effect, two PMOS devices (MP1 and MP2) are adopted. MP3 and MP4 helped in weakening the pull-up networks of the main voltage conversion stage, thus reducing conflict NH and NL nodes.

These nodes also reduced the leakage current flowing through the pull-up networks when they are turned OFF. Finally, to achieve reliable voltage conversion, two diode-connected PMOS devices (MP5 and MP6) were placed between the pull-up logics and the supply rail VDDH. These devices limit the pull-up strength, but also reduce leakage power. A high to low transition of the main input causes MP4 being turned ON. Its drain current brings the diode-connected MP5 device in the saturation region.

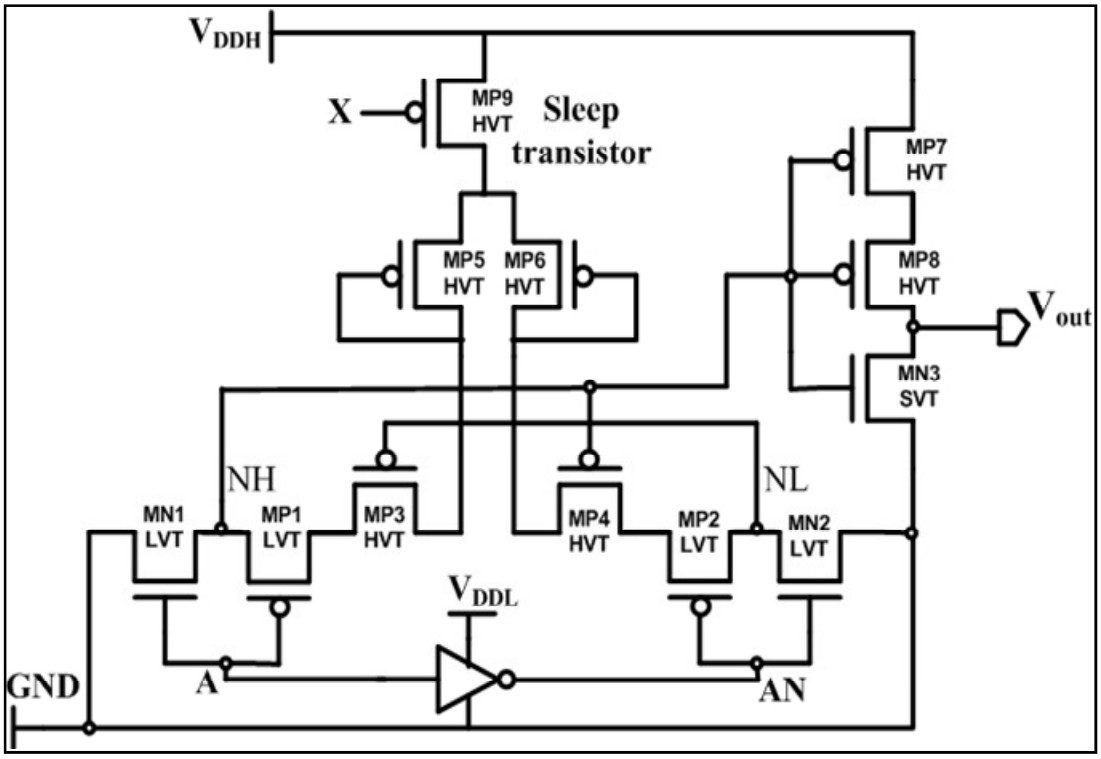

Figure 4: Novel Level Shifter

In this region creates a voltage drop across MP5 terminal that produce a bulk source voltage drop on MP3. Due to this bulk effect, there is an increase in the MP4 threshold voltage and the reduced voltage level (VDDH-VTH, MP5) on the source terminal of MP3 limits its VGS, thus further weakening the MP3 action. When MP3 is turned ON, the MP4 is therefore turned off. In this case, the small leakage current flowing through MP5 is not enough to turn MP7 ON. For this reason, MP4 results power gated from the VDDH power rail, leading to a significant reduction in its sub-threshold current. The diode-connected MP6 device minimizes the leakage current, also by increasing the threshold voltage of MP4. In fact, MP6 causes the source of transistor MP4 to be at lower voltage than the bulk node and thereby reduces the sub-threshold leakage current due to the bulk effect.

This significantly differs from those adopted in other LS designs that implemented diode connected transistors [iii]. Since MP5 limits the output range of the main conversion stage to [0 V, VDDH – VTP], an output inverter connects to node NH, to assure a required conversion. The pull-down of such an inverter uses a MP7, MP8 and MN3 device, whereas its pull-up is designed by exploiting PMOS (HVT) transistors stack, thus limiting the leakage current flowing through the pull-up network of the output inverter, when NH is high. Opposite and substantial threshold voltage variations on MP5 and MP7-MP8 could, cause the latter transistors to go in weak inversion, thus increasing the static power dissipation. Now the PMOS sleep transistor is placed in series with MP5, MP6, MP7 and power supply (VDDH). A sleep control scheme is used for efficient power management. In the active mode, X is set low and SLP P (HVT) is turned ON. Since its on-resistances are small, the supply voltage almost functions as a real power line. In the standby mode, X is set high, SLP P (HVT) turned OFF and decreasing the power dissipation.

4. Simulation Results

In this section, the proposed level shifter is designed in sub micron CMOS technology. The proposed level shifter is compared to the conventional level shifter for average power consumption, delay, and power-delay-product (PDP). The availability of high efficiency power supplies and multi-VTH CMOS technology are the important factors affecting the optimum supply voltages in a Multi-VDD system. A wide range of lower supply voltages is considered in this paper since the factors vary with the 45nm and 90nm technology. The simulations are carried out for the following different values of VDDL: 0.7V, 0.9V, and 1V for conventional level shifter and then for same voltages LS using sleep transistor is verified at above voltage values. Comparison results are obtained using LS with sleep transistor than conventional Level shifter. The conventional level shifter and the proposed level shifter are implemented in Virtuoso Schematic Editor and Spectre simulator using a 45nm and 90nm CMOS process technology. These tools are part of Cadence Virtuoso Design Environment provided by Cadence Design Systems. Generic Process Design Kit (GPDK) 45nm and 90nm technology file is used to get the transistor models. Table 1 and 2 are describes change the VDDL to shifts VDDH values, then we find power, delay and power-delay-product (PDP) of Proposed LS in 90nm and 45nm technology. The comparisons of power and PDP in different circuits in 45nm technology are given in Table 3.

The figure.5 shown simulation waveform of the proposed level shifter of the figure.4, the Waveform consists of sleep transistor X is given high, A and AN is inverter values is given VDDL=0V-0.7V, the nodes NL and NH, Vout value is equal to VDDH=0-1.8V, and Power signal, When the voltage scale down by reducing the power and PDP.

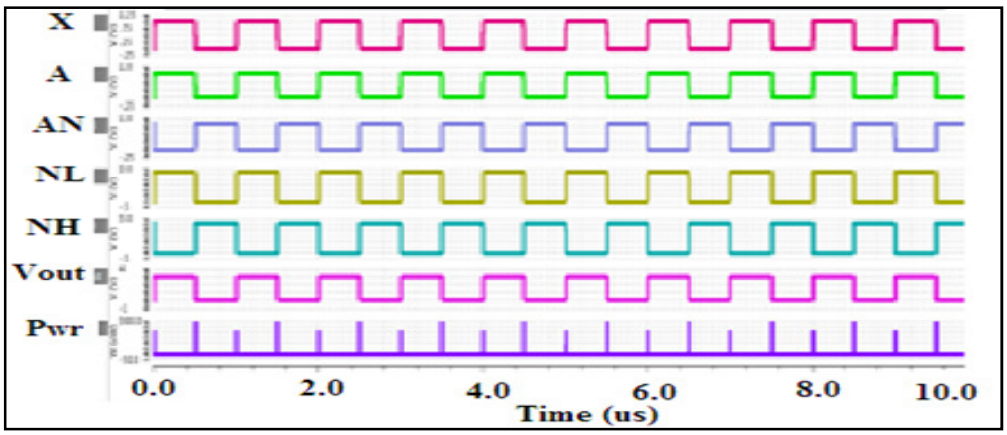

Figure 5: Simulation Wave Form of Proposed level shifter in 45nm technology at VDDL =0.7V, VDDH=1.8V at 1MHZ.

Parameter	V_{DDL} (V)	V_{DDH} (V)	Power (µW)	Delay (ns)	PDP (fJ)
Proposed Level Shifter	0.7	1.8	0.155	2.48	0.38
		3	2.026	1.24	2.51
	0.9	1.8	0.211	2.00	0.42
		3	2.26	1.11	2.51
	1	1.8	0.254	1.81	0.46
		3	2.34	0.92	2.15

Table 1: Summary of Proposed Level Shifter in 90nm Technology

Parameter	V_{DDL} (V)	V_{DDH} (V)	Power (nW)	Delay (ns)	PDP (fJ)
Proposed Level Shifter	0.7	1.8	27	5.82	0.15
		3	310	7.78	2.41
	0.9	1.8	28	4.55	0.12
		3	258.1	6.16	1.59
	1	1.8	33	4.09	0.13
		3	254	5.51	1.40

Table 2: Summary of Proposed Level Shifter in 45nm Technology

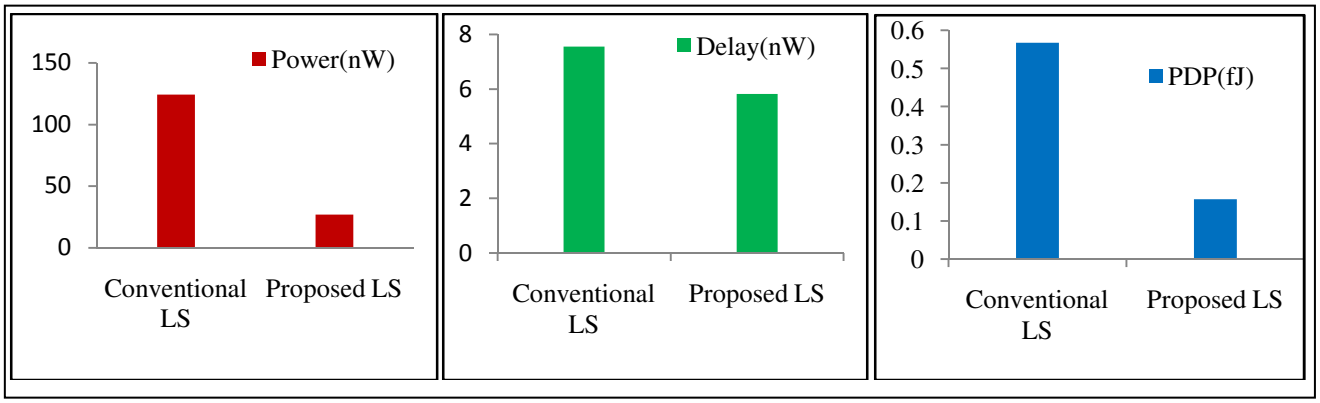

Figure 6: Comparison graphs of Average Power, Delay and PDP of Conventional and proposed level shifters in 45nm Technology.

Parameter	Power (nW)	PDP (fJ)
TSLS	271	1.9
WCM LS	71	0.35
LVLC	118	0.67
Conventional Level Shifter	168	0.55
Proposed Level Shifter	33	0.13

Table 3: Performance and characteristics comparisons of different circuits at VDDL = 1V and VDDH=1.8V in 45nm technology

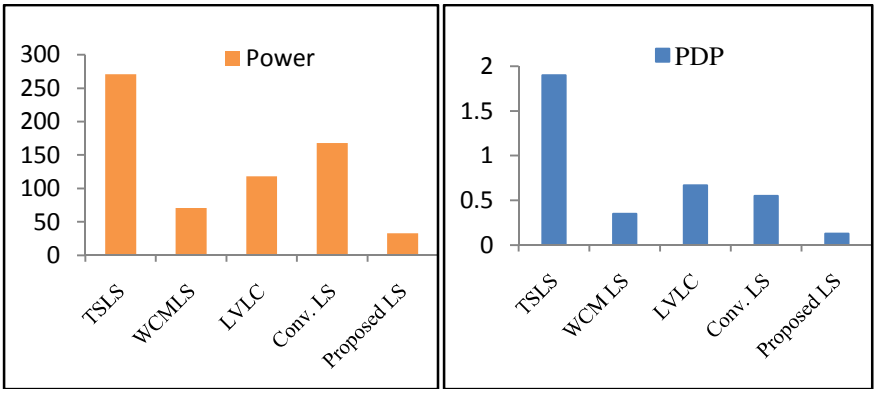

Figure 7: Power and PDP comparisons in different level shifters at 45nm technology

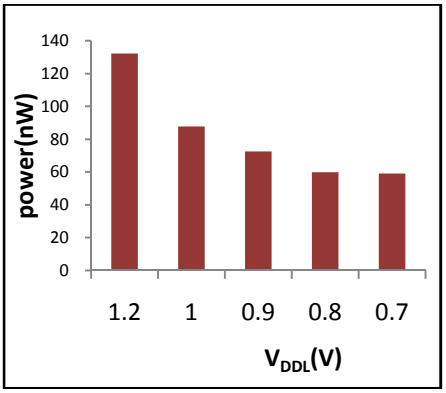

Figure 8: VDDL Vs Power

5. Conclusion

The simulation results of the level shifter in a 45nm and 90nm process Technology show that this circuit topology offers good performance and reduce power. The proposed level shifter circuit operates properly and output level of 1.8V has been obtained with the input pulse of 0.4V at 1MHZ frequency. It is designed using a 45nm and 90nm CMOS process in cadence virtuoso tool. The novel level shifter has reducing power consumption of 27nW and propagation delay of 5.82 ns and power delay product (PDP) of 0.157fJ, in 45nm technology. We has been observed of 78% on average power consumption and 72% on PDP compared with conventional level shifter. These level shifters suitable for wide I/O interface voltage applications in ultra-deep sub-micron.

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