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A Hybrid CMOS SET Made Indirect Logic Based Pulse Train Generator for BIOS Operation

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Abstract:
Hybrid CMOS SET is a promising field of advanced device research which encapsulates both the merits of CMOS transistors and single electron transistors in a nutshell. This short communication intends to deliver the logical synthesis of Hybrid CMOS SET in designing advanced indirect logic based pulse train generator for advanced computing. The logical analysis of the proposed model is made on the simulation study and the comparative analysis is derived from the test bench. The results are in good shape and thereby the authors hereby intend to report the same. An ephemeral introductory on hybrid CMOS SET is followed by design study and the same concludes with the comparative analysis of both the hybrid model and its conventional equivalent model.

Keywords: *MIB Model, Hybrid CMOS SET, Indirect Logic, Pulse Train Generator, Advanced Computing.*

1. Introduction

Mesophysics is a customized study of nano regime physics. Besides Mesophysics Researchers at Delft University reported inter allied co-designing of existing CMOS technology and newly invented ultra-modern Single Electron Transistor (SET) tunnelling technology [i-v]. Apparently this conceptualized the hybridization of CMOS and SET [vi]. Perhaps this is the ultimate form of device research as the device engineers can manipulate single electron with the help of e beam lithography. The technique bridges the gap of background charge problem, low gain, room temperature operation of SET as well as dimnish the scaling issues of CMOS transistors in one platform. Other merits of this novel topology is crafted from the analytical study of MIB model coined from the research led by Prof. Santanu Mahapatra [vii]. He and his team empirically demonstrated the robustness of hybrid CMOS SET which was later incorporated by TOSHIBA very recently. Convincingly Prof. Mahapatra's team reported [viii] the perfect co bonding of two device metaphor only to resemble the attributes of high speed low power consuming ULSI nano devices.

Following the same pathway of device research worldwide, Scientists emphasized on hybrid CMOS device research involving both analogue research as well as typical logic oriented device synchronization [ix-xvi]. Promisingly the analytical study of predecessors reached major attention; lacking of sophisticated lithography techniques pointed out inadequate scope in mobilizing the fundamental topology into logical synthesis using SET. Thus the research for device miniaturization was categorically upheld into numerical computations only. Then after the next phase of research of Hybrid CMOS SET based logical synthesis was augmented by Japanese group of Scientists during 2009. This motivated Researchers in developing Hybrid CMOS SET based logical orientations which mimics the logical output of conventional CMOS logic gates. Thus Researchers worldwide anticipated the ample scope of Hybrid CMOS SET based logic device modelling which catered interest both in academia and in industry.

Here Researchers and students conventionally adapted Hybrid CMOS SET based logic realizations in developing indirect logic based pulse train generator which is of utmost importance in electronic industry appliances. The authors largely adhered to the previous works of Gope et.al. [xvii-xxiii] to design the pulse train generator and empirically demonstrated its uniqueness compared to conventional pulse train generators.

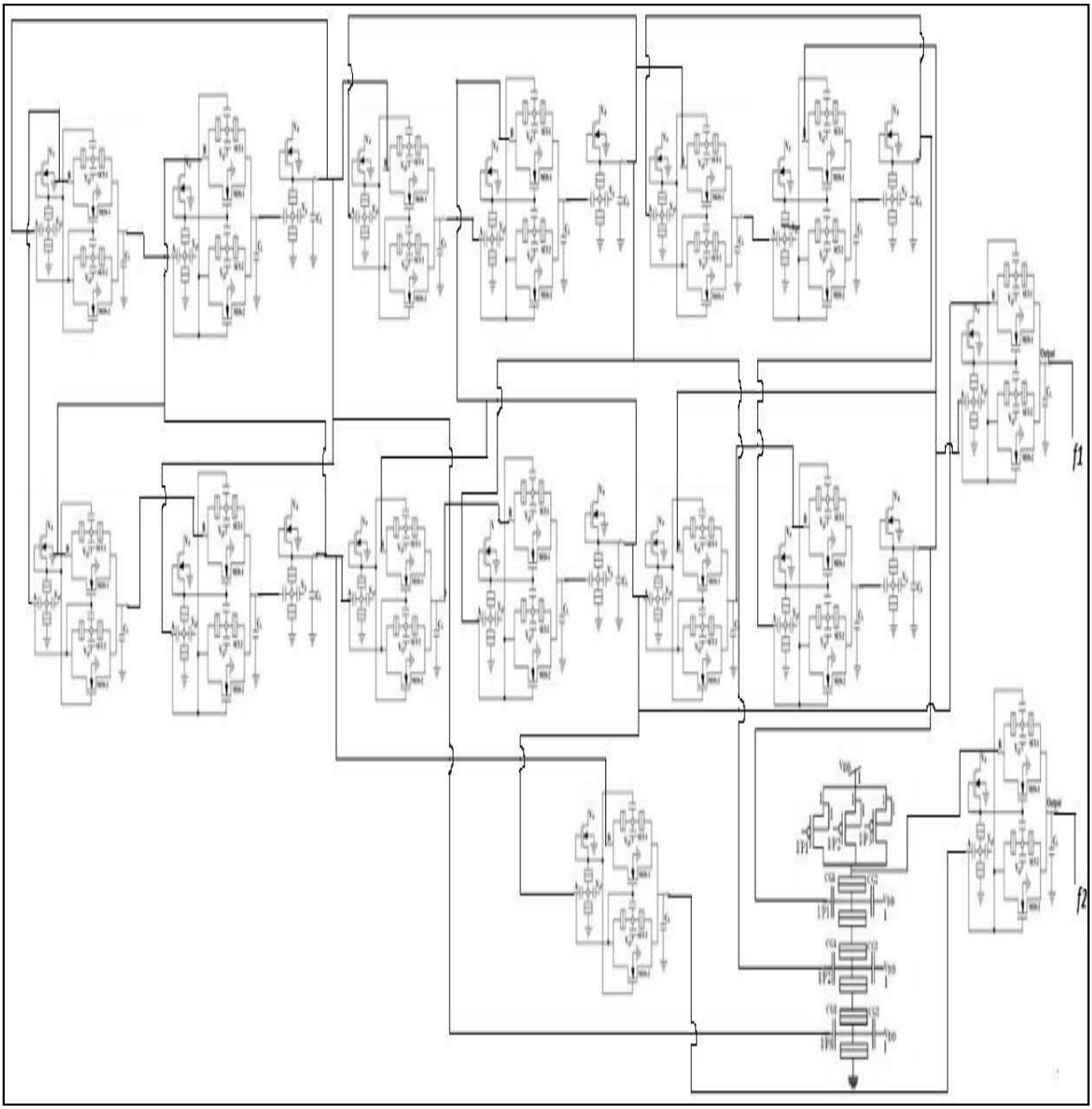

Figure 1: Hybrid CMOS SET Based Nano IC for Indirect Logic Based Pulse Train Generation

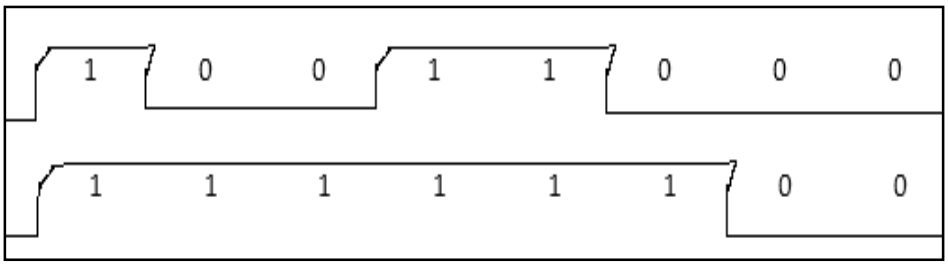

Figure 2: Response of Hybrid CMOS SET based proposed model vs. its traditional counterpart

2. Design and Implementation of Hybrid CMOS Set Based Indirect Logic Oriented Pulse Train Generator

Fig 1. Is a compact monolithic hybrid CMOS SET based nano IC intended for Indirect Logic based pulse train generation operation and it comprises of 108 tunnel junctions and 126 capacitors. The load of CMOS here in this circuit is the SET driven by merely 0.20mv and logic 1 implies 0.18mv (high) whereas logic 0 is substantially low ~0.01mv. The other considerations of the proposed design are that it requires at least three subsections of Hybrid CMOS SET based Flip Flops and the output is obtained from f1 and f2. The combinational logic at the right most end is a typical analogy of logical synthesis of synchronous/ripple counters made up of the novel Hybrid CMOS SET logic gates.

For test bench implementation the authors considered two pulse trains i) 10011000 and ii) 11111100. As these are both 8 bits long thus 8 unique states to generate those two pulse trains are essentially required. This is why a mod 8 i.e. a 3 bit ripple counter is used in the right most side and f1 and f2 provide the outputs of the combinational synthesis. By and large f1 and f2 produces a waveform quite similar to as shown in Fig.2.

The present model embraced highest implementation of Hybrid CMOS logic orientation of in one typical complex indirect logic based circuit. Eventually the proposed model poses the virtue of nano device methodology and cordially can be included in BIOS architecture for high speed large computation. As the proposed model showed no errors in performing the logic operations thus the next few states i.e. i)power consumption and ii)propagation delay are now here is eventually considered for comparative analysis. Table I below indicates the estimated value of Hybrid CMOS SET based gates perpetually to the CMOS based logical interventions.

Power Supply	No. of CMOS gates	No. of SET gates	Power Consumption	Propagation delay
0.01v	54	54	4.12e-09W	~ 1 ns

Table 1

3. Conclusion

The simulated model of Hybrid CMOS SET made indirect logic based typical pulse train generator produces successful implementation of pulses in a sophisticated manoeuvre. This design has the attire of low power consumption (4.12e-09W), and high speed caused from extensively nullified propagation delay of (~ 1 ns); furthermore, the typical size of the circuit is in nm range. It is also noteworthy that the circuit produces high gain and can be designed in room temperature operations. Last but not least the switching speed mobility and power dissipation improves satisfactory in the proposed model. Henceforth, the authors advocate the incorporation of such models in the BIOS for future advanced computing systems.

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