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Topology Comparison and Design of Low Noise Amplifier for Enhanced Gain

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Abstract:
This paper presents the comparison of Low Noise Amplifier (LNA) and the design of Common gate as topology and Cascode inductive Source degeneration topology. The Low Noise Amplifier with Common gate as topology and Cascode inductive Source degeneration has been designed for the required noise figure and gain characteristics. The design of LNA is discussed and topologies chosen were simulated using Ansoft Nexxim designer. The design using the Common gate stage achieved a very low gain with a value of 0.86 dB. The LNA with the cascode design of single ended form is then simulated which achieved a higher gain of 24.5 dB. This basic study is used to understand the characteristics of LNA topology under similar conditions.

Keywords: *LNA, Common Gate, Cascode, Gain.*

1. Introduction

Low noise amplifier (LNA) is an important building block in RF communication system. Noise figure (NF) of LNA dominates the sensitivity of whole receiver system [1]. The primary goal of Low Noise Amplifier is to get large gain with low noise figure. Generally, the impedance mismatch provides signal distortion and loss in the circuit design. This type of impedance mismatch losses can be minimized by inserting proper matching networks to achieve 50Ω impedance at input termination of wideband LNA. The various types of impedance matching networks can be employed depending on the requirement by using either a resistive termination in parallel at the input of the amplifier or a negative feedback. But this resistive network has an effect on amplifier's noise figure which can be replaced with inductive source degeneration to meet impedance matching without the resistive thermal noise [2]. For short range point-to-point links with data rates of several Gbits/s a millimeter wave LNA circuit is used for band from 57 to 66 GHz. CMOS technology has enabled high-performance and energy-efficient digital circuits with smaller chip area. The high data-rate with low cost fully integrated analog RF-front-end, baseband and self-calibration circuitry on single die [3]. By varying the biasing current of the gain stage, the gain can be controlled without affecting the figures of merit of the circuit for the UWB LNA with different link budgets. The gain is sufficient over the entire bandwidth of 7500-MHz with input impedance matching of 50Ω and noise figure is low to enhance the sensitivity of the receiver with low power LNA [4]. Due to the use multiple stages, they occupy more space and consume high power with good performance in matching and power gain [5]. For short range point-to-point links with data rates of several Gbits/s a millimetre wave LNA circuit is used for band from 57 to 66 GHz. CMOS technology has enabled high-performance and energy-efficient digital circuits with smaller chip area. The author proposed a current-mirror biasing with negative feedback based on the process, voltage, and temperature (PVT) insensitive current source (sink) which has strong immunity to these variations will result in low power, better bandwidth with minimal noise [6].

1.1. Low Noise Amplifier (LNA)

The communication system is growing faster and the transceiver section requires needful systems to receive the weakest signal from the medium without loss. To achieve this requirement amplifier can be used, which helps to improve the signal strength. However, a simple transceiver system consists of amplifier as major block. In the receiver section the front end design comprises of Low Noise Amplifier next to antenna in order to amplify the desired signal with low noise and is considered as a key element. In the designing of low noise amplifiers, the important goals are minimizing the noise figure of the amplifier, producing higher gain, low power consumption and producing stable 50Ω input impedance. To achieve all these goals different LNA architectures are available. Input matching architectures in LNAs can be classified into four types. They are Common-Source stage with resistive termination, Common-Gate LNA, Common-Source with shunt feedback, Common-Source with inductive source degeneration, Common-Source with Cascode inductive source degeneration. Each of these architectures can be implemented in single-ended or differential form.

1.1.1. CS Stage with Resistive Termination LNA

This technique uses resistive termination in the input port to provide 50 Ω input impedance. A 50 Ω resistor is placed in parallel with the input, to realize input matching for the LNA. The Figure 1 shows the Resistive termination of CS topology.

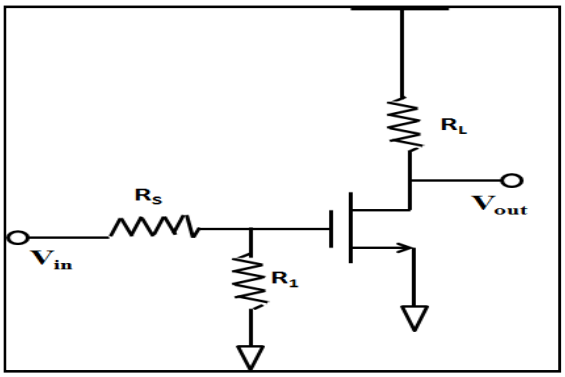

Figure 1:CS Stages with Resistive Termination Topology

The NF of this structure is very high. The NF degradation is due to two reasons. The added resistor R_1 contributes as much noise as the source resistor R_s does. The poor NF makes this architecture unattractive for applications where a low noise as well as a good input matching is desired.

1.1.2. Common-Gate LNA

The CGLNA is well known for wideband applications and its topology is shown in Figure 2. The input impedance and voltage gain of a CGLNA are

$$Z_{in} = \frac{1}{g_m} \quad (1)$$

$$A = g_m R_L \quad (2)$$

To realize the input matching, its g_m value is fixed at $\frac{1}{R_S}$. As a result, only the load impedance R_L remains as a design variable. Moreover, due to the input matching constraint, the transconductance of the input transistor cannot be arbitrarily high.

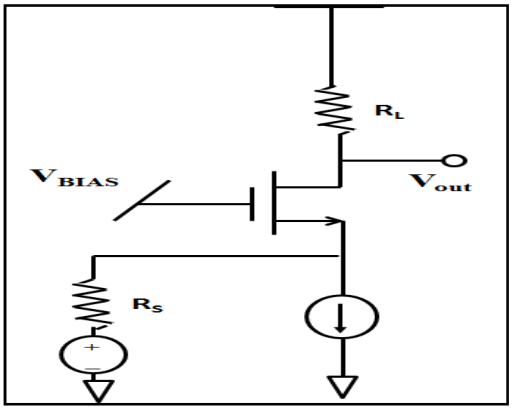

Figure 2: Common-Gate Stage Topology

The noise factor is given by,

$$F = 1 + \frac{\gamma}{\alpha g_m R_S} \quad (3)$$

When the input is matched, noise factor simply becomes $F = 1 + \frac{\gamma}{\alpha}$. This noise factor is quite reasonable and acceptable. However, it is important to note that other noise sources such as gate induced noise and substrate noise can degrade the performance substantially.

1.1.3. CS Stage with Shunt-Series Feedback LNA

Compared to the conventional CGLNA, it normally can achieve lower NF. However, it still has several disadvantages. Different topologies of negative feedback amplifier exist in the literature. The amplifiers which use shunt-series feedback architecture is shown in Figure 3, that dissipate higher powers compare to other architectures.

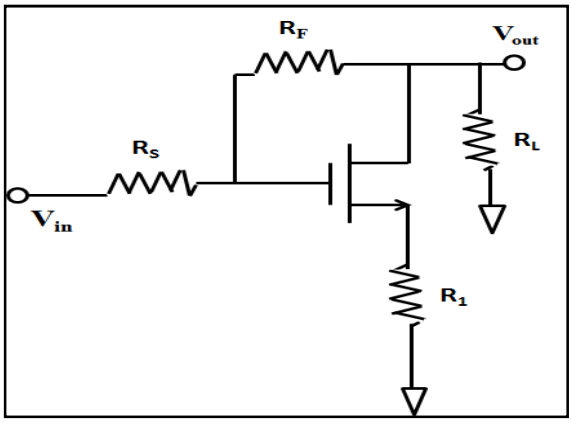

Figure 3: Topology of Shunt-Series Feedback

The channel thermal noise can be reduced by using noise cancellation technique for wideband LNA for this structure. Therefore, it has the same disadvantages. The LNA consumes 35 mW from 2.5 V supply voltage which is quite high for our targeted application.

1.1.4. CS Stage with Source Inductive Degeneration LNA

The input impedance has a resistive term, which is directly proportional to the inductance value. Even when different value of resistance is chosen, it does not generate thermal noise like an ordinary resistor, because a pure reactance is noiseless. The inductively degenerated LNA (L-degLNA for short) satisfies the input matching requirement without introducing the additional noise attributed to a real resistor.

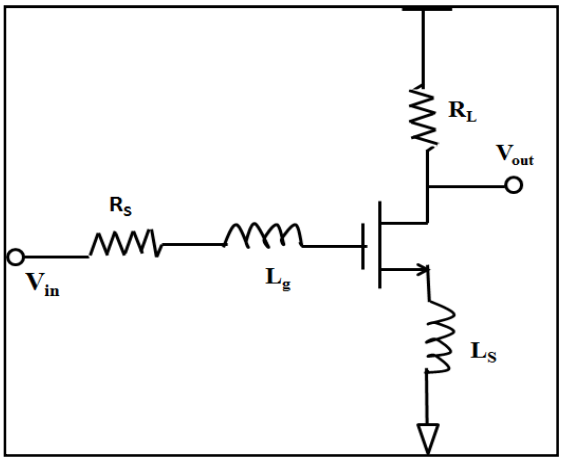

Figure 4: Source Inductive Degeneration Topology

In addition, compared to other architectures, L-degLNAs consume less power and therefore are especially suitable for low-power applications. The design of L-degLNA involves many trade-offs among gain, NF, power consumption, matching, and linearity. Several design techniques have been proposed to satisfy these requirements for different applications. The noise factor of the L-CSLNA without cascode stage is derived as

$$F = 1 + \frac{r_{LG}}{R_S} + \frac{\overline{I_{d1}^2}}{\overline{V_{in}^2}} \frac{1}{(g_{m1} Q_{EFF})^2} \qquad (4)$$

This topology is widely used in the design of CMOS narrow-band LNAs. However, in system-on-chip (SoC) design, inductor normally has low quality factor, i.e., has large parasitic resistance which significantly affects the input matching and the NF of the LNA.

1.1.5. CS Stage with Cascode Source Inductive Degeneration LNA

For CS topology, in order to have high reverse isolation and stability, a cascode structure is preferred and is shown in Figure 5. The quality factor is defined as the ratio of the voltage across the gate-source terminal and the voltage at the input of the input matching network.

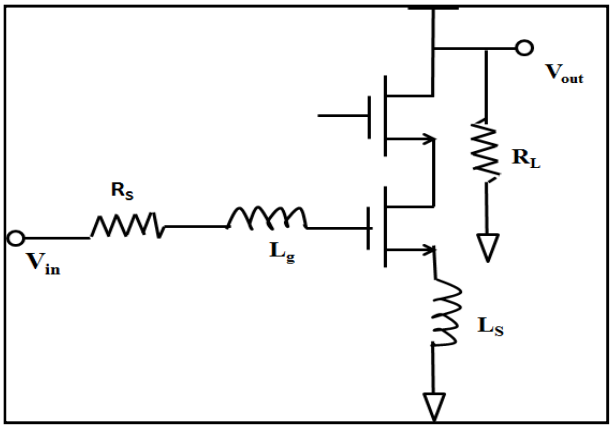

Figure 5: Cascode of source Inductive Degeneration LNA

In narrow-band systems, low noise figure is achieved by employing an inductive source degeneration to present a 50Ω input resistance without the resistive thermal noise. To satisfy the input power matching condition, another inductor is placed a gate of the MOSFET to resonate at the desired frequency, which is typically at the carrier frequency.

The noise Figure is given by

$$F = 1 + \frac{\overline{I_{d1}^{\,2}}}{\overline{V_{in}^{\,2}}}\left(\frac{1}{g_{m2}}\right)^2 \qquad (5)$$

The cascode stage has a relatively small impact on the overall noise figure if the input stage is not optimal. While it is known that increasing the width of the cascode device monotonically improves shielding from the output, its impact on the noise performance is not well understood. The width can increase until the bias of the cascode stage approaches the threshold voltage, or it can decrease until the input device reaches the linear region. The width of the cascode stage device is swept with the minimum channel length. The inductors L_S and L_G are readjusted to keep the input impedance to 50Ω. As the width of the cascode stage increases, the generated noise power from the cascode stage also increases.

TYPE	ADVANTAGES	DISADVANTAGES
Resistive termination common source	➢ Broad band amplifier. ➢ Good input match.	➢ Adding the noise from the resistor so Large NF.
Resistive termination Common gate	➢ The input impendence is equal to 1/gm. To get 50 Ω. ➢ Excellent input match.	➢ Huge NF and Power. ➢ The impedance varies with the bias current.
Current Reuse Technology	➢ Isolation of input and output is good. ➢ Higher gain. ➢ Lower noise figure.	➢ The inductor is off chip at low frequency.
Using Neutralization Technique	➢ Good reverse isolation	➢ Increased area. ➢ stability concerns
Inductive degeneration common source	➢ Good narrowband Match. ➢ Small NF. ➢ The source and gate inductors make the input impendence 50 Ω. ➢ Not adding noise from the input	➢ Increased area. ➢ The inductor is off chip at low frequency and low isolation.

Table 1: Comparisons of Low Noise Amplifier Topologies.

2. Common Gate Topology Design of LNA

The various types of Low Noise Amplifier have been proposed. In this SoC work the need of wide band is met with the topology of Common Gate and Cascode of Source Inductive Degeneration which is implemented using Ansoft Nexxim.

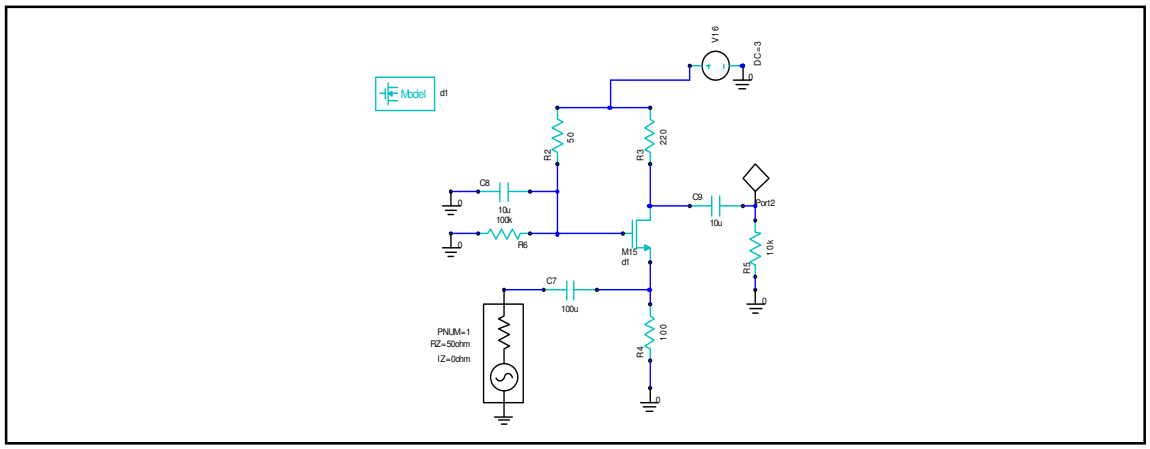

Figure 6: LNA-Common Gate Topology

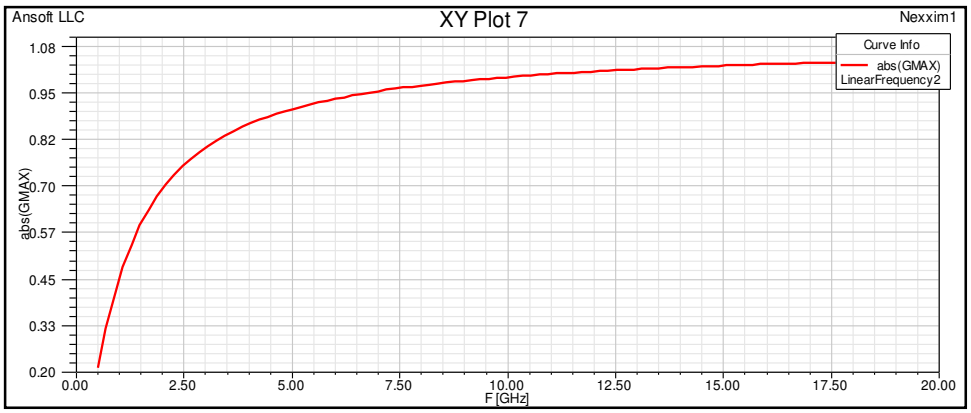

Figure 7: Gain Characteristics

2 Cascode Inductive Source Degeneration Topology Design of LNA

The achieved gain of common Gate Topology lies in the range of 0.86 dB which is very low as shown in Figure 7, hence the topology of Cascode Source Inductive Degeneration has been implemented using Ansoft designer.

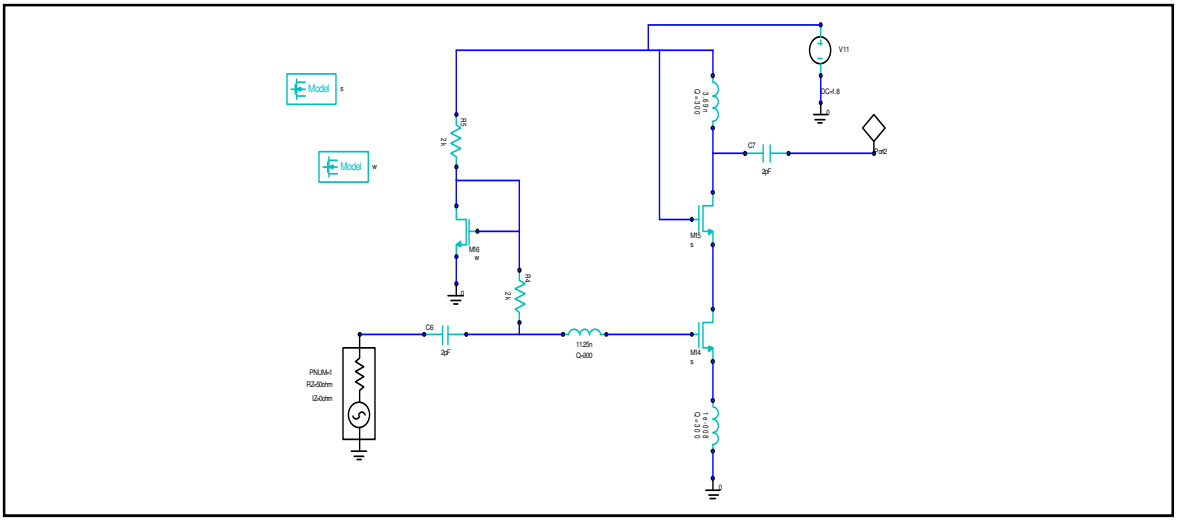

Figure 8: Cascode Inductive Source Degeneration Topology

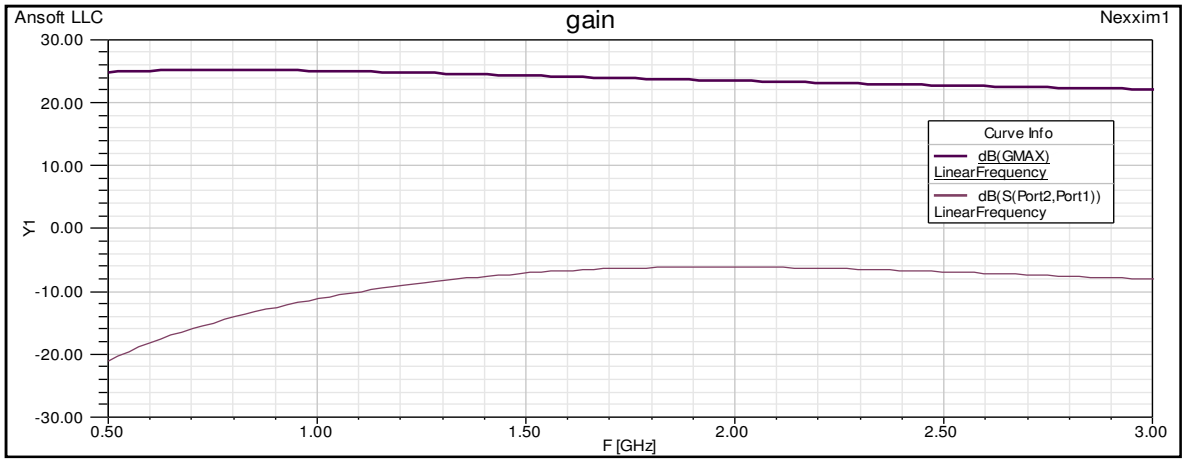

Figure 9: Characteristics of Frequency against Gain

By using Cascode Inductive Source Degeneration topology, the design has achieved a maximum gain of 24.5 dB which has been done in single-ended form as shown in Figure 9.

3. Conclusion

This paper has studied the various LNA topologies with their characteristics. The Low Noise Amplifier with Common gate as topology and Cascode inductive have been chosen and implemented using Ansoft Nexxim designer. Source degeneration has been designed for the required noise figure and gain characteristics. The simulation results show that while using the Common gate stage the resulted gain was very low achieving a value of only 0.86 dB for the specifications considered. The LNA is then designed with the cascode design of single ended form which achieved gain of 24.5 dB. This is a reasonably better gain when comparing with the common gate stage. Thus this simple analysis helps to understand the topologies of LNA and its gain characteristics.

4. References

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