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Power and Delay Reduction Using D-Latch in Carry Select Adder

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Abstract:
Carry Select Adder (CSLA) is one of the high speed adders used in many computational systems to perform fast arithmetic operations .Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Experimental analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

Key words*: Low Power, CSLA, Area Efficient, BEC, D-Latch*

1. Introduction

Design of high speed data path logic systems are one of the most substantial research area in VLSI system design. High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. The detailed structure and function of BEC. This logic can be implemented with any type of adder to further improve the speed. CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers. The modified CSLA using BEC has reduced area and power consumption with a slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by D latch with enable signal. The proposed architecture reduces the area, delay and power. This paper is organized as follows; section III presents the detailed structure and the function of the binary to excess-1 converter logic. Section IV and section V explain the regular and modified CSLA respectively. Section VI deals with the proposed architecture. The results are analysed in the section VII. Section VIII concludes

2. Literature Review

Bedriji 1962 proposes [1] that the problem of carry propagation delay is overcome by independently generating multiple radix carries and using these carries to select between simultaneously generated sums. Ramkumar et al 2010 proposed a BEC method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ramkumar and Harish 2011 [7] propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

3. Binary To Excess-1 Converter

To reduce the area and power consumption of regular CSLA, RCA with Cin=1 is replaced with BEC. An n+1 bit BEC replaces the n bit RCA. A structure of 4-bit BEC and the truth table is shown figure 1 and table 1. How the goal of fast addition is achieved using BEC together with a multiplexer (mux) is described, one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial product results in parallel and the muxes are used to select either BEC output or the direct inputs according to the control signal Cin.
The Boolean expressions of 4-bit BEC are listed below, (Note: functional symbols,
~ NOT, & AND, ^ XOR).
X0 = ~ B0 (1)
X1 = B0 ^ B1 (2)
X2 = B2 ^ (B0 & B1) (3)
X3 = B3 ^ (B0 & B1 & B2)

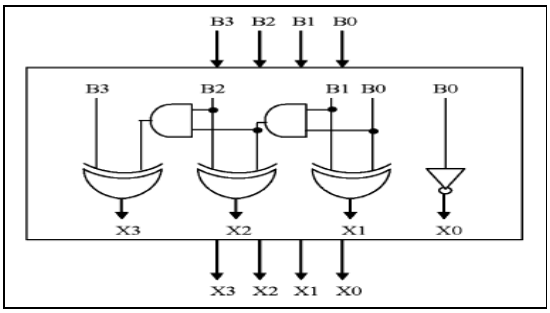

Figure 1: Struture for 4-Bit Binary to Excess-1 Code Converter

BINARY	EXCESS 1
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Table 1: Function Table Of The 4-Bit BEC

4. Regular SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Fig. 5. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 2, in which the numerals within [] specify the delay values. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer. Internal structure of the group 2 of regular 16-bit CSLA is shown Fig. 3. By manually counting the number of gates used for group 2 is 57 (full adder, half adder, and multiplexer). One input to the mux goes from the RCA with Cin=0 and other input from the RCA with Cin=1 The group2 has two sets of 2-b RCA. The arrival time of selection input c1 [time (t) = 7] of 6:3 mux is earlier than s3 [t = 8] and later than s2 [t = 6]. Thus, sum3 [t = 11] is summation of s3and mux [t = 3] and sum2 [t = 10] is summation of c1 and mux.

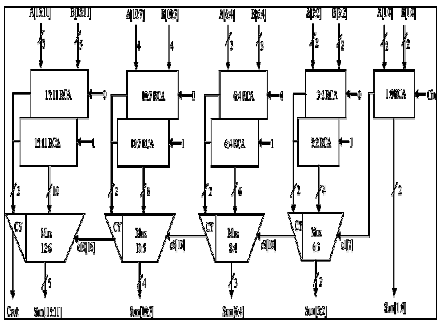

Figure 2: Regular 16 bit SQRT CSLA

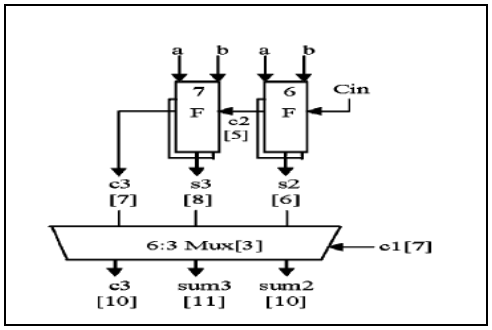

Figure 3: Group 2

5. Modified CSLA Using BEC

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The delay and area estimation of each group 2 is shown in Fig. 5. One input to the mux goes from the RCA with Cin=0 and other input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power. But the disadvantage of BEC Method is that the delay is increasing than the regular CSLA.

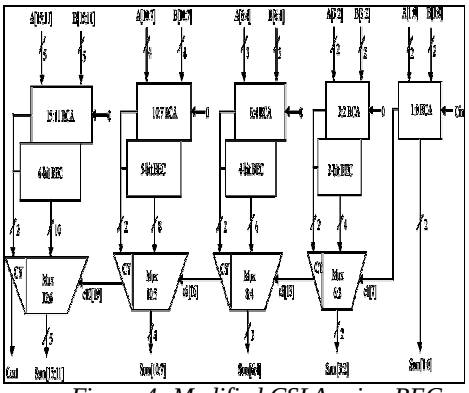

Figure 4: Modified CSLA using BEC

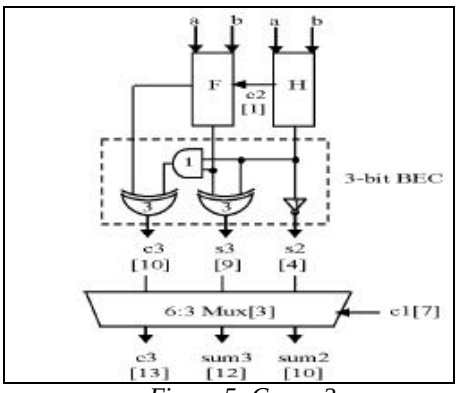

Figure 5: Group 2

6. Modified 16-Bit CSLA Using D-Latch

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch and it‘s waveforms are shown in Fig.6 &7. The architecture of proposed 16-b CSLA is shown in Fig. 8. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay.

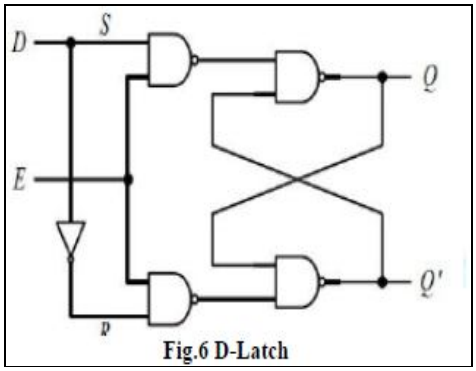

Figure 6

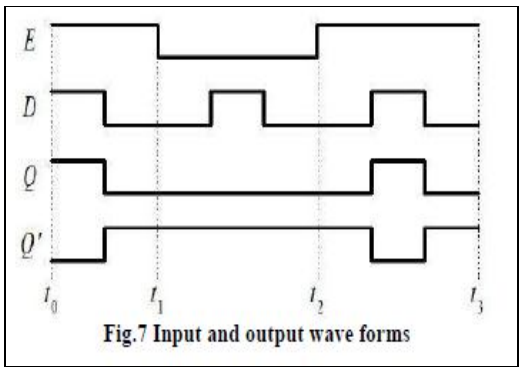

Figure 7

Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig. it can understand that latch is used to store the sum and carry for Cin=1 and cin=0.Carry out from the previous stage i.e, least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

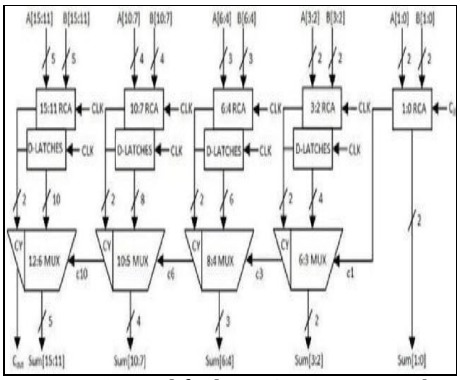

Figure 8: Modified CSLA using D-Latch

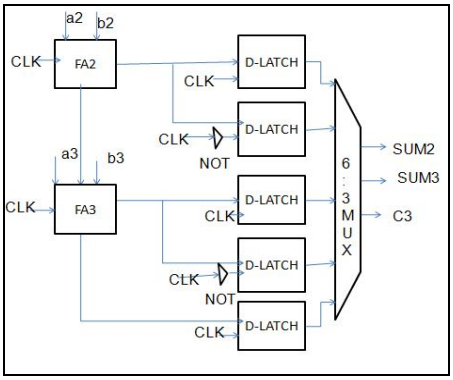

Figure 9: Group 2

The Fig.9 shows the internal structure of group 2 of the proposed 16-bit CSLA. The group 2 performed the two bit addition which is a2 with b2 and a3 with b3. This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2

structure has five D-Latches in which four are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer. When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the first D-Latch is not enabled. The second D-Latch store the sum wit c_{in} =0 by using inverted clock enable. When the clock is high, the addition is performed with carry is equal to one. The other D-Latches enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

7. Simulation Results

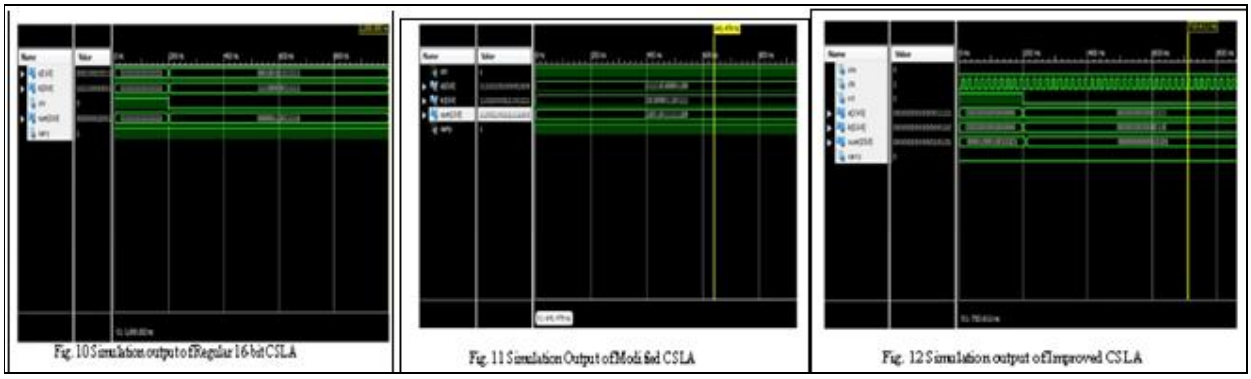

Figure 10 *Figure 11* *Figure 12*

Comparison of Regular, Modified and Improved Carry Select Adders After the observation of simulation waveforms, synthesis is performed for calculation of delay and area and thereby the speed and power of the CSLA's are calculated and a comparison of Regular, modified and improved CSLA is made in terms of delay, area and power and listed in the below table.

Parameters	Regular CSLA	Modified CSLA	Improved CSLA
No. of slice registers	28	27	32
No .of slice LUT's	28	28	40
Delay (ns)	9.704	10.276	4.185
Power (mW)	326	302	277

Table 2: Comparison Of Regular, Modified And Improved Csla

The comparison of all the three types of Carry Select Adders is made in terms of delay, area and power. Our main interest here is of the speed of CSLA and the power. Therefore compare the delay and power of the three types of Carry Select Adders [10]. From the above comparison table, we can see that delay and power of an Improved CSLA is reduced and therefore we can say that CSLA with D-latch is a High Speed Carry Select Adder.

8. Conclusion

All the three models of CSLA are designed and are implemented in VHDL using Xilinx 13.2 ISE tool and the results are compared in terms of delay and power. The CSLA with D-Latch proves to be the High Speed and Low Power CSLA. It is also implemented with vertex 5 FPGA. The performance of this CSLA in terms of delay and power is evaluated by implementing an FIR Filter by using the CSLA in the adder part and again it proves to be the High Speed and Low Power CSLA. Thus a high speed and low power FIR filter can be designed using an Improved CSLA with D-latch. The Improved CSLA architecture is therefore, high speed, low ower and efficient for VLSI hardware implementation.

9. References

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