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Comparative Analysis of Keeper Techniques for Domino Circuits

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Abstract:
Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage offered over static CMOS logic circuits. The main drawbacks of dynamic logic are lack of design automation and less tolerance to noise. In performance-critical applications, Domino logic is widely employed since it has a lower delay at the cost of reduced noise immunity, compared with static CMOS logic but still it is not preferred much for practical applications mainly due to delay variations and large power dissipation.In this work the comparative analysis of various domino keeper topology techniques for various important constraints such as power, area, speed and PDP has been done. These techniques are compared by detailed transistor simulation on benchmark circuits such as 2-bit OR gate using microwind 2 and DSCH 2 CMOS layout CAD tools.

Key words: *Domino logic,Keeper Topology,CMOS,Dynamic Logic*

1. Introduction

The rapid integration of VLSI circuit is due to the increased use of portable wireless systems with low power budget and microprocessors with higher speed. To achieve high speed and lower power consumption transistor technology and power supply must be scaled down simultaneously. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (Vth*)* is also scaled down to achieve high performance. Since reducing the threshold voltage exponentially increases the sub threshold leakage current improving noise immunity are of major concern in robust and high-performance designs in recent technology generations, especially for wide fan-in dynamic gates. As technology is scaled down, power supply must be scaled to decrease power consumption. However, this leads to degradation of noise immunity because of lowering the switching threshold voltage.

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits. Domino logic is a CMOS-based evolution of the dynamic logic techniques which is based on either PMOS or NMOS transistors. It allows a rail-to-rail logic swing and is developed to speed up circuits. Using this technique, glitch-free operation can be obtained as each gate can make only one transition. But the main problem is that of the charge distribution. The major necessity of making use of CMOS domino logic for the design of combinational logic circuits is that of low-power high speed operation.

Wide fan-in domino circuits [1] are used to design high performance register files, ALU front ends, and priority encoders in content addressable memories. Wide domino logic refers to domino logic gates with N parallel pull down branches when N is greater than 4; that are used to design circuits in the microprocessor critical path. By scaling down the technology the sensitivity of the dynamic node to the noise sources has emerged as a serious design challenge. For improving noise immunity and reducing leakage the keeper transistor is added.

The rest of the paper is arranged as follows. Section 2, studies four types of circuits that have been proposed in related literatures, weak keeper topology, VRSK keeper topology, keeper topology logic, current mirror keeper topology logic. Simulation results of different methods and compare in section 3. Conclusion in section 4.

2. Literature Review

2.1. Weak Keeper Topology

The footer nMOS transistor MN2 is connected to the source of evaluation nMOS transistor to obtain the FDL [2] design which basically reduces the leakage current. Fig.1 shows the most conventional footed domino logic circuit. When clock is low, the dynamic node is pre-charged to VDD [3]. In this phase the footed transistor MN2 is turned off, which reduces the leakage current.

When clock goes high, footer transistor MN2 is turned on. So, depending on incoming data to pull-down network the state of output node is obtained.

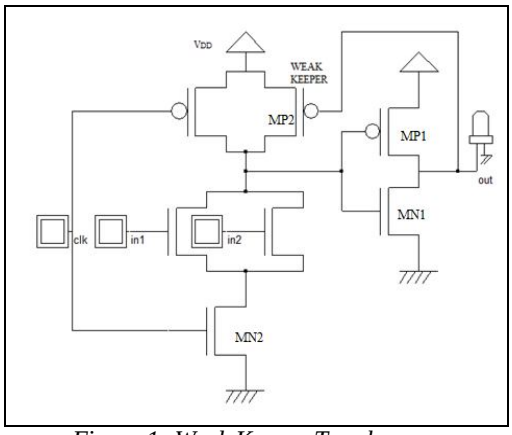

Figure 1: Weak Keeper Topology

2.2. VRSK Keeper Topology

This technique also incorporates a voltage regulated static keeper (VRSK) instead of a conventional pMOS keeper. In VRSK a self-biased Mp transistor is cascaded with the Mk transistor[4]. By using the conventional keeper circuit the contention effect occurs when the dynamic node is to be evaluated as logic '0' as the keeper and the pull down network are simultaneously on. By incorporating VRSK the transistor Mk has a lower supply voltage with a weaker strength resulting in lowering the contention effect.

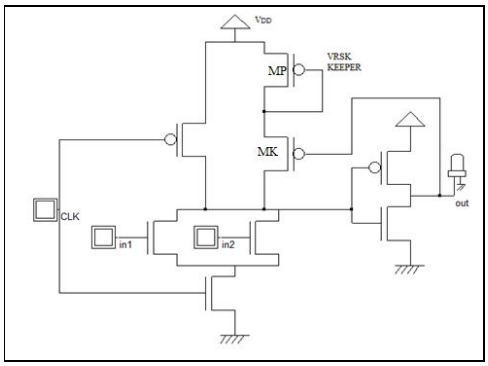

Figure 2: VRSK Keeper Topology

2.3. Keeper Topology

In the precharge phase, clock is low, the dynamic node is charged to V_{dd} by precharge transistor, output node is discharged to $V_{gnd.}$ Evaluation phase begins when the clock transitions high. Dynamic node is discharged to $V_{gnd.}$ through pull down network provided that the inputs are high. Output node is charged to VDD. In this technique the standard keeper is replaced by two keeper transistors among which the first keeper provides the resistance path and the second keeper minimizes the problem of charge sharing[5]. Since the second keeper is connected to the output node, each time when the dynamic node is charged to V_{dd} the output remains low and it turns ON the second keeper and makes the dynamic node to maintain the logic level thereby preventing charge sharing to the pull down network. Also the delay variation is reduced by means of keeper topology.

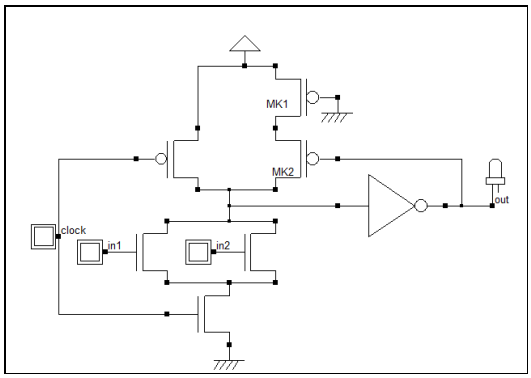

Figure 3: Keeper Topology

2.4. Current Mirror Keeper

It consists of a replica transistor whose width is a safety factor times the total nMOS pull down logic width. The gate of this transistor is connected to source and the leakage current is mirrored to the dynamic node through the pMOS current mirror transistors. This technique provides excellent tracking of the Delay[6]. The contention is still high because the keeper is strongly ON during the beginning of the evaluation phase.

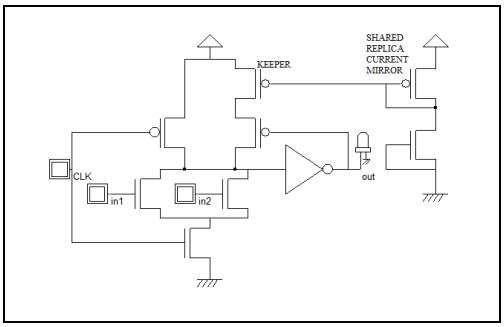

Figure 4: Current Mirror Keeper

3. Simulation Result and Performance Analysis

To assess the reduction in various constraints offered by the above discussed circuit techniques, keeper topology technique were simulated according to the test circuit for the 45-nm technology and the following results are obtained.

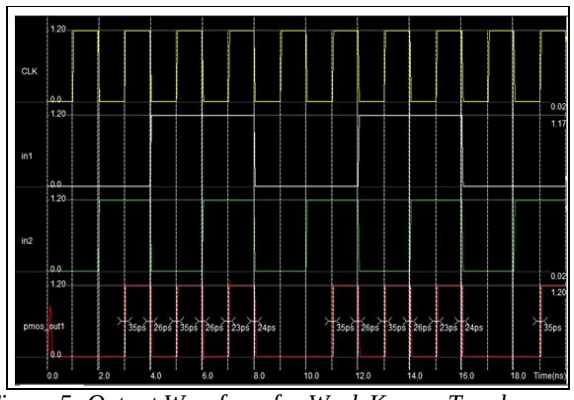

Figure 5: Output Waveform for Weak Keeper Topology

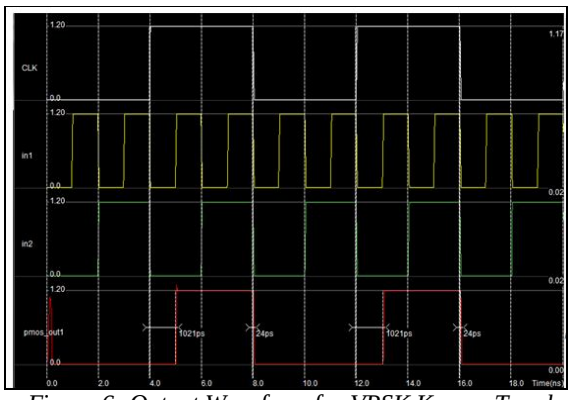

Figure 6: Output Waveform for VRSK Keeper Topology

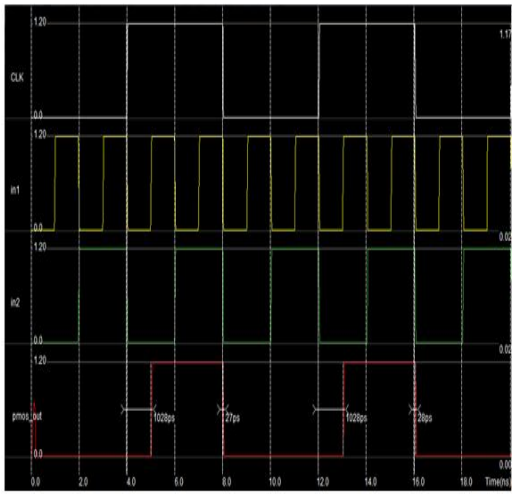

Figure 7: Output Waveform for Keeper Topology

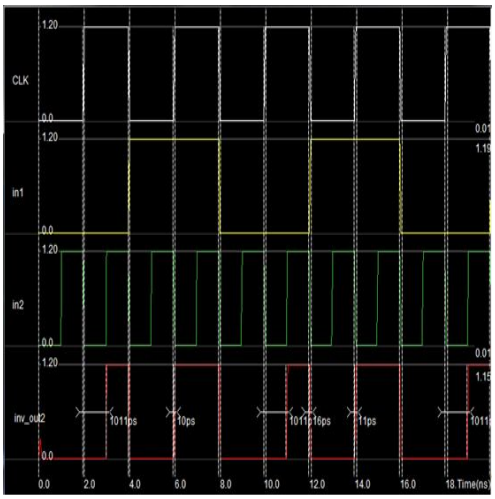

Figure 8: Output Waveform for Current Mirror Keeper

CIRCUIT TECHNIQUS	AREA (µm2)	Power (µW)	Delay (ns)	PDP (fJ)
Standard keeper	107.1	12.788	0.650	8.312
VRSK keeper	115.2	3.529	0.630	2.223
Keeper topology	115.2	4.372	0.490	2.142
Current mirror keeper	138.1	4.038	0.510	2.059

Table 1: Optimum Values For 2 Inputs Or Gate.

4. Conclusion

In this work, the benchmark circuit OR gate was successfully implemented by using CMOS technology. As it is from the results, it can be observed that the current mirror keeper technique have low PDP, VRSK keeper technique have low power, standard keeper technique have less area and in keeper topology delay is reduced.So this comparison of these different keeper techniques can make it easy for someone to choose logic design technique according to the need of design.

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5. References

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