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Designing of Differential SRAM with Improved Parameters

Loknath Kumar Patel
M. Tech Student, Department of ECE
Ajay Kumar Garg Engineering College, Ghaziabad, UP. India
Monika Gupta
Assistant Professor, Department of ECE
Ajay Kumar Garg Engineering College, Ghaziabad, UP. India

Abstract:
This paper represent a technique for a designing differential 6T SRAM with improved parameters. In SRAM designing Lowering power consumption and increasing noise margin have become two essential topics every state of art. Static RAM (SRAM) is a form of memory that holds data in the form of static. Refreshing is not requiring in the SRAM circuit. Reduction of operating voltage in SRAM degrades the stability of the cell. Our 6T SRAM is proposed design in which we have calculated, Read Margin (RM); Write Margin (WM), Power consumption with temperature or without temperature. It also consumes less power when compared to the 8T SRAM design. It provides the improved write margin, read margin when compared to the other SRAM designing. The simulation has been carried out on 180 nm CMOS technology. Tanner EDA tool used for simulation

Keyword: *Low power, SRAM, Read Margin, Write Margin, Power consumption*

1. Introduction

In the last decade, LOW-POWER and high-stability have been the main themes of SRAM designs [1]. The explosion of the portable electronic market constantly urges for less power-hungry architectures. Today Static Random Access Memory (SRAM) continues to be one of the most fundamental and critically important memory technologies. Modern digital systems have need of the capability of storing and retrieving large amounts of information at high speeds. Memories are systems or circuits that store digital information in huge quantity [2]. Therefore, semiconductor memory arrays capable of storing big quantities of digital information are important to all digital systems. In a broad sense, memory can be divided as mass storage memory main memory. The main memory is usually the random access type. The Random Access Memory (RAM) is the one in which the time required for writing (storing) the information and for reading (retrieving) information is independent of the physical location (within the memory) in which the information is stored [3]. In other words, RAM refers to the type of memory in which any bit of data may be accessed at any time irrespective of its position in memory [4]. RAM is also called as Read-write memory (RWM) because both write and read operations can be performed. RAM may store information in flip-flop style circuits or generally as charge on capacitors [2]. Because write-read memories store data in energetic circuits, they be volatile; that is, stored information is lost when the power provide is broken up.

The type of RAM which is regularly used in VLSI integrated circuits is the simply SRAM or Static Random Access Memory. Static RAMs hold the stored value in flip-flop circuits as long as the power is on. Static Random Access Memory tends to be high-velocity memories with clock cycles in the range of 5 to 50 ns [2]. Along with the a range of configurations available for implementing the SRAMs, full CMOS SRAM cells are presently most popular due to the lowest static power dissipation and high speed among the a variety of circuit configurations and compatibility with current logic process [4]. Due to this reason SRAMs not only occupy a significantly large segment of modern SoCs but also hold a major content in ASIC domain. Therefore, understanding SRAM design and operation is crucial for attractive a range of aspects of chip design and manufacturing. This work includes the study and implementation of Designing of Differential SRAM with Improved Parameters.

2. 6T Static SRAM (SRAM) Design

The 6T SRAM cell is two cross-coupled inverters (i.e. per inverter two transistors) arranged in a logic loop with a pair of pass transistors. The access transistors are connected to the word line at their respective gate terminals, and the bitlines at their source/drain terminals. Fig 1 shows the Schematic 6T SRAM design. Table 1 Summary of the 6T SRAM design circuit**.** The word line is used for select the cell while the bitlines are used for absolute read or write operations on the cell. Within, the cell holds the stored value on one side and its complement on the other side. Suppose that node Q holds the stored value while node holds its complement. The two complementary bitlines are used to get better speed. The VTC of cross-coupled inverters is shown in Fig 2. The VTC conveys the answer cell design considerations in favor of read and write operations. During the cross-coupled design, the stored values are shown by the two balanced states in the VTC. The cell will preserve its current state until one of the

internal nodes crosses the switching threshold. This when occurs, the cell will flip its internal state. for this reason, during a read operation, we have to not disturb its present state, while for the duration of the write operation we be required to force the internal voltage to fall past V_{DD} to change the state.

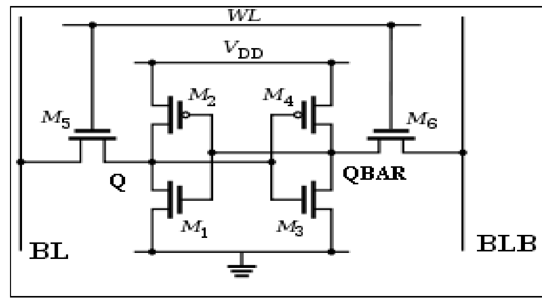

Figure 1: Schematic 6T SRAM Design

Name of Transistor	Type of Transistor	Operate	Length(L)	Width(W)
M_1	NMOS	DRIVER	180 nm	600 nm
M_3	NMOS	DRIVER	180 nm	600 nm
M_6	NMOS	ACCESS	180 nm	600 nm
M_5	NMOS	ACCESS	180 nm	600 nm
M_2	PMOS	LOAD	180 nm	300 nm
M_4	PMOS	LOAD	180 nm	300 nm

Table 1: Summary of the 6T SRAM design circuit

Pull up ratio is a ratio between sizes of the load transistor to the access transistor during write operation. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation. The stability of the cell depends on the cell ratio and it depends on the driver of the transistor. Speed of the SRAM cell depends on the driver of the transistor. Speed of CMOS SRAM is directly proportional to the cell ratio.

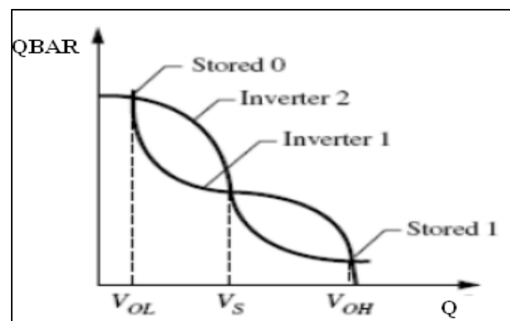

Figure 2: VTC of 6T SRAM cell

Pull Up Ratio = (W4/L4) / (W6/L6) (During Write Operation)
Cell Ratio = (W1/L1) / (W5/L5) (During Read Operation)

3. Operation of SRAM Circuit

There are three types of operation happen in SRAM circuit.

3.1. Write Opration

The start of a write cycle begins as a result of applying the value to be written to the bit lines. If we wish in the direction of write a 0, we would apply a 0 to the bit line, i.e. setting BL to 0 and BLB to 1. Assume WL to 1, Q to 1 QBAR to 0 Fig 3 shown the 6T CMOS SRAM during write '0' operation. Fig 4is the corresponding wave forms for Q and QBAR. Now, again I am setting WL to 1, BL to 1, BLB to 0, Q to 0 and QBAR to 1. Then corresponding circuit diagram are shown in the fig 5.

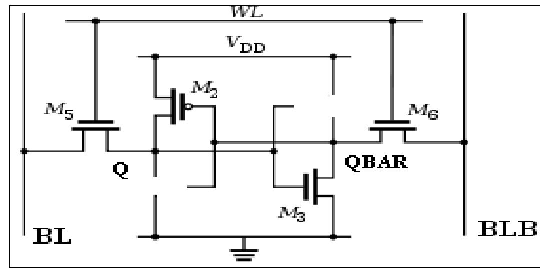

Figure 3: 6T CMOS SRAM cell during write ‘0’ operation

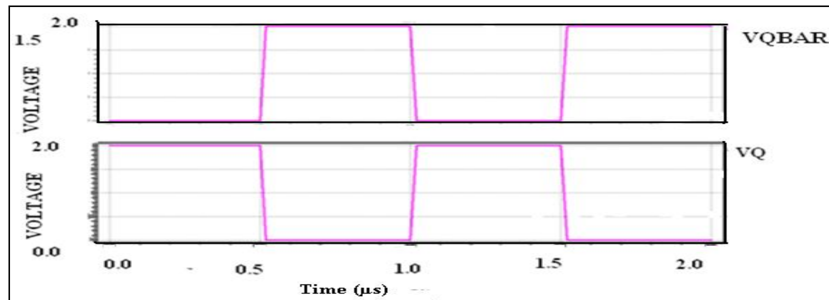

Figure 4: Write operation wave form for Q and QBAR

3.2. Read Operation

Assume that the content of the memory is a 1, stored at node ‘Q’. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line signal with the high voltage pulse enabling both the cut-off transistors. The second step occurs when the values stored in Q and QBAR are transferred to the bit lines, one of the bit lines will discharge through the driver transistor and the other bit line will be pulled up through the load transistors in the direction of V_{DD}, a logical 1. Read operation of the waveform BL and BLB shown in the fig 6.

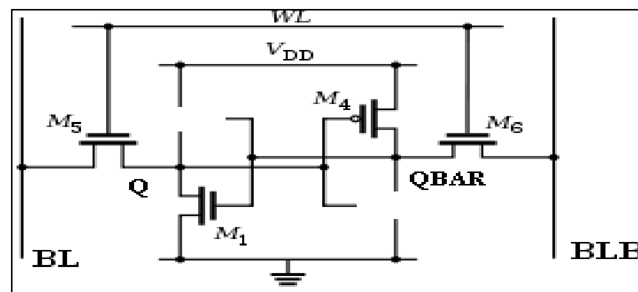

Figure 5: 6T CMOS SRAM cell during write ‘1’ operation

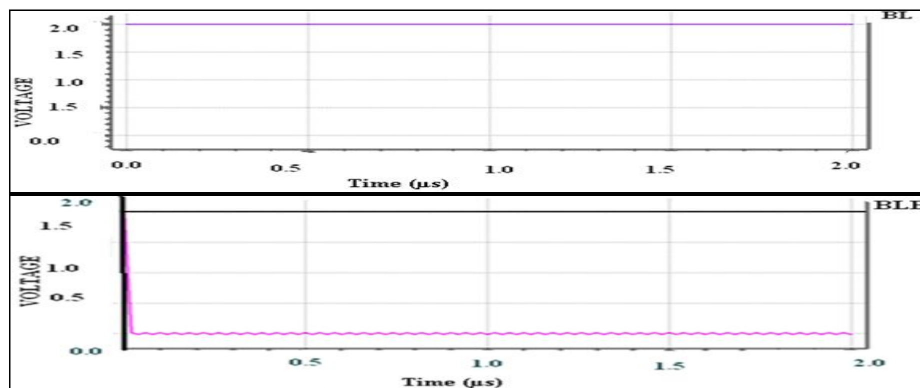

Figure 6: Read operation wave form for BL and BLB

3.3. Standby Opeartion

If the word line be not asserted, the access (Pass) transistors will dis-connect the cell from the bit lines. Then two cross coupled inverters created the two inverter coupled back to back reinforce each other as long as they are disconnected from the outer world. And they will save the data which they have before now stored in the memory cell.

4. Performance Matrices of SRAM cell

4.1. Power consumption with Temperature or without Temperature

Power consumption is defined as the rate of energy transfer, Power consumption or lost from electrical structure. When an electrical current does not job on a conductor the inside energy of the conductor increases causing its temp. To get higher exceeding the ambient temperature. The total power consumption of a circuit includes together a dynamic and a static element that can be not easy to isolate from every one other in simulations. Table 2 summarized the power supply voltage (V_{DD}) v/s power consumption without temperature and table 3 summarized the power consumption v/s power consumption with temperature.

Supply voltage(V_{DD})	Power consumption
2.0 V	852.5 µW
1.8 V	436.1 µW
1.6 V	268.2 µW
1.4 V	203.2 µW
1.2 V	106.7 µW
1.0 V	7.55 nW
0.8 V	1.68 nW

Table 2: Supply Voltage V_{DD} v/s Power consumption without Temperature

V_{DD}(V)	Temperature(°c)	POWER CONSUMPTION(µW)
2.0	36	835
2.0	33	840
2.0	30	844
2.0	27	849
2.0	24	854
2.0	21	858
2.0	18	862

Table 3: Supply Voltage V_{DD} v/s Power consumption with Temperature

4.2. Write Margin

Write margin is defined as the lowest bit line voltage essential to flip the state of an SRAM cell [1]. The write margin significance and variation is a function of the cell design, SRAM arrangement size and procedure variation. Table 4 summarized the power supply voltage v/s write margin and equivalent Graphical representation of supply voltage (V_{DD}) v/s Write Margin shown in the Fig 7.

Pull up ratio is directly proportional to the write margin. Its value increases with the increases the value of the pull up ratio. Its value depends upon the pull up ratio. So watchfully we have to design SRAM cell inverters prior to calculating the write margin of SRAM cell during write operation. Pull up ratio also totally depends on the amount of the transistor.

V_{DD} (V)	Write Margin
2.0	115 mV
1.8	113 mV
1.6	112 mV
1.4	111 mV
1.2	94.9 mV
1.0	62.2 mV
0.8	52.6 mV

Table 4: Power supply voltage v/s Write Margin

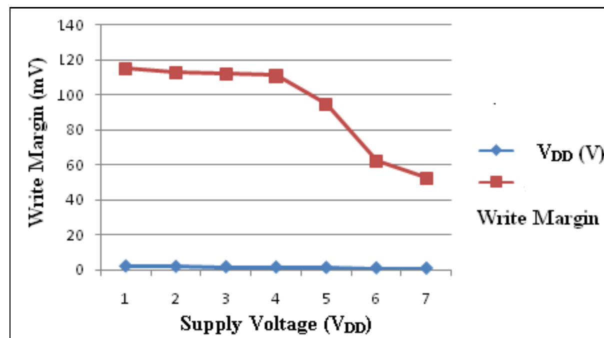

Figure 7: Graphical representation of supply voltage (V_{DD}) v/s Write Margin

4.3. Read Margin

Read margin depend on the cell ratio. Having directly proportional to the cell ratio. Their values increase with increases the value of pull up ratio. So carefully we have to design SRAM cell inverters prior to calculating the read margin of SRAM cell during read operation. Pull up ratio also totally depends on the size of the transistor. The process of analysis of read margin is matching as the analysis of static noise margin. Table 5 summarized the supply voltage (VDD) v/s read margin and the corresponding graphical representation shown in the fig 8.

VDD(V)	Read Margin(mV)
2.0	427.49
1.8	397.49
1.6	365.48
1.4	230.34
1.2	200.48
1.0	177.27
0.8	155.32

Table 5: VDD V/S Read Margin

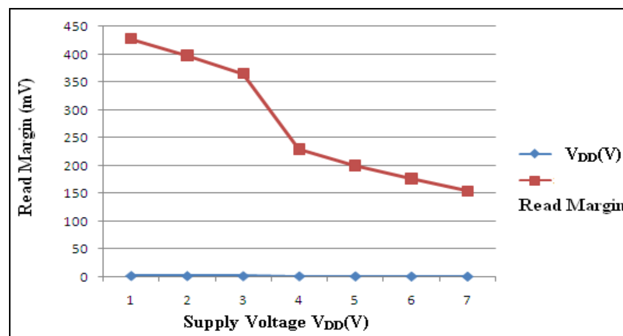

Figure 8: Graphical representation of supply voltage (vdd) v/s read margin

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6. Conclusion

A fully differential 6T SRAM circuit has been proposed and analyzed. The proposed design has improved both static noise margin and write margin. We have also analyzed improved version of read margin and lowering power consumption with temperature or without temperature. The simulation result shows that much better noise margin and lower power consumption with temperature and without temperature using the conventional 6T SRAM design. Simulation of 6T SRAM cell has been done for 180nm CMOS Technology.

7. References

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