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Predictive simulation of Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs

Vijayeta Kumari
M. Tech Student, Department of Electronics and Communication Engineering
B.S.A. Institute of Technology and Management, Faridabad, Haryana, India
Anju Ravish
Lecturer, BSAITM, Faridabad, Haryana, India
Indrash Babbar
Head, Department of ECE, BSAITM, Faridabad, Haryana, India

Abstract:
In this paper, a triple-material cylindrical gate-all-around(TM-CGAA) MOSFET is proposed and an analysis of its natural length based on center potential is presented by means of 3D TCAD simulations. This paper provides contrast between the estimation of the natural length using surface potential and the use of center-potential based natural length formulation for an accurate subthreshold analysis. The effects on the threshold voltage and DIBL due to the device parameters like the cylinder diameter, oxide thickness, gate length ratio, etc., are also examined.

1. Introduction

The 20th century marked the beginning of an era of miniaturization of computer and hand held gadgets with every possible application. It became possible by a process known as 'Scaling'.But as the MOS dimension attained its physical limit, the scaling beyond 22-nm node became an almost impossible task. This enforced VLSI engineers to look beyond the conventional MOSFET structure and design new ones. The degree of Gate controllability started gettingbetter and better with newer devices being developed like FinFET, Omega/Pi Gate MOSFET and Gate-All-Around (GAA).As the MOS structure is continued to be scaled down, a lot of undesired effects like SCE and DIBL also come into play.

One of the prominent means to get rid of SCE is by using cascaded gate structure consisting of two or more metals of different work functions. This structure is commonly known as Double-Material-Gate (DMG) or Triple-Material-Gate (TMG). The metal gates are so cascaded that the gate near the drain is a metal with lower work-function and the source side metal is of relatively higher work function. As a result of this, the electron velocity and the lateral electric field along the channel increases sharply at the interface of the two gate material which further results in the increased gate transport efficiency. In the present work, it has been demonstrated that the channel forms at the Si body center first than at the surface. Thus, formulation centre potential is more worthy than the surface potential. The natural length derived through centre potential will be more accurate than that at surface. A rather simplified method has been adopted to derive the device characteristics employing parabolic potential approximation in the channel.

2. Short Channel Effects

2.1. Hot Carrier Effects (HCE)

Hot-carrier (HC) degradation affects reliability, increases SCE and causes long-term instability, manifested by a threshold voltage decrease and sub-threshold drive current increase. The high electric field near the drain creates hot carriers which are injected into the oxide with enough energy to create defect states (traps) in the oxide near the silicon/oxide interface.

2.2. Mobility Degradation

For a planar bulk MOSFET, continuous scaling requires continuous increase in the channel doping (N_a). This is because it is desired to have a lower junction electric field in the channel region. Also higher doping ensures non-overlap of the source and drain depletion in the channel. But a serious effect of mobility degradation due to the impurity scattering comes in play with higher amount of channel doping. Also the threshold voltage variations take place due to random dopant fluctuations inside the channel.

2.3. Quantum Effects

Scaling the oxide leads to strong surface electric field near the silicon/oxide interface creating a potential well and leading to quantum confinement of the inversion carriers, giving rise to discrete sub-bands for motion in the direction perpendicular to the interface and shifting the peak of the inversion charge centroid away from the interface. The confinement decreases the inversion charge density at a given bias, increases the effective oxide thickness and increases the threshold voltage.

2.4. Drain Induced Barrier Lowering (DIBL)

As the lateral dimensions are scaled, the source/drain channel p-n junction depletion width becomes significant in comparison to the channel length leading to loss of gate control over the channel. An increase in drain voltage leads to further penetration of the drain-induced field into the channel of the transistor, reducing the lateral potential barrier that is typically controlled by the gate. This effect is termed drain induced barrier lowering (DIBL).

3. Device Structure

The cross sectional diagram of the fully depleted TM-GAA MOSFET structure used for modelling and simulation is shown is shown in Fig. 1. The radial and lateral directions are assumed to be along the radius and the z- axis of the cylinder as shown in the Fig. 1. The surrounding metals divide the entire channel region into three regions named as region I, II and III as shown in Fig. 1. The lengths of the three regions connected in a non-overlapping way are symbolized as L_1, L_2 and L_3. The device has uniformly doped source/drain with doping density of $N_D = 1x10^{20}cm^{-3}$. The channel is kept lightly doped with doping density of $N_A = 1x10^{16}cm^{-3}$. The gate oxidethickness and the diameter of the silicon pillar are t_{ox}= 2nm and t_{Si}=40 nm respectively. The work function of the gate materials in decreasing order from source to drain are: Ψ_1= 4.8eV (e.g., Au), gate material 2 with Ψ_2= 4.6 eV (e.g., Mo), and gate material 3 with Ψ_3= 4.4 eV (e.g., Ti).

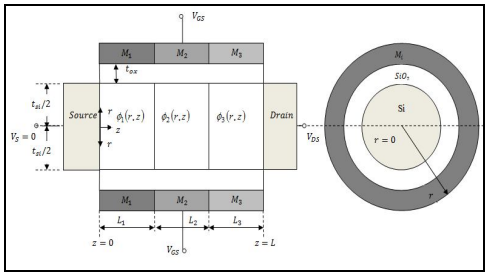

Figure 1: Cross-sectional view and side-view of the TM-GAA MOSFET

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