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Efficient Quantum Dot Cellular Automata Adder Using Five Input Majority Gate

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Abstract:
Transistor can be accommodated more and more in single die due to its smaller size but however transistor cannot get smaller than its current size. One of the possible solutions to overcome this physical limit is quantum dot cellular automata (QCA) approach. In QCA, the previous adders are designed using three input majority gate (MG). In this project, a novel quantum-dot cellular automata adder is designed using five input majority gate. Here we apply the Majority logic method for constructing QCA. The designed adder is implemented in FIR and IIR filter. The power and total gate count can be analyzed by using the Xilinx software. The performance analyses of this adder are compared with adder designed using three input MG.

Key words: *Quantum dot cellular automata (QCA), majority gate (MG), five input majority gate*

1. Introduction

A quantum-dot cellular automaton is an emerging nanotechnology that promises low-power high-performance digital circuits [1]. For this reason the designing of logic circuits in QCA draws much attention nowadays. The fundamental arithmetic operation is addition and several kinds of different logic styles are used in designing arithmetic circuits [2] – [8].

The architecture exploited in conventional CMOS designs is viewed as basic reference for the QCA design structure. The QCA design for carry look-ahead (CLA), Ripple carry adder (RCA), and Conditional sum adder are described in [11].The Carry flow adder presented in [12] was majorly an developed RCA in which harmful wire effects are alleviated. The major effectual structures for CLA and Brent-Kung adder (BKA) were presented in [5] and in [9].

In this concise progressive technique is described to implement high performance adders in QCA. Three new theoretical formulations for CLA and parallel –prefix adders were described in [15].These adders allow carry to propagate to consequent bit positions. In addition, the architecture at the top level leads directs to concise layouts avoiding redundant clock cycles. The designed adder runs in same manner as RCA runs but computational delay is lower than RCA and achieves less are-delay product. The rest of concise is arranged as follows: brief description of the QCA technology is given in section 2 and previous adder designed in QCA is given in section 3, proposed work is introduced in section 4 and simulations results are described in section 5 and conclusion is presented finally in section 6.

2. Background

A QCA is a nanostructure and the basic cell of QCA consists of four quantum dots in which two quantum dots are occupied by free electrons. Thus each cell contains two electrons. Electrons are arranged opposite to each other due to Coulombic repulsion [1]. The two possible binary states 1 and 0 are determined by arrangements of electrons inside the cell. Binary numbers are encoded inside the cell such that each QCA represent binary information.

Due to electrostatic forces nearer cells interact and likely to adjust their polarizations, QCA cells do not have inherent data movement. To control the direction of data flow cells in QCA design are divided into clock zones. Each clock zone corresponds to four clock signals and each clock signal is phase shifted by 90º. This makes the QCA design constitutionally pipelined such that clock zone acts like D-latch [8].

3. Novel QCA Adder Based On 3-Input Majority Gate

In conventional QCA method, full adder requires five MG and three inverters but in novel QCA method full adder requires only three MG and two inverters.

3.1. Majority Gate

In QCA design, both logic structure and interconnections are made of QCA cells that can utilize the bridge technique [2]. The fundamental logic gates of QCA technology are majority gate (MG) and inverter. The logic function of MG for three inputs A, B, C is reported in (1).

M(ABC) = A.B + B.C + A.C (1)

The input cell belongs to the same clock signal. The three input majority gate is shown in Figure. 1.

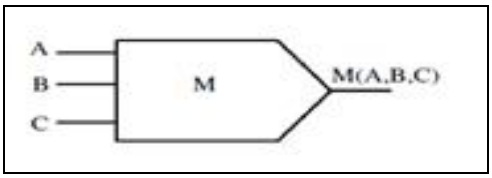

Figure 1: Three input Majority gate

The majority gate function as both AND and OR gate. When third input is 0 the MG act as AND gate and produces generate term and when third input is 1 the MG acts as OR gate and generates propagate term. The corresponding equations are reported in (2) and (3).

MG (A; B; C) = A.B when C = 0 (2)

MG (A; B; C) = A+B when C = 1 (3)

3.2. Full Adder Based on 3-Input Majority Gate

The full adder based on three inputs MG is shown in Figure. 2. The n-bit adder is designed using three inputs MG. To implement ripple adders in QCA, the novel architecture is used. In novel architecture three input MG is used.

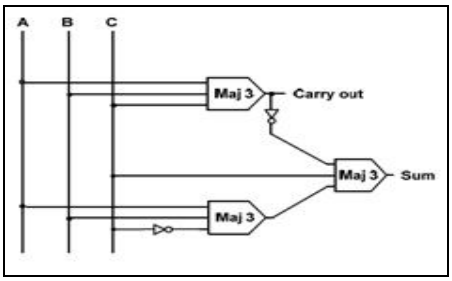

Figure 2: Full adder schematic

Consider ith bit stage for given n-bit addends

X =$x_{n-1}\ldots x_0$ and Y =$y_{n-1}\ldots y_0$ then propagate term P_i =x_i + y_i and generate term G_i =x_i . y_i are obtained. At (i-1)th bit position the first carry is generated. The conventional CLA logic given in (4) is used to compute carry. The last mentioned can be rewritten as reported in (5) by using Theorem 1 and 2 explained in [15]. In this way the circuit operates in RCA fashion and only one MG is needed to propagates the carry to consequent bit position. But in conventional circuits, two cascaded MGs are required to perform the same operation. In other words the novel QCA adder has worst case path nearly half when compared to conventional QCA design.

$c_{i+2} = g_{i+1} + p_{i+1} \cdot g_i + p_{i+1} \cdot p_i \cdot c_i$ (4)

c_{i+2} = M(M(x_{i+1}, y_{i+1}, g_i) M(x_{i+1} , y_{i+1})c_i) (5)

To design novel 2-bit module shown in Figure. 3 the equation (5) is used and the carry c_{i+1} =M ($p_i g_i c_i$) is obtained.

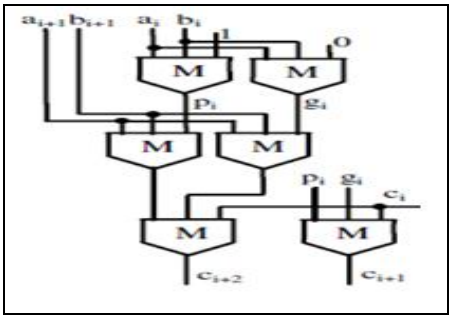

Figure. 3: Novel 2-bit module

The cascading of n/2 2 bit modules gives n-bit adder and it is shown in Figure. 4. Initially carry-in of the adder is considered as 0 and initial propagate term p_0 is not considered. The module used at least significant bit position is made simpler. The carry bits are generated first and sum is generated finally by taking carries generated as input and it is shown in Figure. 5.

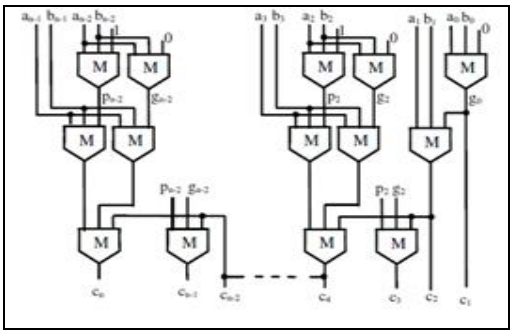

Figure 4: Novel n-bit adder generating carry

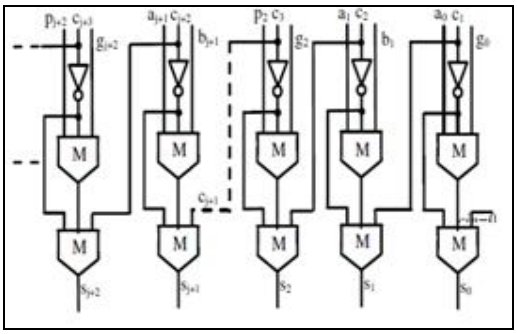

Figure 5: Novel n-bit adder generating sum

The carry is generated at least significant bit and the generated carry is propagated to consequent bit positions to most significant bit. The designed adder is applied in 4-tap FIR and IIR filter.

3.3. Area And Power Analysis

QCA Adder using 3-input MG	Peak Memory Usage (MB)	Maximum combinational path delay (ns)	Power consumption (W)
Adder	455	11.488	3.314
Adder in FIR filter	497	12.844	7.390
Adder in IIR filter	534	13.606	8.021

Table 1: Area and power analysis of existing adders

4. Proposed Work

The designing of QCA adder is simplified by using 5-input majority gate which reduces the total gate count required.

4.1. Novel Design for 5-Input Majority Gate

A five input majority gate contains 5 input and 1 output and it is shown in Figure. 6. The logic function of the 5-input majority gate voter is reported in (6) and truth table is shown in Table 1.

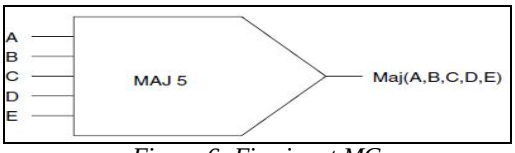

Figure 6: Five input MG

M (A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE (6)

∑ (A, B, C, D, E)	M (A, B, C, D, E)
0	0
1	0
2	0
3	1
4	1
5	1

Table 2: Truth Table Based on Sum of Inputs of 5-Input Majority Gate

4.2. Full Adder Based on 5-Input MG

Full adder designed using 5-input majority gate require only three gates (3-input MG, 5-input MG and one inverter). So the number of gates count required is reduced which in turn simplifies the QCA adder design. Thus full adder shown in Figure 7 requires only two MG and one inverter. The designed full adder using 5-input MG has reduced the number of majority gates and inverter which in turn reduced the complexity of the previous design.

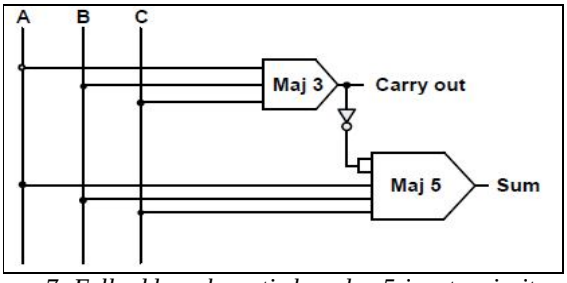

Figure 7: Full adder schematic based on5-input majority gate

4.3. Novel QCA Adder Based on 5-Input Majority Gate

The designing of QCA adder using five input majority gate reduces the total gate count required which in turn reduces the area required. Here 128-bit novel adder is designed using 5-input majority gate and the designed adder is implemented in FIR and IIR filter and simulated using Xilinx software. The obtained result is compared with adder designed using 3-input majority gate.

5. Simulation Results and Discussion

5.1. Simulation Result of FIR filter

The designed adder is implemented in FIR filter and simulation result is shown below in Figure 8.

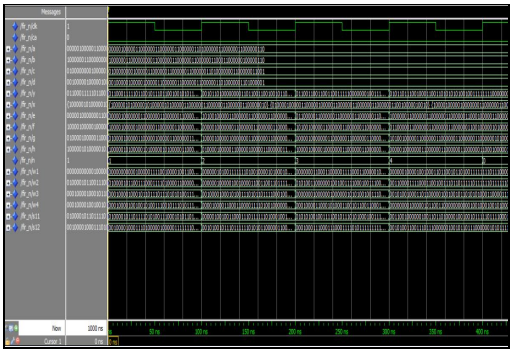

Figure 8: Simulation result of FIR filter

5.2. Simulation Result of IIR Filter

The designed adder using five input majority gate is implemented in IIR filter and simulation result is shown below in Figure 9.

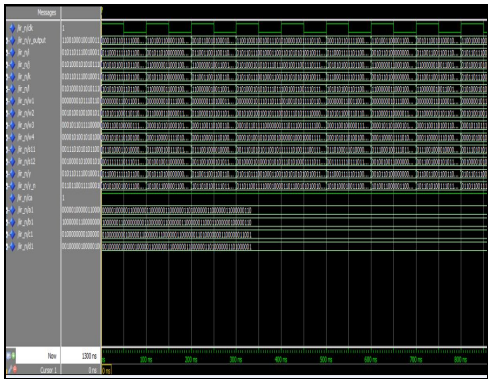

Figure 9: Simulation result of IIR filter

5.3.Area and Power Analysis

QCA Adder using 5-input MG	Peak Memory Usage (MB)	Maximum combinational path delay (ns)	Power consumption (W)
QCA Adder	454	8.946	3.202
Adder in FIR filter	483	9.795	5.351
Adder in IIR filter	524	21.342	6.073

Table 3: Area And Power Analysis of Proposed Adders

6. Conclusion

In this work, QCA circuits are designed taking advantage of the QCA logic. The designed adder is compared to previous work in this area. The adder designed using five input majority gate requires less gate therefore the total area required is less. The total power consumption is also less.

7. References

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