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New Control Strategy to Reverse the Power Flow in the Looped Electrical Distribution Network

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Abstract:
The distributed generators are very essential now-a-days due to power crisis. Generally distributed generators are connected in radial system. These radial systems are converted to looped or meshed network for improving the power transfer capability. So we are in need of power electronics converters for the injection of power. Here a static series synchronous Compensator (SSSC) can be used to do the same. So this type of SSSC is called D-SSSC. This scheme uses a Cascaded multi- level inverter which neglects the transformer and gives good efficiency. The looped network sometimes will be reversed the power flow operation. That time, the phases current are not considered in the earlier current phase locked loop control. Using voltage phase locked loop, current phase locked loop control can be neglected. Here in this proposed project work the voltage phase locked loop and current phase locked loop are presented and comparative study is shown using simulink. The existing control strategy that is VPLL is dealt with PI controller. But it has some disadvantages like maximum overshoot, harmonics and more oscillation and settling time. In order to reduce these disadvantages the PID controller is used and a compared and presented for PI and PID controller in D-SSSC cascaded H-bridge to reverse the power flow.

Key words*: Distributed static series synchronous compensator (DSSSC), Cascaded H-bridge, power flow control, phase locked loop (PLL), Proportional Integral (PI), Proportional Integral Derivative (PID) controller*

1. Introduction

In this paper investigation is done on benefits of looping the conventional radial distribution system by a series power electronic system to control power. Due to the deregulation of electrical system the conventional radial electrical distribution system will change to loop or even meshed system and connection of Distributed Generation to Medium and Low voltage in future. Controlling the power flow between two feeders from different substation by placing a D-SSSC in the connection point will be having advantages like voltage regulation, increasing reliability, loss reduction, avoiding congestion in cables and facilitating use of distributed generation. Distribution Static Synchronous Series Compensator (D-SSSC) is able to control the power flow between two feeders from different substations. Thanks to use the multilevel converter topology, to omit the bulky transformers cascaded D-SSSC is connected directly to the line. Cascaded H-bridge is the best option for this kind of realization. Controlling the power flow in new configuration of electrical distribution system is source of advantages. One of the great impacts of D-SSSC is balancing the power flows of connected feeders, avoiding congestion of feeders and cables damages. The energy for customers is produced in large power plants which are distributed all over the electrical system in the conventional network. As shown in Fig. 1 the electrical network is divided in 3 parts which are the generation system, transmission system and distribution gird. By restructuring the electrical network and government supports for Distributed Generation, many new small DGs start to feed electrical network, which most of them are connected directly to medium voltage level.

Fig. 2 shows the scheme of future electrical network. In this network conventional radial distribution system is changed to meshed and looped system [1], DGs play an important role in producing energy. Whereas the power electronic devices are used to manage the power flow in the new network. In spite of the future needs of the meshed distribution system Structure, changing the available conventional radial system to a Looped Power Flow Controlled (LPFC) structure is the source of many advantages. For looping the conventional radial system and controlling power flow a *Distribution Static Synchronous Series Compensator* (D-SSSC) can be used to connect two different feeders together.

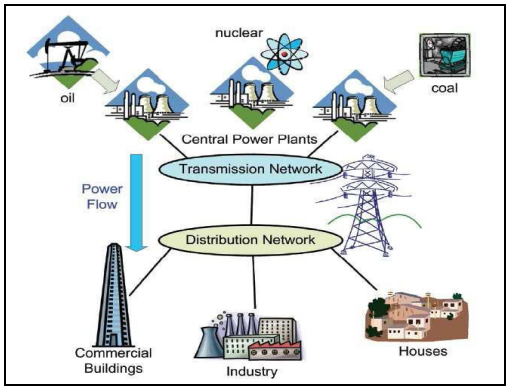

Figure 1: Conventional Electrical Network

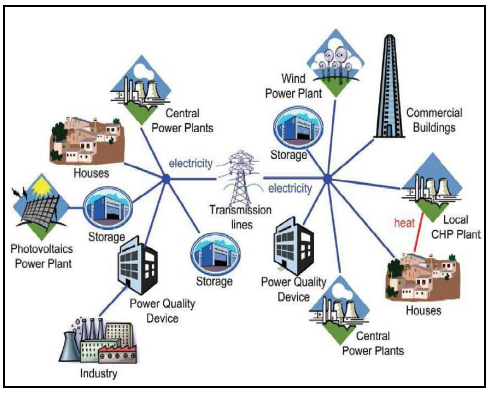

Figure 2: Future Electrical Network

2. Distribution Static Synchronousseries Compensator System Modeling

The conventional radial electrical distribution system will change to loop or even meshed system due to the deregulation of electrical system and connection of Distributed Generation to Medium and Low voltage in future. Controlling the power flow between two feeders from different substation by placing a D-SSSC in the connection point will be source of many advantages. These advantages will be voltage regulation, increasing reliability, loss reduction, avoiding congestion in cables and facilitating use of distributed generation. The main principle of D-SSSC operated without an external electric energy source as a series compensator whose output voltage is in quadrature and controllable independently of the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted active power. The D-SSSC may include transiently rated energy storage or energy absorbing devices to enhance the dynamic behavior of the power system by additional temporary real power compensation, to increase or decrease momentarily, the overall resistive voltage drop across the line [3].

Fig 3 Shows a simple transmission line with an inductive reactance (XL) Connecting a sending-end voltage source (Vs), and a receiving-end voltage source (Vr) respectively. The single line diagram of a simple transmission line real and reactive power (p and Q) flow at the receiving end voltage source are given by the expressions. Vs are the voltage magnitude of machine-1. Vr is the voltage magnitude of machine-2.□s and □r are the phase angles of the voltage sources VS and Vr, respectively. □□is the phase difference between these voltages. For simplicity, the voltage magnitudes are chosen such that VS = Vr = V and the difference between the phase angles is □= □s-□r. D-SSSC acts as capacitive impedance in two times of operation.

$$P = \frac{V_S V_R}{X_L}\sin(\delta s - \delta r) = \frac{V^2}{X_L}\sin\delta \quad \text{-------- (1)}$$

$$Q = \frac{V_S V_R}{X_L}(1 - \cos(\delta s - \delta r) = \frac{V^2}{X_L}(1 - \cos\delta) \quad \text{------- (2)}$$

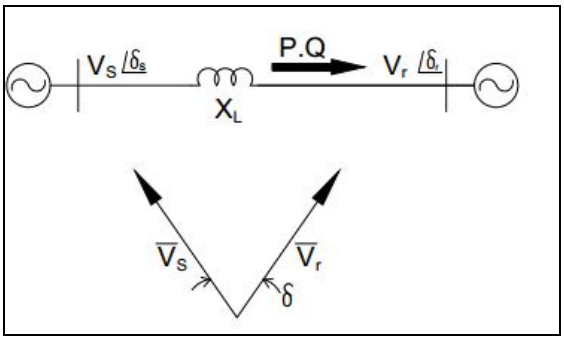

Figure 3: Power transmission system

$$P = \frac{V_S V_R}{X_L}\sin\delta. \qquad Q = \frac{V_S V_R}{X_L}(1 - \cos\delta)$$

Once in the positive power flow controlling which the injected voltage is less than the difference voltages of receiving ends and second in the reversed power flow which the injected voltage is more than the difference voltages of sending ends. So when the power flow is going to reverse the injected voltage needs to change from inductive mode to capacitive mode. Therefore, the expressions for power flow given in equation (1) become

$$P_q = \frac{V^2}{X_{eff}}\sin\delta = \frac{V^2}{X_L\left(1 - \frac{X_q}{X_L}\right)}\sin\delta \quad \text{------- (2a)}$$

$$Q_q = \frac{V^2}{X_{eff}}(1 - cos\delta) = \frac{V^2}{X_L\left(1 - \frac{X_q}{X_L}\right)}(1 - cos\delta) \quad \text{---------- (2b)}$$

Where *Xeff* is the effective reactance of the transmission line between its two ends, including the emulated variable reactance inserted by the injected voltage source of the SSSC. The compensating reactance, *Xq*, is defined to be negative when the SSSC is operated in an inductive mode and positive when this is operated in a capacitive mode. Fig4.shows an example of a simple power transmission system with an SSSC operated both in inductive and in capacitive modes and the related phasor diagrams. The line current decreases from Io% to I-100%, when the inductive reactance compensation,

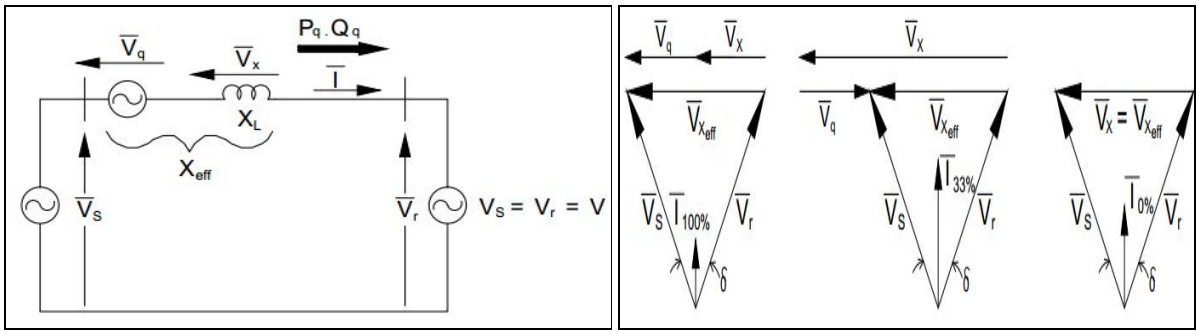

Figure 4: A phasor diagram of SSSC operated in inductive and capacitive mode, -Xq/XL, increases from 0% to 100%. The line current increases from Io% to I33%, when the capacitive reactance compensation, Xq/XL, increases from 0% to 3%.

$$P = \frac{V_S V_R}{X_{eff}} sin\,\delta, \qquad Q = \frac{V_S V_R}{X_{eff}}(1 - cos\,\delta)$$
$$X_{eff} = X_L - X_q$$

3. Multilevel Voltage Source Inverter Using Cascaded-Inverters with Separated Dc Sources

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 5 illustrates the schematic diagram of wye-connected seven-level inverter using three H-bridge cells and three SDCSs per phase, which will be used to verify the concept of the optimized harmonic stepped-waveform technique. From Fig 5. V_{AN} is the voltage of phase A, which is the sum of V_{a1}, V_{a2}, and V_{a3}.The same idea is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. The same three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively According to three-phase theory, line voltage can be expressed in term of two-phase voltages. The advantage of three-phase system is that all triples harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. [4] and [5]

4. Control Strategy

A PLL is a feedback system that includes a voltage control oscillation (VCO), phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the Frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track. As a result of not including any auxiliary source power this strategy can control only the active or Reactive parts of power flow. This control strategy uses two control loop, one for maintaining the DC bus voltage at its reference value which produces the in phase part of injected voltage with the line current and the second loop, control the amount of power flow in the connected line which makes the quadratic part of injected voltage with current. The reference current, active or reactive power is compared with the actual value and passing through a PI controller generates the quadratic part amplitude. The power flow can be increased by acting DSSSC as additional capacitive impedance in series with the transmission line, and decreased by acting it as additional inductive impedance in series with the transmission line .In this control technique two PI controllers are used. One of the PI output controllers is used to identify the mode of operation.

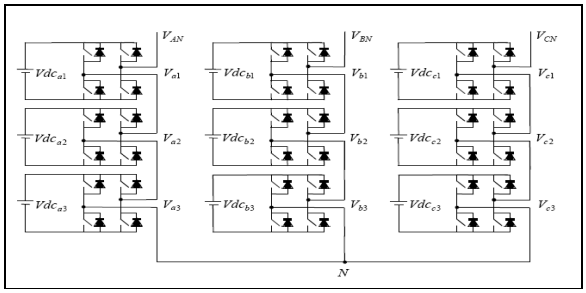

Figure 5: Three-phase seven-level inverter using cascaded-inverters with SDCSs

The reference DC bus voltage is compared with actual DC bus voltage using another PI controller the amplitude of in phase part of injected voltage is as shown in fig 6. But in crossing from the zero current for reversing the power flow the PLL is not able to produce the well results and lose the current phase track which causes the mal function of whole control system. So for solving this problem another control strategy is proposed which uses the phase of feeder voltage instead of current phase. As a result of not having the current phase, it is not possible to maintain the DC bus voltage by controlling the in phase part of injected voltage directly. So the new control strategy which is showed in Fig. 7 and 8. uses the variable DC bus voltage. The active power or current is compared to the actual value and passing a PI controller the voltage reference is produced. In this control strategy, the DC bus voltage is not fixed and varies by the changing in power flow while the modulation index is fixed at (0.9). This reference is compared with the actual DC bus voltage value and using another PI controller, a phase displacement γ is obtained. As a result of having one of feeder voltages close to the injected voltage, it is easy to use it as a reference for phase synchronization.

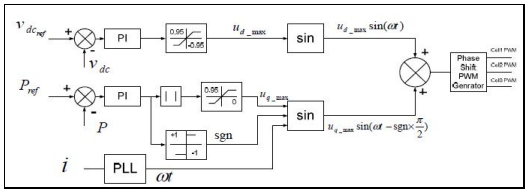

Figure 6: Power flow control with current phase locked loop (With PI controller)

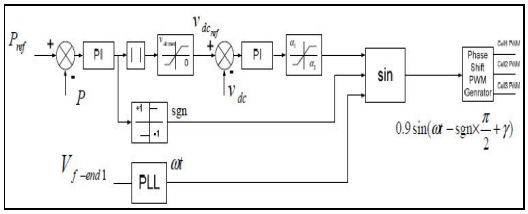

Figure 7: Power flow control with voltage phase locked loop (With PI controller)

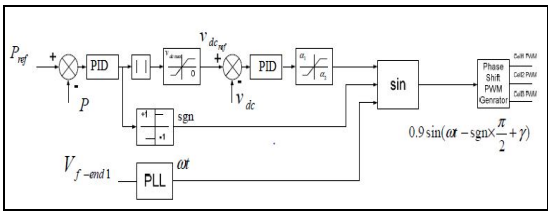

Figure 8: Power flow control with voltage phase locked loop (With PID controller)

Note that the feeder voltage unlike the feeder current has no changes during reversal of power flow and becomes a good choice for synchronization. The same control strategy like Fig. 7 with current PLL is achievable while it is suitable for one direction power flow demanding. In this strategy the DC bus voltage is more than the difference voltages between feeders at connection point when the power flow is reversed. Also using the voltage phase, there is no need to change the control strategy while power flow is reversed .

5. Simulation Results

[1] CURRENT PLL AND VOLTAGE PLL PI CONTROLLER RESULT ARE COMPARED

(A) CURRENT PLL WITH PI CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND CURRENT.

Fig.9 From 0 to 0.5 Sec interval powers is zero after 0.5 to 3 Sec interval power is 1 Pu. Here using the controller is PI. by use of PI controller transient minimum to maximum from 0 to 11 Pu. After the From 3 to 5 Sec intervals the power flow goes to the negative direction but the voltage is increased and current goes to the zero. So, the power flow in 3 to 5 Sec interval is zero. The DC link voltage is maintain 2800V at 0 to3 Sec interval, after it's goes to decreased up to 1500V.

[B] VOLTAGE PLL WITH PI CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 10. From 0 to 0.5 Sec interval power is have some oscillations. After 0.5 to 3 Sec interval power is 0.5 Pu. Here using the controller is PI. After the 3 to 5 Sec interval

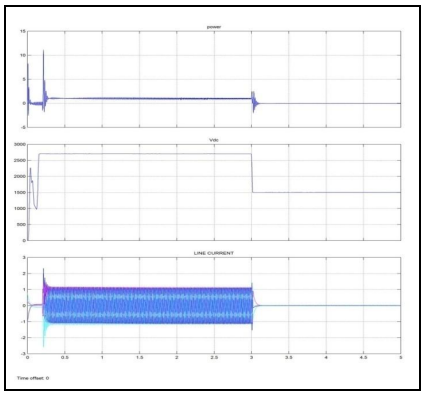

Figure 9: power Vdc and line current

the power flow goes to the negative direction but the power voltage is decreased and current goes to increasing. So, the flow in 3 to 5 Sec interval is negative 0.5 The DC link voltage is Maintain 1000V at 0 to 3 Sec interval, after its goes to increased up to 1500V.From 0 to 3 Sec interval magnitude of the current is 0.5 after it's increasing because of reverse power flow

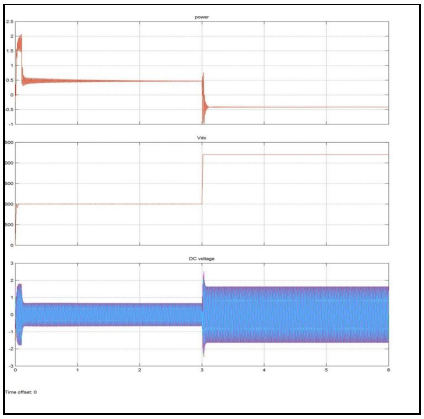

Figure 10: power, Vdc and line current

[2] CURRENT PLL AND VOLTAGE PLL PID CONTROLLER RESULT ARE COMPARED

[A] CURRENT PLL WITH PID CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 11 from 0 to 0.5 Sec interval powers is zero after 0.5 to 3Sec interval power is 1Pu. Here using the controller is PI. By use of PI controller transient min to max is 0 to 7. After the 3 to 5 Sec interval the power flow goes to the negative direction but the voltage is increased and current goes to the zero. So, the power flow in 3 to 5 Sec interval is zero. Compare to PI and PID controller, the transient minimization is better for PID. So the transient stability will improved by using the PID controller. The DC link voltage is maintain 2800V at 0 to3 Sec interval, after it's goes to decreased up to 1500V.At the point 0 to 3 Sec interval magnitude of the current is 1 after it's goes to zero because of reverse power flow.

[B] VOLTAGE PLL WITH PID CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 12. At 0 to 3 Sec interval power is 0.5 Pu. Here using the controller is PID after the 3 to 5 sec interval the power flow goes to the negative direction but the voltage is decreased and current goes to increasing. So, the power flow in 3 to 5 Sec interval is negative 0.5.

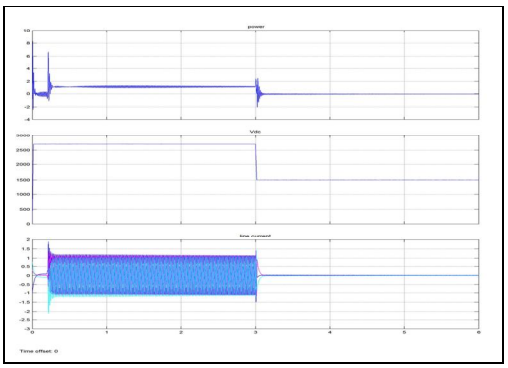

Figure 11: power Vdc and line current

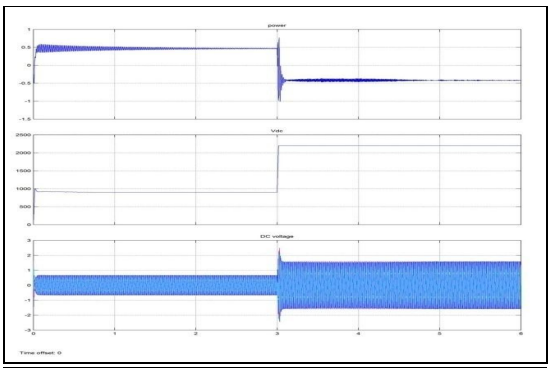

Figure 12: power Vdc and line current.

Compare to PI and PID controller, the transient minimization is better for PID. So the transient stability will improved by using the PID controller. The DC link voltage is maintain 1000V at 0 to3 Sec interval, after it's goes to increased up to 1500V.At the point 0 to 3 Sec interval magnitude of the current is 0.5 after it's increasing because of reverse power flow.
COMPARISON OF THD FOR PI AND PID CONTROLLER FOR BOTH CASES

S.NO	CONTROLLER	PLL	THD (%)
1	PI	CURRENT	0.60
2	PI	VOLTAGE	0.56
3	PID	CURRENT	0.24
4	PID	VOLTAGE	0.12

6. Conclusion

New control strategy i.e. voltage phase locked loop (VPLL) is introduced. The existing control strategy i.e. VPLL is dealt with PI controller. But it has some disadvantages like maximum overshoot, harmonics and more oscillation and settling time. In order to reduce these disadvantages the PID controller is used and a comparative study has been done for PI and PID controller in DSSSC cascaded H-bridge to reverse the power flow. The total harmonic distortion (THD) for the system with compensation (CPLL, PI controller) is 0.60% and proposed compensation (VPLL, PI controller) is 0.56%. From this, we can clearly state that the THD for the system with compensation reduces the harmonics. The total harmonic distortion (THD) for the system with compensation (CPLL, PID controller) is 024% and proposed compensation (VPLL, PID controller) is 0.12%. From this, we can clearly state that the THD for the system with compensation reduces the harmonics

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