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Design and Verification of OCP-AHB Bus Wrapper

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Abstract:
As the design of SoC is getting more and more complicated, the IPs (Intellectual Property) reuse ability increasing is the key issue to improve the time of the embedded systems development and integration. However, the different SoC design nature will affect the IPs reuse ability, such as in different system bus. In this paper we have implemented a standard OCP-AHB bus wrapper bridge. By this wrapper bridge, the IP with OCP interface can connect to AMBA AHB bus rapidly, and IP designer can focus on the development of IP functionalities without considering the data transaction in different interconnects. This will minimize the IPs development time, and maximize the reuse ability. As a result the system integration and verification can be fastened.

Key words*: AHB, AMBA, OCP, IP, SoC*

1. Introduction

The Design and Verification of AHB Interface OCP Master slave Controllers is a novel approach to enable data transfer between two bus architectures, AHB and IP with OCP interface, which have different functionalities and characteristics. The Advanced High-Performance Bus (AHB) is a part of the Advanced Microcontroller Bus Architecture (AMBA). The Advanced Microcontroller Bus Architecture (AMBA) was introduced by ARM Ltd in 1996 and is widely used as the on-chip bus in System-on-a-chip (SoC) designs. The AHB bus is optimized for high-performance, high clock frequency system modules. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macrocell functions.

The Open Core Protocol™ (OCP™) delivers the only non-proprietary, openly licensed, core-centric protocol that comprehensively describes the systemlevel integration requirements of intellectual property (IP) cores. The OCP supports very high performance data transfer models ranging from simple request-grants through pipelined and multi-threaded objects. Higher complexity SOC communication models are supported using thread identifiers to manage out-of-order completion of multiple concurrent transfer sequences.

As the SoC is widely used in the personal electronic products (such as Smartphone, tablet PC), how to improve the time of the integration and verification of SoC is becoming an important issue. And the key point of the acceleration of the SoC integration and verification is how to increase the reuse ability of IPs. However, the IPs designer needs to modify their IPs interface to conform to different system buses and this will affect the IPs reuse ability, and costs additional time to re-verify the correctness of the IPs. As the result, in this paper we have implemented the OCP AHB wrapper with the standard protocol defined by OCP-IP organization [1]. The IP designer just needs to modify the IP's interface to conform to the OCP standard protocol. Therefore, the IP can quickly connect to AMBA 2.0 AHB bus by our OCP-AHB wrapper. This will improve the IP reuse ability and the acceleration of the SoC integration. Furthermore, we added the built-in ICE circuit in our OCP-AHB wrapper to make the verification of SoC more quickly and flexible. The rest of this paper is arranged as following: section 2 describes the related work, section 3 introduces the functionality of the wrapper, section 4 is the organization of the OCP-AHB wrapper, section 5 is the experimental results and section 6 is the conclusion.

2. Related Work

In recent years, the wrapper is designed in two different ways, one is automated synthesis such as [3] [4] [5], in [3], it proposed an algorithm which used two different protocol's FSM to synthesis the corresponding wrapper; in [4], it proposed the algorithm for the automated synthesis can support non-blocking and out of order mechanism; and in [5], the author categorized the interface protocols into 3 groups by the data width and clock frequency, and uses the individual group's algorithm to synthesize the corresponding wrapper. The other way is manual design. According to the different system buses to design the corresponding bus interface, and add some architecture to optimize the wrapper performance, such as [6] ~ [9], and our OCP-AHB wrapper design.

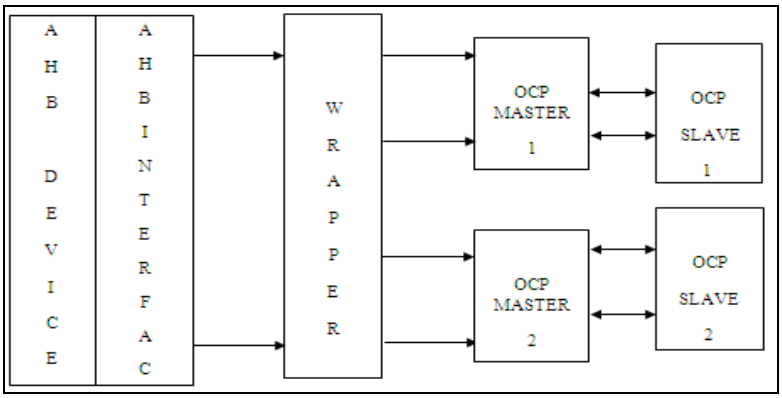


Figure 1. FSM based architecture of OCP-AHB interface

3. Wrapper Functionality

In this section, we will introduce the functionality of OCP-AHB wrapper.

3.1. Functionality of OCP/AHB Wrapper

Figure 1 shows the block diagram of the OCP-AHB master/salve wrapper in the embedded system. The OCP signals from the IP are converted to the AHB signals by the OCP-AHB wrapper.

The OCP-AHB wrapper can support the following transaction mode and processing mechanism:

- Support SRMD (Single Request Multiple Data) transaction mode.
- Support burst and single read/write transaction mode.
- Support the retry and split processing mechanism.
- Support master/slave IP busy state processing mechanism.
- Support four different register in/out version design.
- Support different data width (32/64 bits) conversion.

4. Organization of the Wrapper

In this section, we will show the organization of the OCP-AHB master/salve wrapper.

4.1. OCP-AHB Wrapper Organization

Figure 2 shows the OCP-AHB master wrapper organization. It was composed of OCP-AHB MI FSM, Address Generator, Write Buffer, Read Buffer, two set of Decoder and MUX, and RI(register in), RO(register out) modules.

The introduction of each module is described as following:

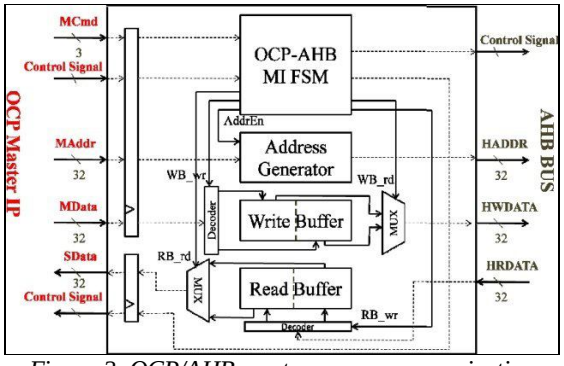


Figure 2. OCP/AHB master wrapper organization

(1) OCP-AHB MI FSM : This module is the kernel unit of wrapper; it is in charge of converting the signals from the OCP interface of master IP to AMBA AHB bus signals. And also controls the other module action.

(2) Address Generator : Since we have taken the SRMD (Single Request Multiple Data) transaction mode, master IP only need to send the first address However, AHB bus is MRMD (Multiple Request Multiple Data) transaction mode, it needs address f or each transfer. Thereby, Address Generator is in charge of generating address of each transfer according to the burst length and the start address.

(3)Write Buffer & Read Buffer : Write Buffer is used to the write data from master IP. The purpose is to improve the performance of burst write transaction, and reduce the latency of waiting. Read Buffer is used to save the read data from the bus. The purpose is the same as Write Buffer. How to use minimal buffer size to achieve the maximum performance will be discussed in section 5.

(4) Decoder & MUX : Decoder decides which entry of the Read/Write Buffer's data will be saved. It's controlled by the WB_wr and RB_wr signals of the OCP-AHB MI FSM.
(5) RI & RO : These two modules are used to adjust system cycle time to avoid the critical path getting too long.
Figure 3 shows the organization of OCP-AHB slave wrapper, and the composed modules are the same as the OCP-AHB master wrapper, besides the FSM module is different. The OCP- AHB SI FSM is in charge of converting the signals from the AHB bus to the OCP interface signals of slave IP.

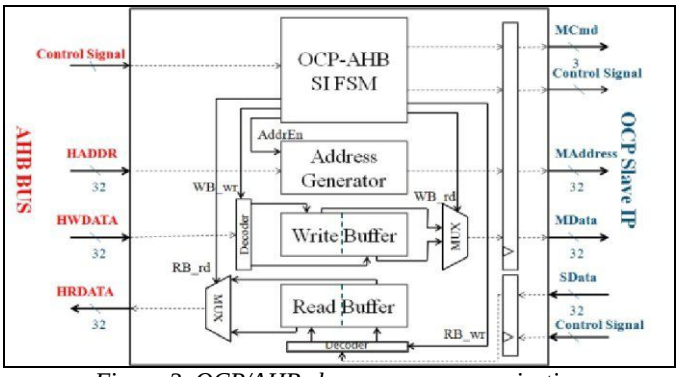
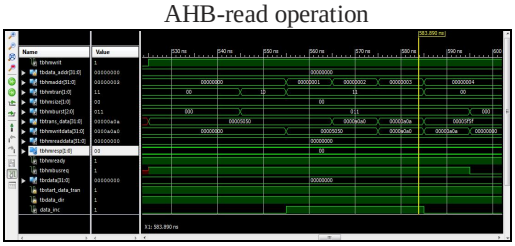


Figure 3. OCP/AHB slave wrapper organization

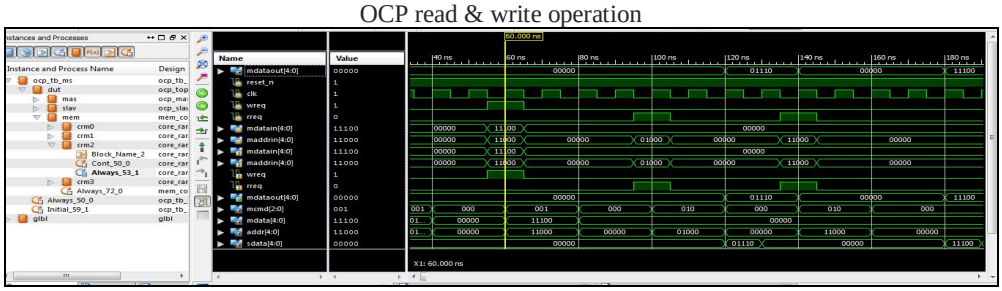
5. Experimental Results

AHB-read operation



AHB-write operation

OCP read & write operation



6. Conclusion

How to increase the IP reuse ability is the key issue for accelerate the SoC integration. In this paper, we have implemented an OCP-AHB wrapper to allow the IP with OCP interface can quickly connect to AMBA AHB bus, and it increases the reuse ability of IP.

7. References

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