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Design and Verification of ADPLL for SERDES

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Abstract:
This project aims towards design of ADPLL (all digital phase lock loop) using Verilog and its verification using Verilog verification methodology. ADPLL is a building block for most high speed digital functional blocks such as SEDRES (Serialization and de-serialization) for clock synchronization. Quistasim/multisim Simulator is used for simulating Verilog Code. This project gives details of the basic blocks of an ADPLL. In this project it is been planned to implementation of ADPLL. Its simulation results are verified for all the corners of inputs. The ADPLL is planned for 200 MHz central frequency. The operational frequency range of ADPLL is 189 KHz to 215 MHz, which is lock range of the design.

Key words*: ADPLL, DCO, FPGA, Loop Filter, Phase Detector*

1. Introduction

The PLL is a self-correcting control system in which one signal chases another signal. PLL has four types i) Linear PLL ii) Digital Phase Locked Loop iii) All Digital Phase Locked Loop iv) Software PLL (SPLL). ADPLL takes input as only digital signals. Due to digital signal as input signal ADPLL offers various advantages over the different types of PLLs. All the components of ADPLL are fully digital. The ADPLL is designed using Verilog HDL. HDL is very flexible for modifying the design parameters. ADPLL has many applications in digital communication. An example of it is FSK decoder. It transfers digital signals.FSK decoder transmits serial binary data by using two different frequency. Logic 0 presents one of frequency and logic 1 presents other frequency. A frequency modulated receiving system based on ADPLL was proposed in 2005. FSK is useful in symbol recovery circuit. ADPLL is a negative feedback control system and it consists of a phase detector, loop filter and digitally controlled oscillator. It contains all the digital blocks. Latest works in the advancement of ADPLL primarily focus on achieving lower output jitter and faster lock-in acquisition for high speed applications. One unique attribute of the ADPLL in this project is its ability to check for input failure in the case of loss of signal. When an error is discovered, the controller is notified and the frequency divider is instructed to continue to produce the output waveform with the last known good characteristics. Meanwhile, status bits are generated to communicate detailed information about the fault situation, such as whether the input signal is stuck at logic high or at low. The structure of the ADPLL is divided into five building blocks. Phase-frequency detector (PFD) determines the differences in frequency and phase between the input reference signal and the output signal. Digitally-controlled oscillator (DCO) acts as the built-in high speed system clock. Input fault detector observes for irregularity on the input signal. Controller provides instruction on how to recreate the resulting waveform.

Frequency divider constructs the output with the proper frequency by dividing down the DCO clock. In this project, a fully operational ADPLL that can be incorporated into an ASIC design was modeled with Verilog HDL and synthesized into circuit using standard cell library available from any EDA tools. It achieved faster lock-in speed than by utilizing a direct approach in acquiring a lock. It also features a monitoring process capable of detecting an input failure and registering the condition as error. In the feedback path a divide-by-N counter is also added in the feedback path to provide a frequency synthesis function. The signal could be single or combination of parallel digital signals. To realize an ADPLL, existing elements must be digital circuits. There are some advantages: No off chip components and Insensitive to technology.

2. ADPLL Functionality

In this section, we will introduce the functionality of ADPLL and their individual blocks The structure of the ADPLL is divided into five building blocks. Phase-frequency detector (PFD), Digitally-controlled oscillator (DCO), voltage controlled oscillator (VCO), input fault detector.

2.1. Functionality of ADPLL for SERDES

Figure 1 shows the block diagram of the ADPLL. It consist of

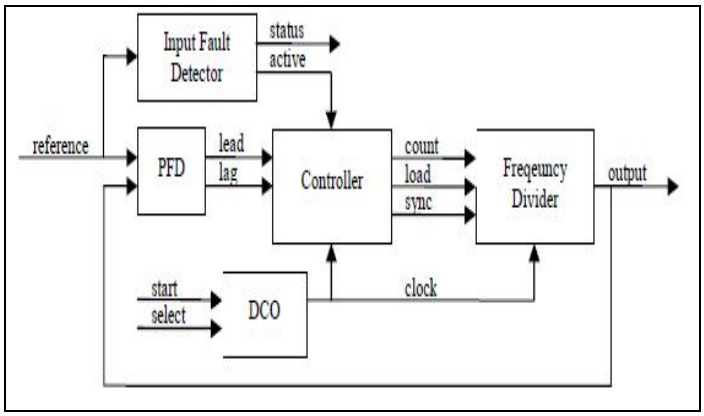

Fig 1.block diagram of ADPLL

The ADPLL can support the following mechanism

- Support multiple functionalities.
- Support internal clock speed in the range of GHz.
- Support external clock to generate max few hundred MHz clock.
- Support multiple clock frequency.
- Support to detect fault at the input.
- Support Clock distribution in large area creates skew/delay and degrades clock quality.

3. Organization of the ADPLL

In this section, we will show the organization of the ADPLL for SERDES.

3.1. ADPLL for SERDES organization

Figure 2 shows the ADPLL. It was composed of counters in that up counter and down counter, JK flipflops, and EXOR gate for phase detector. The input fault detector operates on two separate binary counters. At the input it change to serialized and given to input fault detector and at the output the obtained value is de-serialized and it produces the initial given input value.

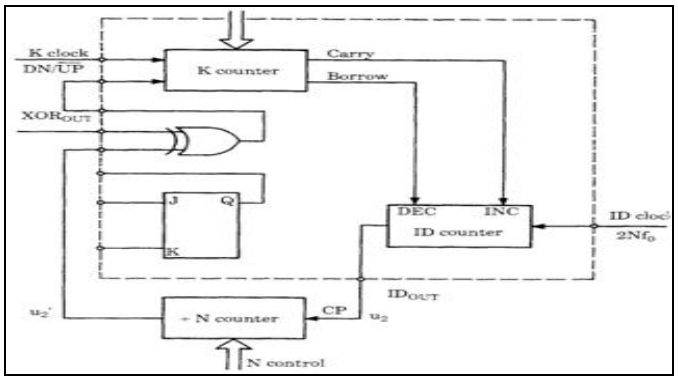

Figure 2. ADPLL Organization

- **Phase Detector-** It compares between input and DCO output signal. Output depends upon the phase error. Output signal contains low frequency and higher frequency component.
- **K Counter Loop Filter-** K counter loop filter is very important loop filter. It always works with JK or EXOR phase detector. It has two counters. Both are independent .One is called Up and other is Down counter. But both counts in upward direction. Counter has modulus K.
- **Digital Controlled Oscillator-** Digitally Controlled oscillators are nothing but a modified oscillator .Depending upon output of the loop filter they change their frequency. Increment Decrement counter is used for our ADPLL design.
- **Input Fault Detector-** One unique attribute of the ADPLL in this project is its ability to check for input failure in the case of loss of signal. When an error is discovered, the controller is notified and the frequency divider is instructed to continue to produce the output waveform with the last known good characteristics

4. Related Work

The ADPLL can be utilized as an intellectual property core to reduce the development time of an ASIC product and maximizing speed and functionality while minimizing power consumption and production cost of an ASIC chip. The advancement of ADPLL primarily focus on achieving lower output jitter and faster lock-in acquisition for high speed applications.

5. Simulation Result

5.1. Phase Detector

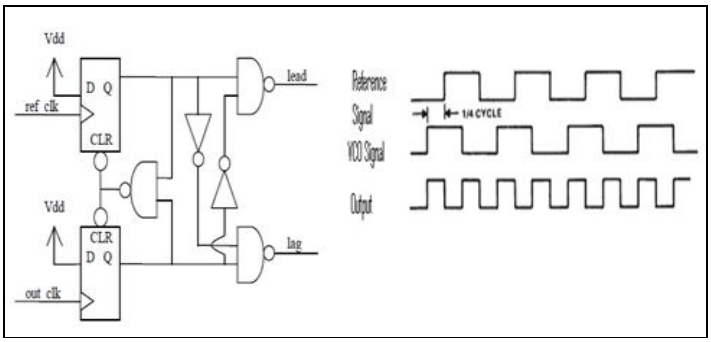

Figure 2: phase detector and required waveform

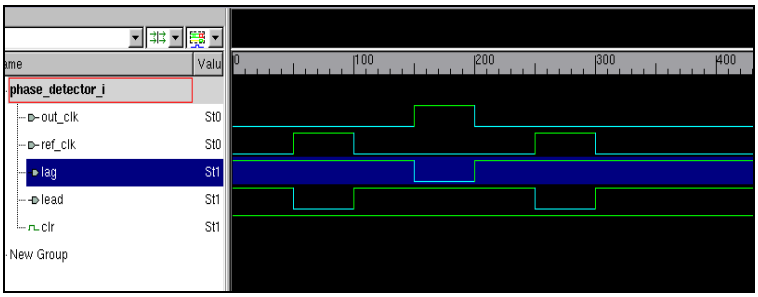

Figure 3: Obtained simulation result for phase detector

5.2. Loop Filter

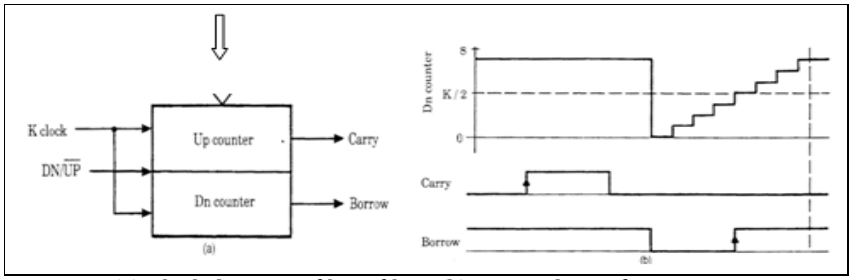

Fig 4. (a) Block diagram of loop filter, (b) expected waveform

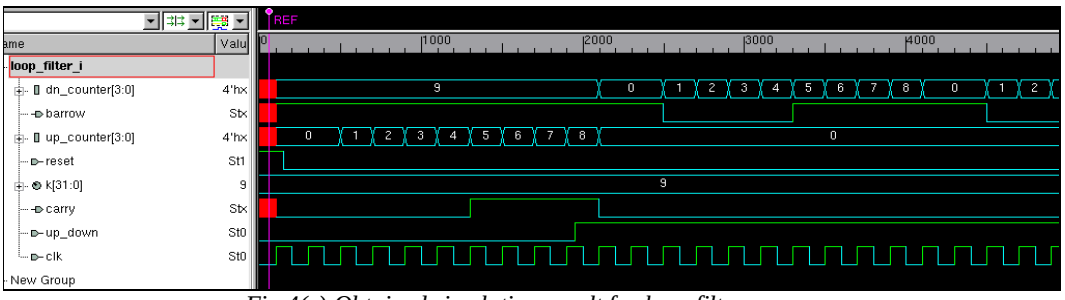

Fig 4(c) Obtained simulation result for loop filter

5.3. DCO and Frequency divider

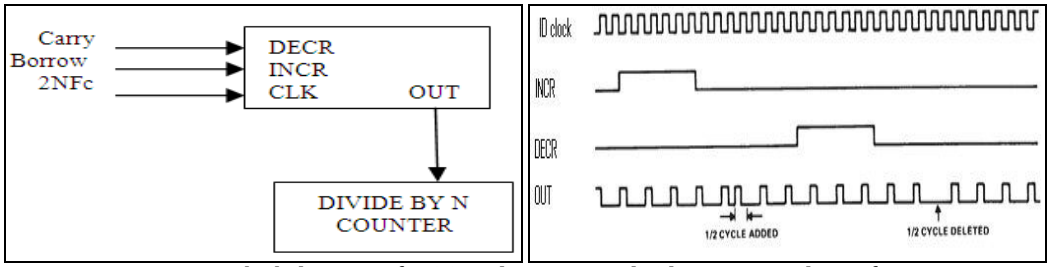

Figure 5: Block diagram of DCO and Frequency divider circuit and waveforms

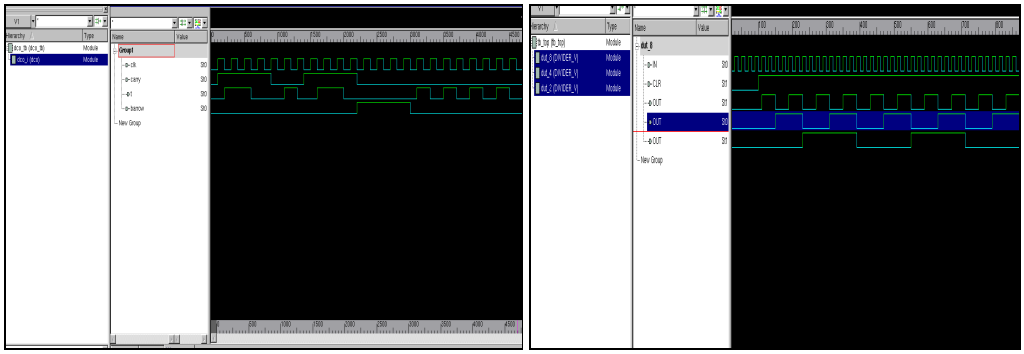

Figure 5(a) Simulation result for DCO and frequency divider

6. Conclusion

This paper discusses the ADPLL design using Verilog HDL It also presents the FPGA implementation in detail. The ADPLL blocks used for the design are also given here. This PLL is designed for the centre frequency of 200 kHz and its operating frequency range of ADPLL is 189 kHz to 215 kHz, which is the lock range of the design. When the input was at fault, it automatically resumed output formation by employing the last known correct parameters.

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7. References

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