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Fast Selective Harmonic Detection and Compensation by Three Phase Cascaded Delayed Signal Cancellation with Shunt APF Circuit

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Abstract:
Fast and accurate selective harmonic detection has crucial value for many power system harmonic compensation systems. The system can be flexibly configured to eliminate or attenuate fundamental harmonic and various background harmonics then detect targeted harmonic's magnitude, phase angle and frequency by PLL. That detected harmonic will be compensated by shunt active power filter circuit. The overall harmonic detection methods are known to have a few drawbacks, such as higher total harmonic distortion, long delay time, sensitivity to grid frequency variation, difficulty to achieve zero study state error and higher total harmonics distortion. In order to overcome these drawbacks, this paper proposes a selective harmonic detection system based on the three phase cascaded delayed signal cancellation with shunt active power filter circuit. It also features very short transient and excellent adaptability under small and considerable frequency variations. Finally this paper provides guidance on how to detect the targeted harmonic's magnitude phase angle and frequency. Also this paper compares the total harmonics distortion in overall harmonics detection method and selective harmonics detection method.

Keywords*: Phase Locked Loop (PLL), Delayed Signal Cancellation (DSC), Selective Harmonic Compensation (SHC), and Active Power Filter (APF) circuit*

1. Introduction

In the past few decades the power electronics field witnessed a rapid growth in power semiconductors and digital techniques, which makes it possible to build systems with high efficiency, reliable and low cost. One of these systems is the voltage source inverter (VSI), which is used in different fields of power converters such as UPS, SMPS, drives, tractions and HVDC. VSI is used to convert DC supply to AC supply at required number of phases and values of voltage and frequency. Different methods were used to generate the gate signals for switching the semiconductor power switching devices in the inverter. The most effective method is the PWM that has ability to regulate the magnitude and frequency of inverter output voltage, and also eliminating or minimizing significant harmonic components of the output voltage. This kind of VSI, based on PWM method, can be performed using different types of strategies. The main types are; natural sampling, suboptimal, optimal and harmonic elimination strategies. Each one of these types depends on an algorithm that generates the PWM patterns which are used to drive the inverter switching power devices [1]. The most effective type is selected harmonic elimination (SHE) technique, which eliminates selected low order harmonics from the spectrum and also reduces the total harmonic distortion (THD). In fact, in order to obtain PWM patterns, number of nonlinear equations in terms of unknown switching angles, depend on number of harmonic components to be eliminated, have to be solved for each value of modulation index using numerical minimization approach.

The detection methods used in harmonics compensation systems can be generally categorized into the overall harmonics detection methods and selective harmonics detection methods. The overall harmonics detection methods eliminate the fundamental frequency signal and extract the harmonics as a whole. The existing method are known to have a few drawbacks, such as long delay time, sensitivity to grid frequency variation, and difficulty to achieve zero steady state error. In order to overcome these drawbacks, a selective harmonics detection system based on the three phase cascaded delayed signal cancellation PLL is available. Also this system can be flexibly configured to detect any individual harmonic from source with various background harmonics. The compensation system can be tuned to address the most problematic harmonics to avoid unnecessary investment on control bandwidth and converter ratings. The compensation delay angle due to sampling and attenuate time is different for each harmonic compensation allows individual correction.

A typical example of harmonic compensation system is the three-phase shunt [2] in Fig. 1. The APF outputs current to dynamically counterbalance the harmonic content in the distorted load current; therefore, the grid/supply current is refrained from harmonic injection [3], [4]. Due to the function in the whole control algorithm, an ideal harmonic detection method must be able to detect the defining characteristics (magnitude, frequency, phase angle, time of occurrence and duration, etc.) of the sensed

harmonic signals as accurately and fast as possible, so as to enable the APF to promptly respond to the everlasting load change [5]-[7].

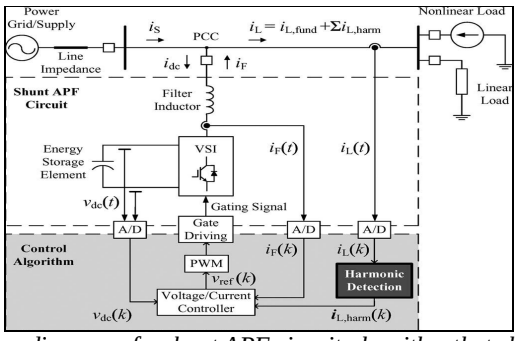


Figure 1: One line diagram of a shunt APF circuit algorithm that shows the location and the function of the harmonic detection block.

This paper proposed a three phase selective harmonic detection method based on a cascaded delayed signal cancellation (CDSC) phase locked loop (PLL) (CDSC-PLL) [22], [23]. It uses αβ-frame CDSC operator to extract harmonic of interest. The undesired harmonics can be completely eliminated, resulting in zero steady state detection error. Multiple CDSC operators can then be arranged in parallel to simultaneously track multiple harmonics. When many harmonics can be present in the input, the number of harmonics to detect avoiding unnecessary uses of parallel CDSC subsystems. The whole system is insensitive to small frequency feedback loop (FFL). Other advantages of the system include the very short transient and small memory overhead.
This paper is organized as follows: Section II introduces the DCS operator and its effect on harmonic signal. Section III explains the construction of CDSC-PLL system and how the system can be configured in different applications. Section IV verifies the system performance with comprehensive experimental result. Section V concludes this paper.

2. DSC and Its Effect on Harmonic Signal

2.1. Representation of harmonic signal
A set of three phase power harmonic signal can be transformed into the αβ frame with Clarke transformation. When load signal is unbalanced and/or distorted, the resulting time domain signal is the sum of harmonics. Each harmonic signal can be represented by a space vector, and each harmonic signal has different magnitude, fundamental angular frequency and initial phase angle. The harmonic space vector rotates at hω frequency in the αβ-frame positive- sequence harmonics (h>0) are rotating counterclockwise, while negative- sequence harmonics (h<0) are rotating clockwise.

2.2. Construction of the DSC operator
The method used for online detection of positive- and negative-sequence components of three-phase quantities, named the delayed signal cancellation (DSC) method, is investigated. Construction of the DSC operator and its effect on harmonic signal are investigated. This technique, based on a combination of positive- and negative-sequence component vectors, allows achieving accurate information on sequence components with a time delay of one-quarter of a period (5 ms at 50 Hz). The method has been successfully applied for flicker mitigation by using a shunt-connected VSC, series compensation by using a SSC, and for shunt-connected VSC used as a front-end rectifier.

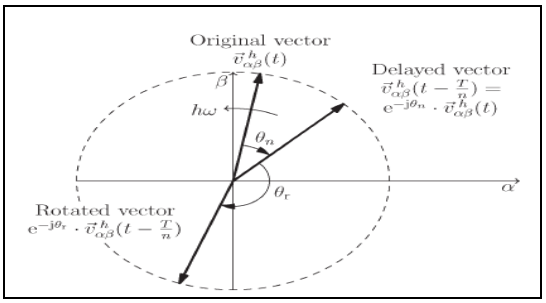


Figure 2: Illustration of the harmonic space vectors used by the DSC operation

Due to the different rotating frequency, different harmonics rotate over different angles in the same portion of time; that's why it is possible to differentiate them through delay operator. Supposing that T/n is chosen as the delay time (T is the fundamental cycle, and n is the delay factor")

2.3. Effect of DSC on Harmonic Signal

When the DSC operator is applied to the input signal that contains different harmonics, each harmonic vector is delayed by a unique angle during T/n time. The rotation angle, however, has a uniform effect on all harmonic vectors, and it is totally subject to the designer's choice. For example it can be "targeted harmonic order". The effect of the designed DSC operator on harmonics can be characterized by its magnitude response (how DSC scales each harmonic magnitude) and phase response (how DSC shifts each harmonic phase angle) as shown in Fig. 3.

All harmonics between the unity gain points and the zero gain points are attenuated but not eliminated.

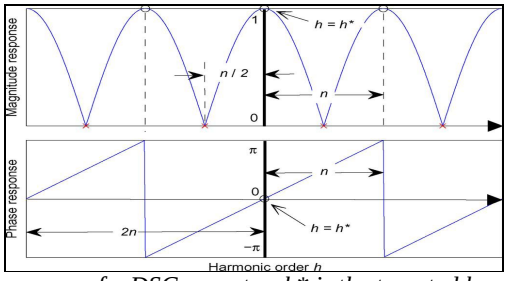


Figure 3: Magnitude and phase response of a DSC operator. h is the targeted harmonics order. n is the delay factor*

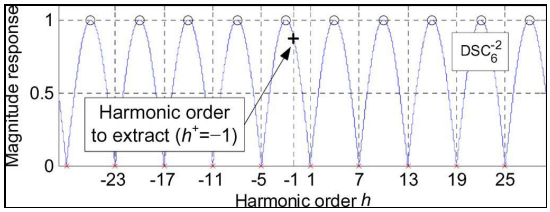


Figure 4: Magnitude response of a DSC operator used to extract the negative- sequence fundamental component

Therefore, by properly selective parameters n and a DSC operator can be configured to eliminate, attenuate, or retain an arbitrarily given harmonic [8].

For example, if a typical harmonic scenario that contains is given , then in order to extract the negative sequence fundamental signal the DSC operator can be designed to use parameters and n=6. Denoted as this DSC operator has such magnitude response that all harmonics and the positive sequence fundamental component can be eliminated. Now with it is easy to formulate the structure diagram of DSC in the time domain. For example of the parameters in fig should be specified as and therefore. Once the parameters are determined, the whole DSC block only involves signal buffering and arithmetic operations [9], [10], and no trigonometric functions need to be called.

The use of a method for online detection of positive- and negative-sequence components of three-phase quantities, named the delayed signal cancellation (DSC) method, has been investigated. Finally, since the DSC method relies on accurate knowledge of the grid frequency, the effect of grid frequency variations has been considered [11], [12]. It has been demonstrated that the error due to inaccurate knowledge of the grid frequency and the error due to non ideal discretization have the same expression and, therefore, the given derivations, including the proposed methods for reducing the detection errors, can be applied without modifications to the case of grid frequency variations.

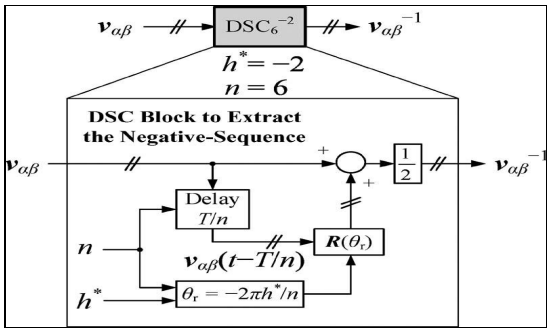


Figure 5: Structure diagram of a DSC operator configured to extract the negative-sequence fundamental component

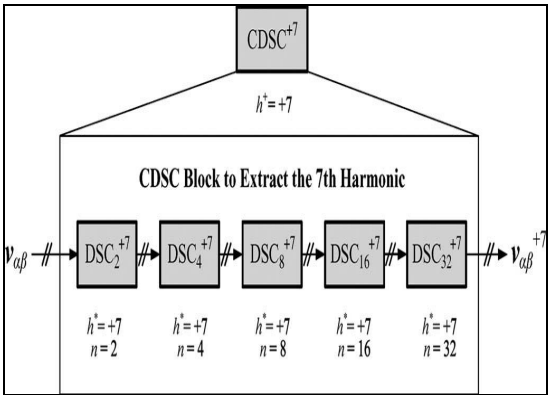
It is worth mentioning that similar delay based signal operation is also studied under the name of extended DSC [11], generalized DSC [12].

3. CDSC PLL for Harmonic Detection

3.1. CDSC Operator and its Effects on Harmonic Signal

Although a single DSC operator cannot perfectly extract a harmonic of interest from all harmonic scenarios, it can be used as a building block. multiple DSC operators connected in series from the CDSC operator, where the DSC operator are configured with different parameter to reject undesired harmonics step by step, leaving only the harmonic component means to extract.

The simplest idea of CDSC design is to use one DSC to eliminate one harmonic [13]. Beyond this idea, however, the fact that a DSC has multiple zero gain points should be considered, which means that one DSC can actually eliminate multiple harmonics. Therefore, by properly coordinating the parameters of each DSC, the total number of DSC blocks can be much less than the harmonics to eliminate.



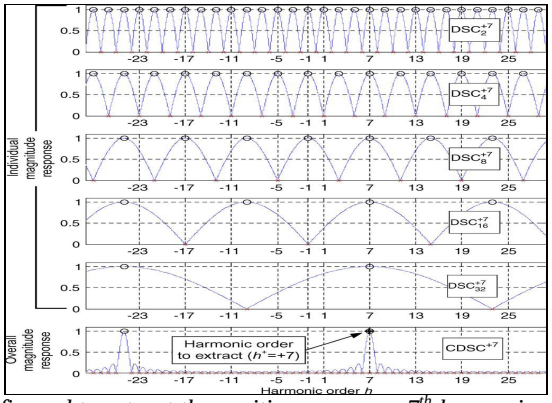


Figure 6: Structure diagram of a CDSC operator configured to extract the positive- sequence 7th harmonic.

Figure 7: Individual and overall magnitude response of a CDSC operator used to extract the positive-sequence 7th harmonic. Unity gain points are marked by "0." zero gain points are marked by "x."

For example, in order to extract the positive sequence 7th harmonic one only needs a CDSC operator with five DSC blocks, as calculated.

3.2. Correction of harmonic signal processed by CDSC

In order to correct the magnitude scaling and phase shift of CDSC on the harmonic to extract, the overall effect of CDSC must be quantified first. Denote the harmonic gain of a DSC operator upon the harmonic order to extract as, and denote the overall gain of the CDSC operator upon as [15].

To be detailed, after the magnitude (denoted as) and the phase angle (denoted as) are determined for the extracted signal. Should be used to multiply to get a correct estimate. Such algebraic operation involves neither mass storage of dada nor time delay, so it is very efficient and convenient. It should also be highlighted that the phase angle of adjustment factor can be further modified to account for other phase delays identified in the harmonic compensation system, such as the sampling delay in A/D conversion, the actuation delay of the power converter. Therefore, the proposed method can provide high accuracy and flexibility to selective harmonic compensation.

3.3. Design of CDSC PLL for harmonic detection

A PLL is a device that is able to keep an output signal synchronized in frequency, as well as in phase, with a reference input signal. More precisely, the PLL is a servo system that controls the phase of its output signal in order to minimize the phase error between the output and reference phases.

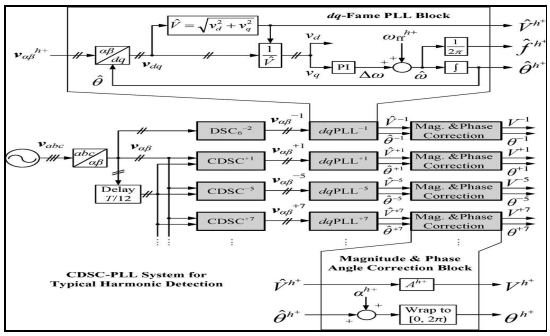


Figure 8: Structure diagram of the CDSC-PLL system for typical harmonic detection

Extended from the example introduced earlier, a complete harmonic detection system using CDSC and dq frame PLL (dqPLL), namely, CDSC-PLL can be created as shown in fig 8. The system takes the sensed three- phase harmonic signal as the input and

gives fundamental and individual harmonic signal magnitude and phase angle as the output. One harmonic component is detected by a subsystem, which comprises of three blocks, and their functions are elaborated as follows.
DSC/CDSC block: This block" sieves" the input αβ- frame signal, letting through a signal component. Moreover, the block, whose magnitude response is shown in fig.4, extract the negative sequence fundamental component.
PLL block: This block detects the magnitude and the phase angle of each extracted harmonic signal.
Magnitude & phase correction block: This block simply corrects the magnitude scaling and phase shift introduced in DSC/CDSC.

4. Experimental Result

Two test cases are required to verify the total harmonics distortion in the simple power system generation, transmission and distribution network. By verifying the total harmonics distortion in different harmonics detection method will shows the better method for harmonics compensation.
Test case 1: Apply the overall harmonic detection method.
In the overall harmonic detection method percentage of total harmonic distortion is high.
Test case 2: Apply the selective harmonic detection method.
In the selective harmonic detection method percentage of total harmonic distortion is low.

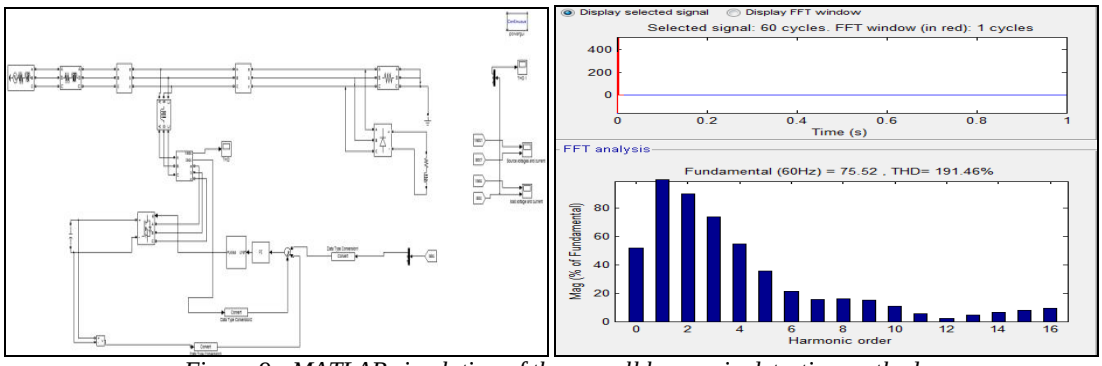


Figure 9: MATLAB simulation of the overall harmonic detection method
Figure 10: Total harmonics distortion in the system before compensation.

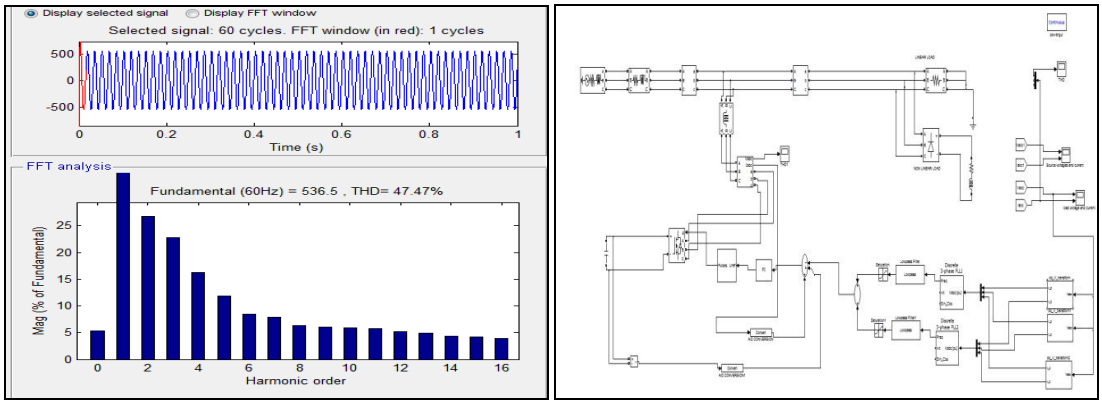


Figure 11: Total harmonic distortions in the system after overall harmonics detection method of compensation.
Figure 12: MATLAB simulation of the selective harmonic detection method of harmonic compensation.

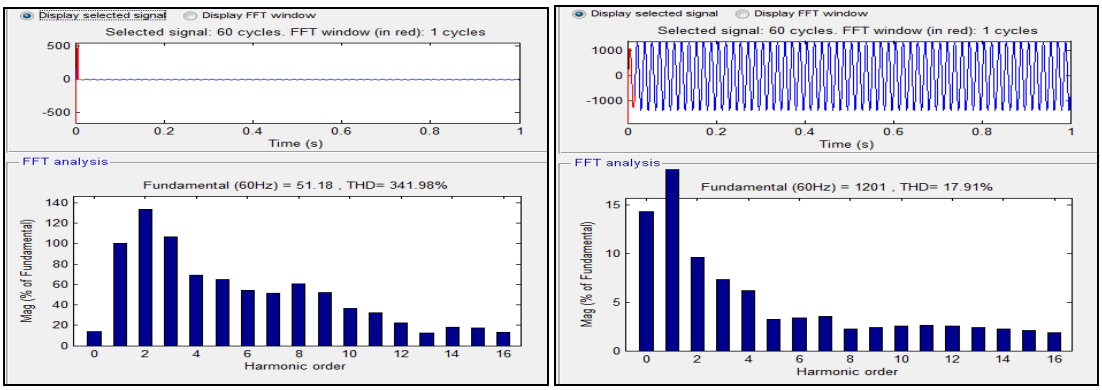


Figure 13: Total harmonics distortion in the system before compensation.
Figure 14: Total harmonic distortions in the system after selective harmonics detection method of compensation.

5. Conclusion

This paper has proposed a selective harmonic detection system based on the CDSC-PLL. The cornerstone of the system is the DSC operator, which can be configured to eliminate some harmonics while letting through the others. It can be further cascaded into the CDSC operator to extract an arbitrary harmonic from various harmonic combinations. One DSC/CDSC block plus some auxiliary function blocks (e.g., *dq*PLL and Magnitude & Phase Correction) constitute a harmonic detection subsystem. Multiple parallel subsystems are capable of detecting all the input harmonics with a very short time delay.

The resulting CDSC-PLL system is insensitive to small grid frequency variations and can be extended to handle considerable frequency shift by using an FFL. Special considerations are also given to the practical implementation issues of this system, and a discretization error reduction method is provided to address the issues.

Different test cases are designed to examine the system performance that percentage of total harmonic distortion. The obtained experimental results confirm that the proposed system is fast and robust under various working conditions, rendering it a good candidate for applications in three-phase selective harmonic compensation systems.

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