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Design and Verification of DDR SDRAM Controller for Satelite Data Acquisition System

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Abstract:
DDR SDRAM, with features of large capacity and high speed, has a good prospect in the acquisition of satellite navigation system which requires large amounts of data accumulation. A Dedicated Memory Controller is of prime importance in applications that do not contain microprocessors (high-end applications). The Memory Controller provides command signals for memory refresh, read and write operation and initialization of SDRAM. Our work will focus on ASIC Design methodology of Double Data Rate (DDR) SDRAM Controller that is located between the DDR SDRAM and Bus Master. The Controller simplifies the SDRAM command interface to standard system read/write interface and also optimizes the access time of read/write cycle. Double Data Rate (DDR) SDRAM Controller is implemented using Cadence RTL Compiler.

Keywords*: DDR SDRAM Controller, Read/Write Data path, Questa sim*

1. Introduction

Memory devices are almost found in all systems and nowadays high speed and high performance memories are in great demand. For better throughput and speed, the controllers are to be designed with clock frequency in the range of megahertz. As the clock speed of the controller is increasing, the design challenges are also becoming complex. Therefore the next generation memory devices require very high speed controllers like double data rate and quad data rate memory controllers. The double data rate SDRAM Controller is implemented using ASIC methodology. Synchronous DRAM (SDRAM) is preferred in embedded system memory design because of its speed and pipelining capability. In high-end applications, like microprocessors there will be specific built in peripherals to provide the interface to the SDRAM. But for other applications, the system designer must design a specific memory controller to provide command signals for memory refresh, read and write operation and initialization of SDRAM. The SDRAM controller, located between the SDRAM and the bus master, minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master. SDRAM's are classified based on their data transfer rates. In Single data rate SDRAM, the data is transferred on every rising edge of the clock whereas in double data rate (DDR) SDRAM's the data is transferred on every rising edge and every falling edge of the clock and as a result the throughput is increased. DDR SDRAM Controllers are faster and efficient than its counterparts. They allow data transfer at a faster rate without much increase in clock frequency and bus width.

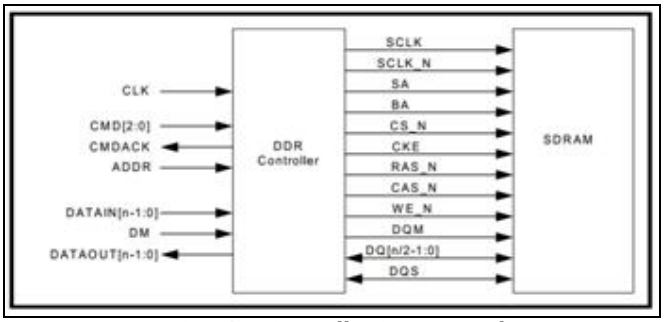

Figure 1: DDR SDRAM Controller System Level Diagram

2. Implementation Methodolody

The DDR SDRAM Controller architecture is implemented using Verilog HDL. The methodology followed is ASIC design flow. The basic steps that an ASIC design must go through are Design entry and Analysis, Technology Optimization and Floor planning, Design Verification, Layout. The RTL Synthesis and Simulations are performed using existing tools like Questa sim

3. DDR SDRAM Controller Architecture

The DDR SDRAM Controller Core consists of four main modules, the SDRAM controller, Control Interface, Command, and Data Path Modules. The DDR SDRAM controller module is the top-level module that instantiates the three lower modules and brings the whole design together. The Control Interface Module accepts commands and related memory addresses from the host, decoding the command and passing the request to the Command module. The Command Module accepts command and address from the Control Interface Module, generating the proper commands to the SDRAM. The Data Path Module handles the data path operations during WRITEA and READA commands. The top-level module also instantiates two PLL's that are used in the CLOCK_LOCK and 2X mode to improve I/O timing and to generate a 2X clock. DDR SDRAM Controller module receives addresses and control signals from the BUS Master. The Controller generates command signals and based on these signals the data is either read or written to a particular memory location.

The DDR SDRAM Controller architecture is shown in Figure 2. It consists of three modules: 1) Main control module 2) signal generation module 3) data path module. The main control module has two state machines and a refresh counter. The two state machines are for initialization of the SDRAM and for generating the commands to the SDRAM. They generate iState and cState outputs according to the system interface control signals.

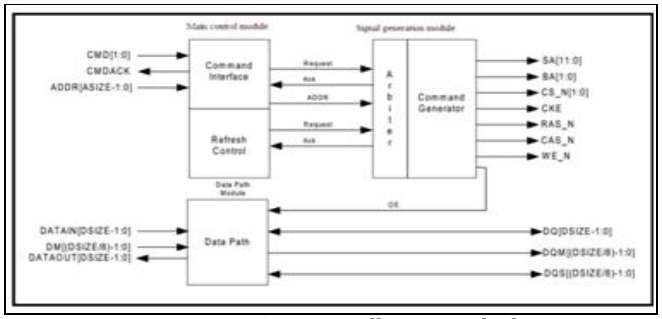

Figure 2: DDR SDRAM Controller Core Block Diagram

The signal generation module now generates the address and command signals depending upon the iState and cState. The data path module performs the read and write operations between the bus master and DDR. Following are some of the important features of DDR SDRAM Controller:

- The DDR SDRAM Read and Write operations are simplified by the controller.
- For initializing the DDR SDRAM controller, separate state machines are designed internally.
- The access time for read and the write cycle is optimised based on the CAS latency and burst length of the DDR SDRAM.
- The auto refresh for the DDR SDRAM is done by the controller.

The main control module consists of three sub modules:

- Initialization FSM module (INIT_FSM).
- Command FSM module (CMD_FSM)
- Counter module.

3.1. Main Control Module

The DDR SDRAM Controller has to undergo an initialization process by a sequence of command signals before the normal memory access. The initialization finite state machine in the main control module is responsible for the initialization of the DDR SDRAM controller. Figure 3 shows the state diagram of the initialization FSM (INIT_FSM). Whenever reset signal is high, the initialization FSM will switch to i_IDLE state. Once the reset signal goes low, the controller has to wait for 200us clock stabilization delay. This is constantly checked by sys_dly_200us signal and a high on the sys_dly_200us will indicate that the clock stabilization delay is complete. The DDR initialization sequence will begin immediately after the clock/power stabilization is complete and then the INIT_FSM will change its state from i_IDLE to i_NOP state. From the i_NOP state, the initialization FSM will switch to the i_PRE state on the next clock cycle. In the i_PRE state, the main control module will generate the PRECHARGE command. The PRECHARGE command generated during this state will be applied to all the banks in the device. Once the PRECHARGE command is generated by the initialization FSM, it will switch to the next state. The next state in the design of initialization FSM is two AUTO REFRESH commands. These refresh commands are generated to refresh the DRAM memory. After the two refresh state, the initialization FSM will switch to i_MRS state. During this state LOAD MODE REGISTER command is generated to configure the DDR SDRAM to a specific mode of operation. After satisfying the i_tMRD timing delay the initialization FSM will switch to i_ready state. The initialization FSM will remain in the i_ready state for normal memory access. And also, when the initialization FSM switches to i_ready state signal sys_INIT_DONE is set to high to indicate that DDR SDRAM controller initialization is completed.

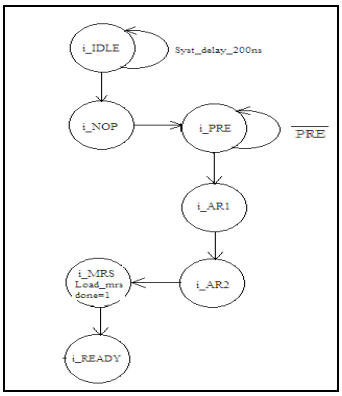

Figure 3: Initialization FSM

In the design of controller, timing control of reading and writing operations is completed according to the state machine. Before issuing a READ or WRITE command, we should active the row to be read or written, as shown in Figure 4. Read and write accesses to the DDR SDRAM are burst-oriented. The burst length determines the maximum number of column locations accessed for a given READ or WRITE command , and the value can be programmable to either 2, 4, or 8. In this design, the burst length is set to be 8 to guarantee the efficiency of read and write.

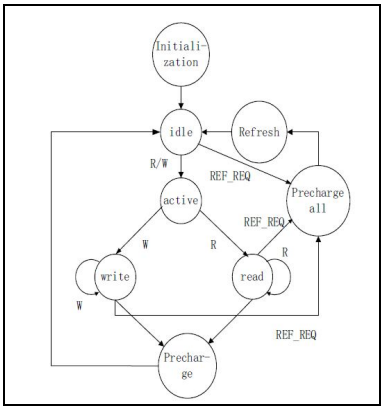

Figure 4: Command FSM

An AUTO REFRESH command is issued to the DDR memory at specified intervals of time to refresh the charge to retain the data. If the memory is reading or writing when issuing an AUTO REFRESH command, the controller will wait until the current operation complete and then send a new command. If the user has read/write request during the refresh process, the controller will not respond to the requests until the completion of the current refresh cycle. CMD_FSM handles the read, write and refresh of the SDRAM

3.2. DATA Path Module

The Data Path Module provides the SDRAM data interface to the host. Host data is accepted on port DATAIN for WRITEA commands and data is provided to the host on port DATAOUT during READA commands The DDR SDRAM Controller design interfaces between the 8-bit data bus, and the bus master with a 16-bit data bus. The data path module for read and write are shown in figure. The data path module depends on cState for its read/write operation. The cState is generated by the CMD_FSM present in the Main Control module

3.3. Signal Generation Module

The Signal generation Module accepts decoded commands from the Main Control Module, along with refresh requests from the refresh control logic and generates the appropriate commands to the SDRAM. The module contains a simple arbiter that arbitrates between the commands from the host interface and the refresh requests from the refresh control logic. The refresh requests from the refresh control logic have priority over the commands from the host interface. If a command from the host arrives at the same time or during a "hidden" refresh operation, the arbiter holds off the host by not asserting CMDACK until the hidden refresh operation is complete. If a hidden refresh command is received while a host operation is in progress then the hidden refresh is held off until the host operation is complete. After the arbiter has accepted a command from the host, the command is passed onto the command generator portion of the Signal generation Module.

4. Analysis Of Result

The Design is simulated after combining the BUS Master, DDR SDRAM Controller and the DDR SDRAM.

4.1. DDR SDRAM Write

Data is written from the bus master to memory when the RAS is made High, CAS is made Low and WEN is made Low. This data is stored in the banks of the SDRAM. Fig. 5 show the simulation waveforms of writing

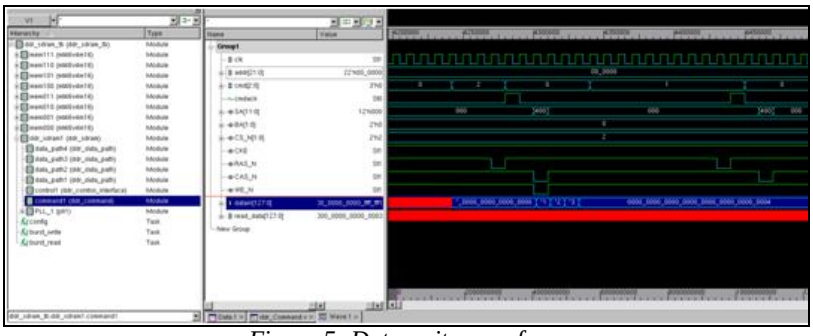

Figure 5: Data write waveform

4.2. DDR SDRAM Read

Data stored in the banks of SDRAM is read to the bus master when the RAS is made High, CAS is made Low and WEN is made High. Fig. 6 show the simulation waveforms of reading.

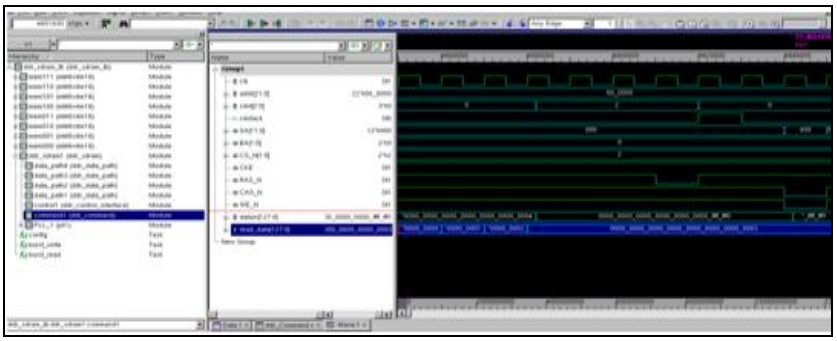

Figure 6: Data read waveform

5. Applications and Advantages

Applications

- Personal computer
- Higher end applications such as satellite

Advantages

- Increase System Memory
- Increase System Speed
- Data is transferred on the rising edge and the falling edge of the clock.
- High throughput
- Low power consumption

6. Conclusion

DDR SDRAM is designed such that we will get double the speed without doubling the price. ASIC Design methodology is opted for Double Data Rate (DDR) SDRAM Controller. The DDR SDRAM Controller architecture is implemented in Verilog HDL. The RTL Simulation and Synthesis results are obtained using Questa sim

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