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Design and Implementation of High Speed Binary Comparator Using QCA Technology

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Abstract: *As the size of CMOS transistors keep shrinking, it will eventually hit its limitation. Hence an alternative device has to be discovered to continually improve the development of electronics devices. Quantum dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low power high performance digital circuits. Efficient solutions have recently been proposed for several arithmetic circuits, such as adder, multipliers, and comparators. This work proposes a new design approach oriented to implementation of binary comparators in QCA. The proposed QCA based comparator has been designed using verilog and simulated using Xilinx 9.1. The comparator proposed here exhibit significantly higher speed and reduced over all area with respect to exhibiting comparators, this is due to elimination of long carry chain of checking bits from MSB to LSB in proposed comparator.*

Keywords: *Binary comparator, Quantum cellular automata (QCA), Xilinx.*

1. Introduction

In the early days of integrated circuits, only a few transistors could be placed on a chip, as the scale used was large because of the contemporary technology, and manufacturing yields were low by today's standards. Today ICs are designed using CMOS technology. The device sizes are continuously shrinking following the Moore's law and the clock speeds and computing performance are increasing. But since the last decade the performance of the devices are improving mostly because of the exploitation of the parallelism in the processors and software. With the advancement of the technology the device sizes are reaching their physical limit. Hence there is a lot of research in the alternative technologies like Quantum Dot Cellular Automata [1]. Quantum Dot Cellular automata use the position of the confined electrons in the quantum dots to represent logic states and unlike conventional electronics does not rely on electron flow. This columbic force is responsible for all the logic operations and transfer of the states from one location to another [12]. In this work the binary comparator is designed using QCA.

A digital or magnitude comparator is a hardware electronic device that has two binary inputs, and determines whether one number is greater than, less than, or equal to the other number. The comparator widely used in Central Processing Units(CPU), Micro Controller Units which is a crucial data path element of image and signal processing architecture [5]. In the last few years, the design of high speed and low power binary comparator has received great deal of attention [6]. Comparator can be broadly classified into Analog and Digital. They are further classified into Total (Full) comparators and Equality comparators. In full comparators, given A and B being 2 n-bit binary numbers, they are able to separately recognize the 3 possible conditions i.e. A>B, A<B, and A=B [5].

The comparison of two bit is one of most widely used in computer system ,device interfaces for equality, scientific computation(graphics and image/signal processing), test circuit application (jitter measurement, signature analyzers, and built in self test circuit) and optimized equality only comparators for general purpose processor components(associative memories, load-store queue buffers, translation look –aside buffers, branch target buffers), and many other CPU argument comparison blocks. Also it is important arithmetic operation in DSP applications, digital filter. Digital Signal Processing (DSP) is one of most important unit in electronic devices.

The rest of this work is organized as follows: Section II gives basic about QCA. Section III gives a brief description of the existing comparator designs. Section IV discusses the methodology involved in the proposed comparator. Experimental evaluation of the proposed comparator is discussed in section V. A brief conclusion of the work done is given in Section VI.

2. Quantum Cellular Automata (QCA)

As alternative to CMOS –VLSI, researchers have proposed an approach to computing with quantum dots, the quantum cellular automata (QCA). First proposed in 1994, conventional computers in which information is transferred from one place to another by

means of electrical current, QCA transfers information by propagating a polarization state. QCA is based upon the encoding of binary information in the change configuration within quantum doe cells. Computational power is provided by the coulombic interaction between QCA cells. No current flow between cells and no power or information is delivered to individual internal cells. The local interconnections between cells are provided by physics of cell to cell interaction due to the rearrangement of electron positions[13].
The basic element of a nanostructure based on QCA is a square cell with four quantum dots and two free electrons. The latter can tunnel through the dot s within the cell, but, owing to coulombic repulsion, they will always reside in opposite corners, thus leading to only two possible stable states, also named polarizations[12].

2.1. Majority Gate
The most important logic gate in QCA is the majority gate [12]. Figure 1 shows a majority gate with three inputs and one output. In this structure, the electrical field effect of each input on the output is identical and additive , with the result that whichever input state (binary 0 or binary 1) is in the majority becomes the state of the output cell, hence the gate's named as majority gate. For example, if input A and B exist in a binary 0 state and input C exists in binary 1 state, the output will exit in a binary 0 state since the combined electrical field effect of input A and B together is greater than that of input C alone[4].

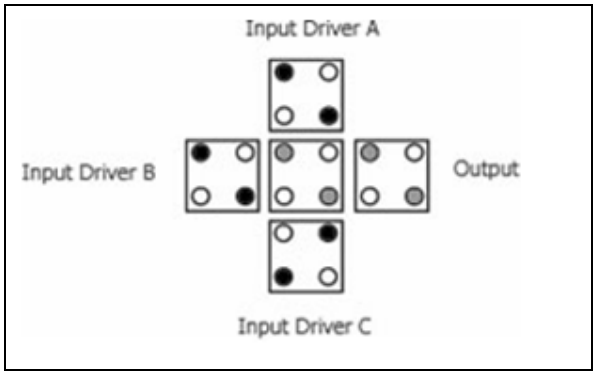

Figure 1: QCA Majority Gate

Other type of gates, namely AND gates and OR gates, can be constructed using a majority gate with fixed polarization on one of its inputs. For input A,B and C , The Majority Gate perform following logic function.
$M(A, B, C) = A.B + B.C + C.A$ --(1)

2.2. Advantages of QCA
- Devices (quantum cell) used for this computational paradigm have dimensions of only a few square nanometers.
- It is estimated that 1-2nm quantum cells would function at room temperatures.
- A quantum cell uses impulses as stimulus, and not current as the transistor does, therefore a drastic reduction in power consumption may result.

3. Existing Binary Comparator Design
The comparator proposed in [14] exploits TB architecture to achieve high speed. Where 4-bit operands are assumed, one instance of the 1-bit comparator presented in [15] is used for each bit position. The intermediate results obtained in this way are then further processed through a proper number of cascaded 2-input OR and AND gates implemented by means of MGs having one input permanently set to 1 and 0, respectively.
The Novel Comparator proposed in [12] uses four theorem and the two corollaries. The Novel formulation can be exploited in the design of n-bit full comparators splitting the operands A(n-1 : 0) = an-1……a0 and B(n-1 : 0) = bn-1…….b0 into a proper number of 2-bit and 3-bit sub words that can be compared applying Theorems 1 and 2. The intermediate results obtained in this way can be then further processed by applying Theorem 3 and 4 together with coloraries 1 and 2. This indeed occupies huge area and increases hardware complexity. To overcome this, separate the binary input into groups called digit sets and perform comparison within digit sets starting from MSB. The checking of all the digit sets is done by a single Initial Processing and adder block where the different digit sets are time multiplexed on these unit.

4. Proposed Comparator Based on QCA
The proposed binary comparator based on QCA consisting of Initial-Computational unit and Adder block. The basic principle of this comparator is to group the binary inputs into digit sets. The digit sets are sending to the initial computational unit starting from Most Significant Digit (MSD) to check for equality and the computations in Initial computation unit are stopped at the first digit set which produces 1 output. The corresponding digit set is send to the Adder block to find the greater of two inputs. Thus, the proposed design avoids unnecessary checking of the entire bit in the input. Figure 2. Shows the block diagram of the proposed comparator

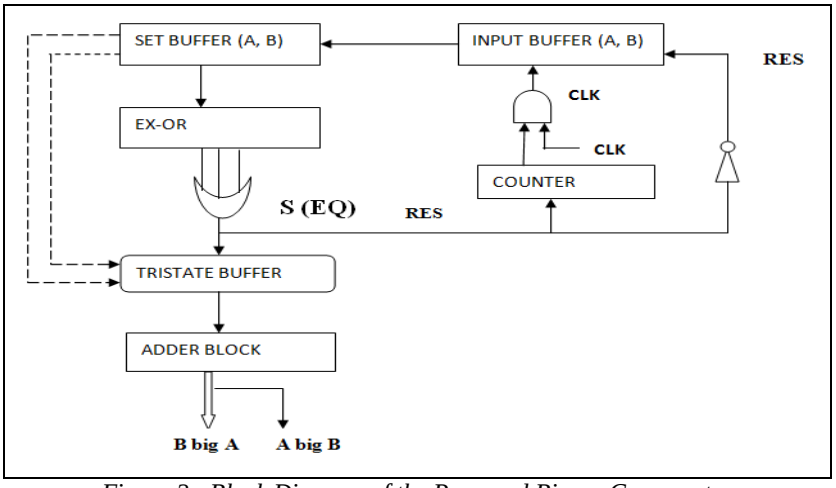

Figure 2: .Block Diagram of the Proposed Binary Comparator

4.1. Pre – Computation Unit

The IB (Input Buffer) stores the two binary inputs. Based on the digit size the counter value is initialized. For each tick of the counter the bits are shifted into the Digit Buffer (DB) from the Input Buffer. The required number of bits is shifted into the DB when the counter output reaches "0". The pre-computation unit performs EX-OR operation on bits in Digit Buffer starting from Most Significant Bit (MSB). The EX-OR outputs are OR ed to find the equality within digits. If two digit sets are equal the ORed output will be zero and the next digit set will be passed to the DB for comparison. In case of unequal digit sets, ORed output will be "1", then the computations in the pre-computation block are stopped and the corresponding digit sets are send to the encoder block to determine the greatest of the two. On the other hand, if the output EX-OR is zero for all digit sets, then the input word is considered to be equal which can be realized by a "1" output at "EQ".

4.2. Adder Block

The adder block of the proposed comparator uses carry generation equation of CLA addition [6] to find the greatest among the two inputs. For a 2-bit digit (A1A0) and (B1B0), comparison can be realized with the following Equation proposed by Chaung et al [6].

BGR = ~ (A1)B1 + ~ (A1^ B1)(~A0B0) ---(1)

This is similar to the carry generation of a CLA adder given by

Cout = G + PCin --(2)

which can be written as

Cout = Gi + PiGi-1 -- (3)

Where Cout is equal to BGR, Generate 'Gi' is equal to '~(Ai)Bi' , 'Pi' is equal to '~(Ai ^ Bi)'. BbigA will be equal to "1" when the digit set B_{DS}(BiBi-1) is greater than digit set A_{DS}(AiAi-1) and BbigA will be equal to "0" if the digit set B_{DS}(BiBi-1) is less than digit set A_{DS}(AiAi-1).

5. Result and Discussion

The proposed QCA based comparator has been designed using verilog code and simulated using XILINX ISE 9.2. The power and delay has been estimated using QUARTUS II .The power and delay has been reduced in proposed comparator. This is due to elimination of long carry chain of checking bits from MSB to LSB in proposed comparator. From the area estimation it can be seen that our comparator realizes the logic with fewer gate counts compared to all other previous designs. This is due to tree based realization of proposed comparator.

PARAMETER		ROPOSED COMPARATOR		
		4 BIT	8 BIT	16 BIT
POWER		125.12	135.56	136.83
DELAY		7.843	10.456	11.345
AREA	XOR	5	12	18
	OR	6	5	6
	NOT	6	12	18

Table 1: Power Delay Area Estimation of Proposed Comparator

5.1. Simulation Wave Form

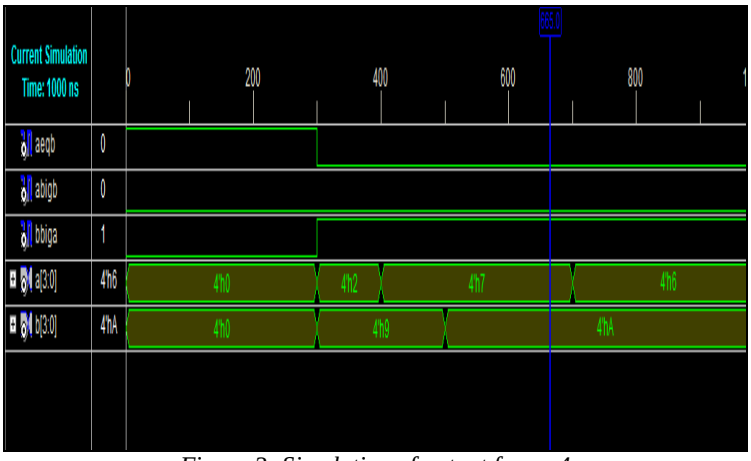

Figure 3: Simulation of output for n=4

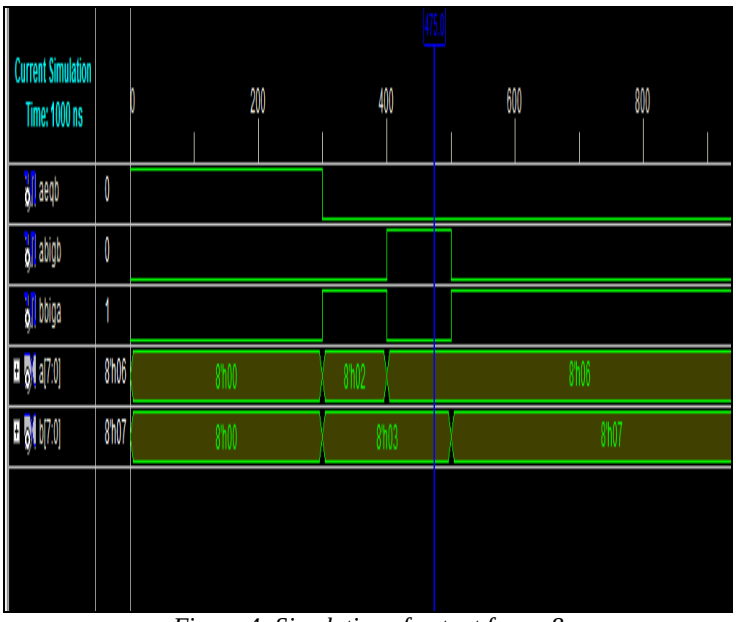

Figure 4: Simulation of output for n=8

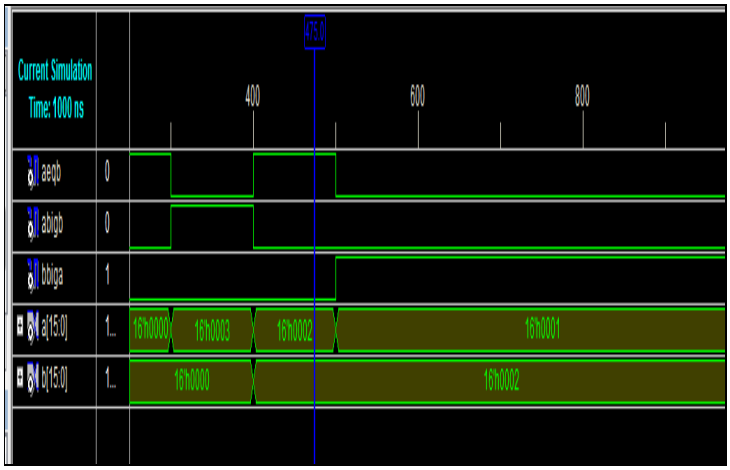

Figure 5: Simulation of Output for n=16

6. Conclusion

A new methodology useful to design binary comparators in QCA has been presented. It is based on innovative that increased speed performances and reduce overall size. The QCA based binary comparator utilizing decision block and CLA technique is proposed in this brief. The inputs are split into groups and checking for equality starts from XOR operation of MSB group first. If

MSB group is equal the checking proceeds to the next successive group towards LSB. On the other hand if any group is not equal the group is processed by an encoder block to find the greater of the two using carry out signal of CLA addition. The results demonstrate better performance of the proposed binary comparator in terms of power and area reductions.

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