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Implementing Multiple Sensors' TIM to Multi -Utility FPGA

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Abstract:
A real time implementation of interfacing multiple sensors to Transducer Interface Module is a challenging yet enthusiastic task on an FPGA like platform. This paper discusses the means of producing multiple sensors' integrated output through FPGA . Apart from the capability of real-time sensing ,a means of providing a single chip solution is also captivated. Tackling the needs of adhering to IEEE standards and meeting to the requirements of bringing in reconfigurability of smart sensors is focused .The inter operability and connectivity characteristics of ADC' and FPGA' are tested to nurture the effectiveness of interfacing modules. This Transducer Interface Module(TIM) thereby supports multiple nodes and dynamic plug and play characteristics, that is an all time solution to the present day industrial needs.

Keywords*: TIM-Transducer Interface Module; Multiple sensors,TEDS-Transducer Electronic Data Sheet*

1. Introduction

The necessity for improvement at the application level of sensing devices/sensors is ever growing. Sensors and sensing devices find trouble coping with standards and in forming conversions with accuracy and effectiveness . In interlinked and interchangeable situations the issues with interoperability and reconfigurability needs to be tackled with more efficient coding constructs. The success will lead way for achieving interlinking of multiple sensors with better interfacing standards. The need for adhering to IEEE standards is accepted with diligence.

IEEE-1451 is one such evolving standard that is to be considered while constructing modules that realize the functioning of multiple sensors.FPGA is most advantageous and most suitable platform that provides (reconfigurability and flexibility) the future sensor networks a most desirable restructuring and recreating base for achieving new heights in implementational standards .

Any attempt to redefine and structure simpler architectures with better prospects, for further miniaturization is a worthy try and is indeed a fair attempt for the ever growing industrial needs.

2. Existing Architecture

For redefining an architecture , a basis IEEE standard architecture has to be chosen so as to adhere to the existing acceptance of interfaces and thereby create a possibility of an easy shift to the newly proposed architecture for better prospects.

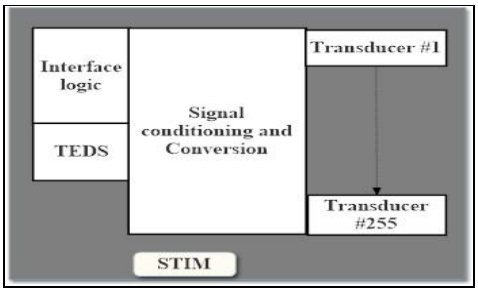

Figure 1: Interfacing architecture proposed by P1451.2 standard

3. Recent Work

On the assertion of venturing into interfacing smart sensor networks and nodes with FPGA's, it is important to sneak through the major theoretical and practical implementations this field has witnessed, right from the initial stages of invent of the concept up till all those phases that are relevant with the subject of discussion are covered. A literary survey on the same is presented below:

- The article of 'Eugene Y. Song and Kang Lee- IEE standards [1]' introduces the IEEE 1451 standard for networked smart transducers highlighting the concepts of smart transducers, IEEE 1451 smart transducers, the architecture of the IEEE 1451 family of standards, application of IEEE 1451, and example implementations of the IEEE 1451 standards

concluding to say that the IEEE 1451 suite of standards provides a set of standard interfaces for networked smart transducers also helping to achieve sensor interoperability for industry and government.

- In the international conference on CS&E (ICCSE 2013),the paper [2]' comes up with a successful architecture for interfacing smart sensor to an independent network. Adhering to IEEE standard this newly defined architecture has laid a platform for showcasing successful message transfer through TEDS segment command built into the FPGA memory block. The importance of testing the TIM under a practical situation is stressed alongside.
- The interfacing of a sensor node to TIM' in turn with an Network capable application processor ,with a refined architecture is presented. Stepping on this basis it becomes effective in introducing redefined architecture in increasing the number of sensors.
- The paper also examines message transfers at different baud rates and an implementation direction onto FPGA necessitating the need of testing the frequencies that best suites each TIM and interfacing FPGA
- The synopsis on [3]' discusses the objectives of the IEEE 1451 that contains one approved and three proposed standards for successful smart transducer communication-as to how the implementation best be used and who benefits from it.
- It highlights the interfacing problems that exists in the real world applications describing how IEEE-p1451 standards with digital protocols and interfaces provides sensors producers and integrators a sigh of relief in aiding for the development of network independent solutions for distributed measurement and control applications.
- The paper on interfacing Time critical mobile functions[4]' shows specs about the necessities and advantages of interfacing arrays of sensors on to a more reconfigurable unit like that of a Lattice semiconductors' FPGA that best provides with lesser power consumption ,flexibility and reconfigurable options overcoming with the existing limitations of single end transducer interface module.
- The paper however fails to provide any interfacing details but is still a worthy go through for motivational content, also fair to quote a part of its conclusion that a new class of low and ultra low-density FPGAs can offer designers a more exciting opportunity to offload sensor management functions from power-hungry applications processors and, thereby in the process, drive down mobile system power consumption, cost and size.
- Jeff Burch Agilent technologies[5]' have charted out an overview of two IEEE standards (1451 and 1588) with bolder block diagrams of generic model of sensors and templates of 1451 architecture with distinguishable colors that can give a good kick start in understanding the basics of proposed IEEE architecture also briefing on the contrasts of 1588 standard and its nearer evolving p-1451 standards.
- The paper on Wireless Sensor Networks in Permafrost Research [6]' outlines practicality in implementation of wireless sensor networks, the importance and necessity of proper synchronisation highlighting the need for development of code efficient (software) and low power utilisation devices. The requiremental thongs and challenges in this aspects are briefed .
- The 'Data Acquisition Handbook'[7]' explains with clarity the importance and contexts of TEDS (Transducer Electronic Data Sheets) .The purpose of its presence and the structural formats as to how it must be used in interfacing is explicitly mentioned.
- The signal conditioning of general-purpose systems from the stages of conversion to decision logics is outlined within its context.
- In another survey report on 'Sensor Systems Based on FPGAs and their Applications' [8]', a brief analysis of sensor nodes ,their challenges in interfacing to boards, effectiveness of FPGA over other computational processors, trends in wireless sensor networks and scope of development of use of multiple sensors in this purview is reported.
- Another Paper [9]' presents an approach for providing reconfigurability in sensor nodes wireless communication. The capability of FPGA for interfacing multiple ICs via I2C enabled communication is discussed . The ability to interface smart sensors on a single chip reconfigurable device and provide multiple configurability options w.r.t communication network is emphasized.

With all this relevant platforms setup it becomes easier to work on an higher challenge of integrating multiple sensors and building a real time work environment that provides simultaneous and real-time outputs.

4. Methodology

Block Diagram

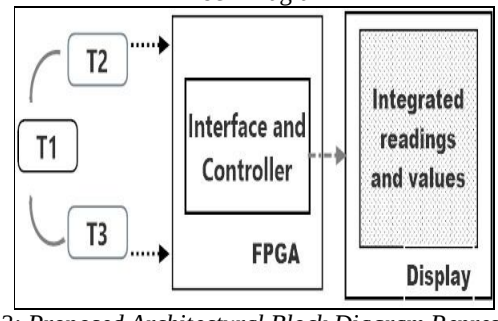

Figure 2: Proposed Architectural Block Diagram Representation

T1, T2 ,T3 are the interfacing transducers (in this case the three sensors : Temperature, Pressure and a Potentiometer for instance) that are to be interfaced to FPGA.
Choice of sensors is carefully made to suit the design and to suffice the clear interfaceary requirement for the demonstration purpose, though the design is capable of being interfaced with most of such similar sensors availble in the market today. The number of transducers that can be simultaneously interfaced to the FPGA board is limited only by the channels supported by the ADC.
ADC0808/ADC0809 supports upto eight channels.Ports are defined accordingly and the sensors are channelled into the ADC.
To interface these sensors effectively to the FPGA, a sensitive interface module like that of a 'TIM' that is designed, is incorporated as the 'Interface and Controller' module/part(Figure 3) into the FPGA.The complete control of information right from the sensing stage to the output display stage , is embedded as software constructs into this part.
The interface controller part contains individual modules that guide the sensory information to all the succesive stages of processing. From conversion to data acquisition; from detection to decoding ; from mapping to placing it on UART and computer display, each of these is individually coded and processed on multi utility FPGA platform.
The produced output is mapped on to seven-segment displays of FPGA, aswell the ROM outputs TEDS information on to the PC. The outputs thus obtained are simultaneously available that solves the problem statement concerning to interfacing multiple sensors and extracting outputs simulataneously.
This raw outlook of sensors interfacing has to be dealt deeply within, describing its inner modules , individually highlighted

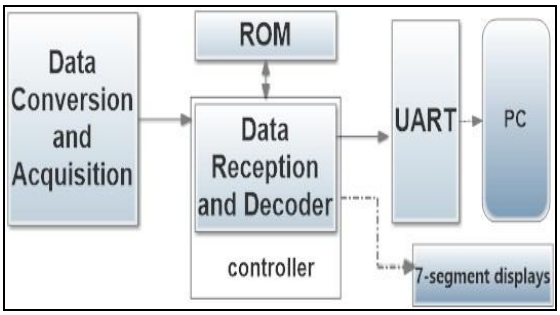

Figure 3: The Interface Controller Block Diagram

In Figure (3) the interface controller unit consists of several processing modules that perform all the requisites to output user friendly values/information.
The sensors input values are subjected to Digital conversion (ADC0809).This raw information and data are recepted , stored in suitable registers.ROM is then looked up for matching these values to suitable user defined-conversions and mapped ,to obtain desired suitable values . Alongside, ROM is also looked up for stored 'Transducer Electronic Data Sheet' values -the basic information relating each transducer and these values are placed onto UART that transmits it to the display screen. Obtained simultaneous output values can also be displayed on the seven segment displays (Only those FPGA's that support for multiple segment display and a minimum of four required)
The above design also supports for Duplex information Processing and to suffice this a relay circuit can also be connected and be proved.

5. Process Flow Representation:

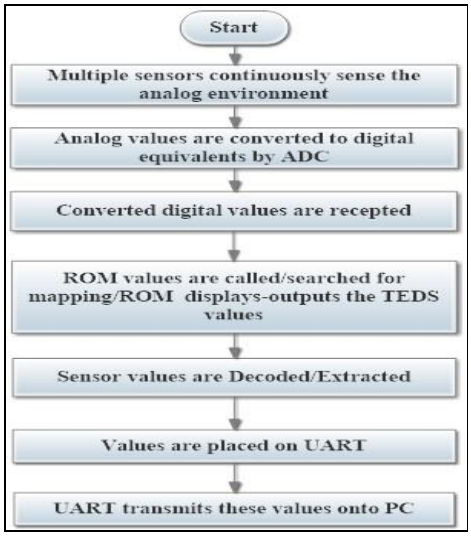

Figure 4: Process Flow Representation

As the execution begins, multiple transducers (three sensors in our case) starts capturing the information from the environment specific to each sensor. The information captured are continuous real time values and are thus analog in nature. These values cannot readily be utilized for further processing and has to be converted to its digital equivalent

This conversion called the analog to digital conversion is performed by ADC convertors. Each input value is sampled across specific intervals of predefined time. Each sample constitutes to become its equivalent digital values. 0808 ADC performs this conversion in our case. These converted values must be recepted accordingly by making use of suitable registers

The recepted values are the raw information that has no clue whatsoever with our output and interfaceables. These values are to be decoded to ascertain their content in the prospective future. To do so, a decoding construct is being used that extracts the values as ASCII characters (for experimental purpose) and outputs an equal value that is necessary for information processing.

These values are sent through UART to be displayed on the PC. Alongside the TEDS data of these individual transistors are fetched from ROM memory and are ready to be further placed on UART to display these values on the PC.

The UART transfers parallel data packets through a serial line following the RS-232 standard. Typically, a UART consists of a transmitter, a receiver, transmit and receive data buffer (Tx buffer, Rx buffer). UART performs the transmission/reception of these information from Sensors/actuators respectively.

6. Results and Discussion

Individually the modules are designed, synthesized and simulated and found to have been working Successfully.

Of all the constructs, the most important ones are of :

ADC, Main Controller and UART

All these modules gave definitive outputs with respect to each sensor as well when connected together.

Multiple sensors have been successfully Interfaced. Real Time Analog values are sensed, converted to equivalent digital values, decoded, mapped with ROM values and obtained at seven segment displays.

Alongside TEDS values are extracted and placed on UART to display on the terminal window of PC. The table below shows the resource utilisation summary on a Xilinx platform.

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	81	4656	1%
Number of Slice Flip Flops	125	9312	1%
Number of 4 input LUTs	95	9312	1%
Number of bonded IOBs	22	232	9%
Number of GCLKs	1	24	4%

Table 1: Synthesis Report Of Device Utilization Summary

7. Conclusion

Real time multiple sensing is no more a probability but a practical reality. This possibility has been witnessed at the implementation level of interfacing of sensors . Making use of reconfigurable platform like that of an FPGA for achieving better interfaceary standards, has been of great advantage. Meeting the requirements of present day Sensor technology , efficiently working Transducer Interface modules ,can become an inspiration for meeting further challenges , setting aside hindrances and in taking a step forward towards the growth of this technology .

8. Acknowledgment

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9. References

1. Understanding IEEE 1451—Networked Smart Transducer Interface Standard Eugene Y. Song and Kang Lee.
2. A Single-Chip Solution for Interfacing Transducers to Sensor Networks Using FPGAs by M.D.R. Perera, R.G.N. Meegama and M .. K. Jayananda.
3. A Synopsis of the IEEE P1451- Standards for Smart Transducer Communication Kang Lee National Institute of Standards and Technology.
4. An FPGA Approach to Implementing Time-Critical Functions in Multi-Sensor Mobile Designs A Lattice Semiconductor White Paper.

5. Overview of IEEE 1451 and IEEE 1588 for Distributed Measurement and Control Applications Jeff Burch Agilent Technologies
6. Wireless Sensor Networks in Permafrost Research: Concept, Requirements, Implementation, and Challenges by Andreas Hasler , Igor Talzi, Jan Beutel , Tschudin , Stephan Gruber
7. The 'DATA ACQUISITION HANDBOOK'-'A Reference for DAQ And Analog & Digital Signal conditioning'.
8. 'Systems Based on FPGAs and Their Applications' The article of 'Eugene Y. Song and Kang Lee- IEE standards.
9. Mapping a Sensor Interface and a Reconfigurable Communication System to an FPGA Core by Volodymyr Kindratenko, David Pointer
10. ADC0808/ADC0809 8-Bit micro Processor Compatible AD Converters with 8-Channel Multiplexer