THE INTERNATIONAL JOURNAL OF SCIENCE & TECHNOLEDGE

Implementation of Reconfigurable, Coding-Efficient All Digital RF-Transmitter

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Abstract:
A new reconfigurable, coding efficient digital RF-Transmitter Architecture has been designed. The current approach uses different pulse shaping techniques and flexible Digital frequency Synthesizer which effectively increases coding efficiency of the system. Here we mainly address two key limitations of the previous architectures, poor coding efficiency and lack of re-configurability. The current architecture combines a maximum coding efficiency and fully reconfigurable while maintaining the high flexibility inherent to the all-digital RF-transmitters. The RF output carrier signal operating at Mega Hertz frequency range is generated. The obtained results also show the feasibility and potential of using reconfigurable digital RF-Transmitter architecture on FPGA.

Keywords: *RF-Transmitter, Digital frequency synthesiser, pulse shaping techniques-Pulse width modulation*

1. Introduction

Digital RF Transmitter basically is that transmitters for which the input is digital. It receives serial data and transmits it wirelessly through its Antenna. Transmission occurs usually at the rate of 1Kbps-10Kbps. Transmitted data is received by an RF receiver operating at same RF frequency as that of transmitter. Digital approaches are used to replace traditional analog RF transmitters and enhance integration, configurability, performance and reduce power consumption and hence to design fully configurable transmitter.

A key challenge for achieving such a new transmitter paradigm involves the development of a very flexible physical layer in order to support the transmission of multiband, multi-rate and multi-standard signals, which in practice is very hard to implement using conventional approaches. Nevertheless, the last advances in this field include the development of novel all-digital transmitters where its data-path is digital from the baseband up to the RF stage. Such a concept has inherent high flexibility and poses an important step towards the development of SDR transmitters. Moreover, this new approach enables the use of field-programmable gate array (FPGA) devices for implementing the RF transmitter, which provides additional flexibility as well as field upgradeability. In fact, current FPGAs have an equivalent logic capacity of millions of logic gates in addition to large RAM blocks, embedded processors, DSP modules and multi-gigabit I/O standards. If efficiently explored, these valuable resources can be used to enable the development of reconfigurable all-digital transmitters.

2. Related Work

RF digital Transmitters have very closer proximity to Software defined radio and Cognitive radio. We have much architecture for both SDR and Cognitive Radio. All transmitters uses different architecture for transmission of digital data. There are many advantages and loopholes for those different architectures. And some of those previous architectures and their drawbacks are discussed below.

"An FPGA based all-digital transmitter with RF for SDR"[1]. It is an FPGA-based digital transmitter for SDR where data is shaped using pulse width modulation (PWM) and up-converted to 800MHz using a digital mixer. In this SDR technology permits wireless infrastructures and makes radio to support multiple air-interfaces, by using reconfigurable hardware platform. The all-digital transmitter uses the PWM technique such that the RF signal with the binary format may be directly synthesized in digital domain. The above mentioned digital transmitter architectures are still very restrictive for developing a truly SDR-based system. The restrictiveness of Architecture to SDR can be reduced furthermore with other pulse shaping techniques. The multiple air-interfaces are retained for multi-band transmission of the signal.

"A novel architecture of delta-sigma modulator enabling all-digital multiband Multi-standard RF transmitters design,"[2] The project describes a new transmitter approach using low-pass modulators and digital multiplexers to design an all-digital multimode RF transmitter. In this approach the modulator shape baseband signals using Delta Sigma modulation, which significantly lightens the processing speed requirements, and therefore simplifies the design of Sigma Delta-based transmitters for operation in the microwave frequency range. The concept of newness lies within the implementation of a selected totally digital

up-conversion together with a low-pass Delta Sigma modulator to supply high-frequency digital-like signals, which might be wont to drive extremely economical switching-mode power amplifiers. The projected design is appropriate for reconfigurable all-digital, multi-standard and multiband wireless transmitters. But the above presented transmitters require very high-quality filters to remove out-of-band noise, others only. And the multi band multi-channel feature is exclusively extracted from the current approach. The more complex Delta sigma modulator can be replaced with some other modulation technique.

"Low pass Delta-Sigma modulators with digital up-conversion"[3]. It presents a low-pass based transmitter front-end also using external multiplexers for implementing the digital up-conversion to RF. ΔΣ modulation is utilized to come up with associate RF signal appropriate for driving extremely economical switching-mode power amplifiers. The full frontend is enforced within the digital domain up to the up-conversion. This architecture generates low RF frequencies, require expensive external multiplexers for implementing the RF up-conversion and have carriers with low SNR. The above mentioned paper supports mostly low frequency generation. Hence for high frequency generation, we go for an alternate better method. The highly complex sigma-delta modulator can be replaced with less complex modulator. Overall performance and coding efficiency can be improved by varying better methods of frequency generation and modulation techniques.

"RF transmitter architectures and Circuits"[4]. The above paper shows different transmitter architectures and different modulation techniques such as direct conversion method, two step transmitter, offset PLL architectures etc.. All the above mentioned architectures have so many loopholes in terms of efficiency, error vector, matching network problem. Hence to overcome all these problems, reconfigurable transmitter architecture should be designed. The architecture mentioned here considers the drawbacks of a number of other architectures, recognizes the solution sand comes up with a code efficient, flexible, and re-configurable design. The merits of some of the architectures are retained and a new transmitter is structured.

3. Methodology And Implementation

The block diagram of proposed architecture is as shown in figure . The input signal which is either 0^0 phases or 180^0 phase is generated by mapping. The phase shift is done using Binary Phase Shift Keying. The shifted signal is then modulated using any of the suitable modulation schemes. The proposed architecture uses the conventional method of generating a PWM modulated wave by comparing the message signal with a ramp waveform using a comparator. And it also uses the method of Random Pulse Width Modulation which is another modulation technique. Then the modulated wave is multiplied with the local oscillator signal. Here, Local oscillator is replaced with a flexible Digital Frequency Synthesizer(DFS) which is suitable for all frequencies. According to the frequency of DFS, Output is generated. Then that resulting signal is fed to select and combine and according to select line which is represented by counting value of 5-bit counter output is taken from serialiser.

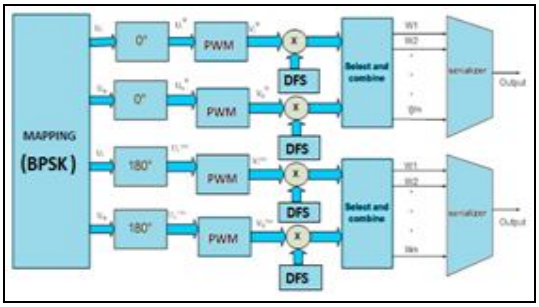

Figure 1: Proposed Block diagram

3.1. Binary Phase Shift Keying : BPSK

In PSK (Phase Shift Keying), the phase of a wave either sine or cosine wave is changed according to the binary signal level. The proper information about the bit stream is contained in the phase changes of the transmitted signal. Usually, if the bitstream is '0' there will not be any phase shift in the wave. If the value in the bitstream contains '1', then there will be a phase shift in a wave. For instance to transmit the signal "0" and signal "1", PSK signals can be written in the form of equations as follows:

$$\Phi_0(t) = A\sin(w_o t + \theta_0)$$
$$\Phi_1(t) = A\sin(w_1 t + \theta_1), 0 < t < T_s,$$

Where, θ_1 and θ_2 are constant phase shifts, 't' is a time interval, w_0, w_1, are frequencies.

Figure 2:Block diagram of BPSK

The implementation of BPSK is as shown in figure-2. A single bit binary data can either be '1' or '0'. According to clock pulse and reset bit, we will get either 12-bit real or 12 bit imaginary output. The information regarding the bit stream is contained within

the changes of phase of the transmitted signal. According to the binary data, input's phase is shifted and output is obtained. In binary phase shift keying, phase shift from input to output is about 180^0.

3.2. Pulse width modulation

PWM is a modulation technique where in Period of pulses are constant but their duty cycle varies according to the amplitude of the modulating signal. The conventional method of generating a PWM modulated wave is to compare the message signal with a ramp waveform using a comparator. The implemented PWM block has 32 bit input and single bit output. The address generator is of 4-bits. When Write enable is equal to '1' and if n-bit address line is taken, for every nth bit, the PWM output is taken. The serial data of PWM purely depends on clock and reset.

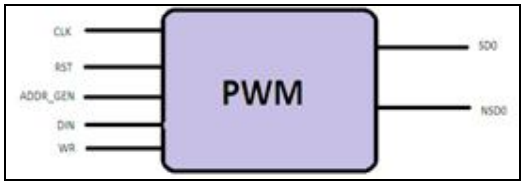

Figure 3: Block diagram of PWM

The implemented block has 32 bit input and single bit output. The address generator is of 4-bits. When Write enable is equal to '1', if a n-bit address line is taken, for every nth bit, the PWM output is taken. The serial data of PWM purely depends on clock and reset.

3.3. Random Pulse width modulation

The Random Pulse Width Modulation is also one of the modulation techniques. Here switching periods of pulses are varied in a random manner, the sampling frequency remains same as that of PWM and it is equal to the reciprocal of the average switching period. This makes us to replace a traditional PWM with the random PWM (RPWM) where ever it is necessary. The same RPWM method and device can easily be adapted for the control of many other pulse-width modulated power electronic devices, such as the dc-to-dc converting switching power supplies or rectifiers which converts ac to dc. Applications of Random PWM are mainly used in Power Delivery and Conversion system and Voltage Regulation.

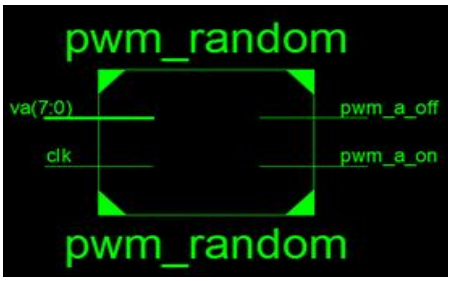

Figure 4: Block diagram of PWMRND

The Block diagram representation of random PWM is as shown in the above RTL schematic. According to the 8-bit input value and input clock, output is taken. The input bits are selected randomly that is, the output will be '1' for certain number of bits and it will be '0' for another set of bits. The process is done by incrementing counter bit value according to the input. The other features are same as PWM.

3.4. Digital frequency synthesiser

The basic DFS consists of a phase accumulator and a phase to amplitude converter (conventionally a sine ROM) blocks and the respective block diagram is shown in fig.3.8. The phase accumulator consists of a 'j' bit frequency register. It stores a digital phase increment word. Then it is followed by a 'j' bit full adder and a phase register. The resulting digital phase increment input word is entered in the frequency register. This data is additional to the data antecedent held within the phase register at every clock pulse. The phase increment word represents a phase angle step that is additional to the previous value at every $(1/f_{clk})$ second to produce a linearly increasing phase value. The phase is generated by modulo 2^j overflowing property of a phase accumulator. The rate of overflow is taking into account as the output frequency, that is expressed as

$$fout = \frac{\Delta P f clk}{2^j}$$

P =1 as the phase increment word, then the output frequency is expressed as,

$$fout = \frac{fclk}{2^j}$$

The information of digital phase is converted into the values of a sine wave from the ROM, which is stored in sthe look-up table.

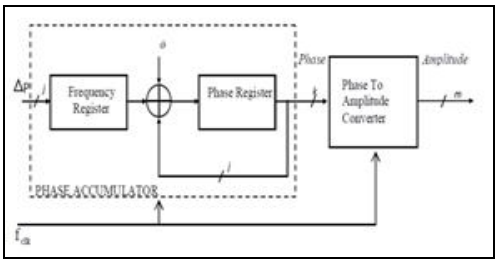

Figure 5: Block diagram of DFS

4. Results And Discussion

Individual modules of the project are designed, synthesized and outputs are taken. The important modules are BPSK, PWM, PWMRND, DFS. All modules gave satisfactory output. The Comparative results between two modulation schemes i.e., PWM and Random PWM is as shown in table-1 It shows maximum utilization of all device resources for FPGA-SPARTAN-3.

FPGA Resources for SPARTAN3S-400 series	**PWM**	**PWMRND**
Number of Slices	268(7%)	376 (10%)
Number of Slice Flip Flops	228(3%)	234(3%)
Number of 4 input LUTs	552 (7%)	724 (10%)
Number of bonded GCLK's	1 (12%)	1 (12%)
Number of IOB'S	6 (4%)	6 (4%)

Table 1:Comparitive Table for PWM and Randomised PWM for SPARTAN-3

The Comparative results between two modulation schemes i.e., PWM and Random PWM is as shown in table It shows maximum utilization of all device resources for FPGA-VIRTEX-6.

FPGA Resources for VIRTEX6-HX380 series	**PWM**	**PWMRND**
No. of slice registers	33 (0%)	171 (0%)
No. of slice LUT's	105 (0%)	480 (1%)
No. of fully used LUT-FF Pairs	33 (31%)	169 (35%)
No. of bonded IOB's	29 (4%)	6 (2%)

Table 2: Comparitive Table for PWM and Randomised PWM for VIRTEX-6

5. Conclusion

The Reconfigurable, coding-efficient RF Transmitter architecture is proposed. It is carried out using different pulse shaping techniques; PWM and Random PWM. It combines multichannel data transmission with high flexibility and high coding efficiency. The usage of Digital Frequency synthesizer makes the design to be reconfigurable. BPSK a technique to map the inputs make the architecture to consume less memory.

From the analysis of two different modulation techniques it has been clearly concluded that, PWM with pattern randomization has higher complexity in circuit design. However it utilizes only 10% of FPGA resources and still provides efficient output, While PWM utilizes just 7% of the device and is less complex.

The obtained result also shows the digital output transferred at high rate with maximum frequency of 295.95 MHz and maximum timing delay of 3.379ns. It has feasibility and potential of using FPGA-based poly-phase multipath architectures for implementing digital RF transmitters.

6. Acknowledgment

I would like to express my heartfelt gratitude to my Guide Mr. Naveen Kumar G N, Assistant Prof, Electronics And Communication Engineering, CMR Institute of Technology, for his timely advice on the technical support and regular assistance

throughout the review work.

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