INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN: 2278 – 0211 (Online) / 2278-7631 (Print)

Design and Implementation of Zigbee Transreceiver using CMOS Architecture

Bhawna
Student, Vaish College, Rohtak, India

Chetna Bhardwaj
Assistant Professor, SPIET, Rohtak, India

Abstract:
There is always the requirement of efficiency enhancement in each architecture. If the hardware based architectures are optimized, It will enhance the complete system. The proposed work is in same direction to reduce the power consumption in the construction of Zigbee Transreciever. The proposed work is the implementation of Zigbee based transceiver system with CMOS technology. We are proposing the implementation of in Active HDL simulation environment. We have to study and perform the analysis of zigbee protocol respective to the packet loss and the throughput in the environment. We will also analyze the power consumption rate in the network. The proposed system is analysis of QPSK modulation. In this system we will implement the phase error to analyze the reliability of the system.

Keywords : *Wireless Network, Zigbee, CMOS, Transreciever, Optimization*

Introduction

ZigBee is the name of a specification for a suite of high level communication protocols using small, low-power digital radios. The technology is intended to be simpler and cheaper than other WPANs such as Bluetooth. The most capable ZigBee node type is said to require only about 10% of the software of a typical Bluetooth or Wireless Internet node. The estimated cost of the radio for a ZigBee node is about $1.10 to the manufacturer in very high volumes. Most ZigBee solutions require an additional microcontroller driving the price further up at this time. ZigBee is the newest and provides specifications for devices that have low data rates, consume very low power and are thus characterized by long battery life. Other standards like Bluetooth and IrDA address high data rate applications such as voice, video and LAN communications.

The target networks encompass a wide range of devices with low data rates in the Industrial, Scientific and Medical (ISM) radio bands, with building-automation controls like intruder/fire alarms, thermostats and remote (wireless) switches, video/audio remote controls likely to be the most popular applications. So far sensor and control devices have been marketed as proprietary items for want of a standard. With acceptance and implementation of ZigBee, interoperability will be enabled in multi-purpose, self-organizing mesh networks

1. ZigBee-style networks began to be conceived about 1998, when many engineers realized that both WiFi and Bluetooth were going to be unsuitable for many applications. In particular, many engineers saw a need for self-organizing ad-hoc digital radio networks.
2. The IEEE 802.15.4 standard was completed in May 2003.
3. In the summer of 2003, Philips Semiconductors, a major mesh network supporter, ceased its investment. Philips Lighting has, however, continued Philips' participation, and Philips remains a promoter member on the ZigBee Alliance Board of Directors.
4. The ZigBee Alliance announced in October 2004 that its membership had more than doubled in the preceding year and had grown to more than 100 member companies, in 22 countries. By April 2005 membership had grown to more than 150 companies.
5. The ZigBee specifications were ratified on 14 December 2004.

6. The ZigBee Alliance announces public availability of Specification 1.0 on 13 June 2005

The "Why ZigBee" question has always had an implied, but never quite worded follower phrase "…when there is Bluetooth".

The bandwidth of Bluetooth is 1 Mbps; ZigBee's is one-fourth of this value. The strength of Bluetooth lies in its ability to allow interoperability and replacement of cables, ZigBee's, of course, is low costs and long battery life. In terms of protocol stack size, ZigBee's 32 KB is about one-third of the stack size necessary in other wireless technologies (for limited capability end devices, the stack size is as low as 4 KB).

Most important in any meaningful comparison are the diverse application areas of all the different wireless technologies. Bluetooth is meant for such target areas as wireless USB's, handsets and headsets, whereas ZigBee is meant to cater to the sensors and remote controls market and other battery operated products. In a gist, it may be said that they are neither complementary standards nor competitors, but just essential standards for different targeted applications. The earlier Bluetooth targets interfaces between PDA and other device (mobile phone / printer etc) and cordless audio applications.

ZigBee is designed for remote controls and sensors, which are very many in number, but need only small data packets and, mainly, extremely low power consumption for (long) life. Therefore they are naturally different in their approach to their respective application arenas

Literature Survey

Anew low-voltage high performance CMOS I-bit Tramsreciever circuit is proposed. The new design is derived by combining XOR (XNOR) gatcs used in the conventional Tramsreciever [I] and transmission gates developed in [Z]. The proposed Tramsreciever can provide full voltage swing **at** a low supply voltage and offers superior performance in both power and speed than the conventional Tramsreciever [I], the transmission Tramsreciever [Z], and thc low-voltage Tramsreciever 131[9]. The sum and carry generation circuits of the proposed Tramsreciever are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem. As Tramsrecievers are frequently employed in a tree structured

configuration for high-performance arithmetic circuits, a cascaded simulation structure is introduced to evaluate the Tramsrecievers in a realistic application environment. A systematic and elegant procedure to scale the transistor for minimal power-delay product is proposed. The circuits being studied are optimized for energy efficiency at 0.18-mCMOSprocess technology. With the proposed simulation environment, it is shown that some survival cells in stand alone operation at low voltage may fail when cascaded in a larger circuit, either due to the lack of drivability or unsatisfactory speed of operation. The proposed hybrid Tramsreciever exhibits not only the full swing logic and balanced outputs but also strong output drivability. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout. Therefore, it remains one of the best contenders for designing large tree structured arithmetic circuits with reduced energy consumption while keeping the increase in area to a minimum[10]. With the characteristics of full voltage swing at internal nodes and very low short circuit current, HSPICE and Nanosim simulations shown that the proposed Tramsreciever offers a power-delay improvement of 36% over the best of other 1-bit Tramsrecievers that were compared. A 0.35μm CMOS technology and a power supply of 3.3.V were used to simulate these adders. When used to build an 8-bits carry-ripple adder, the proposed Tramsreciever offers power savings up to 28% respect to the other ones[11]. By using hybrid various CMOS and pass transistor logic (PTL) design approaches, two novel low-power full-swing Tramsreciever cores with output driving capability are proposed for high-performance embedded structure. The main design objectives for these Tramsreciever cores are providing not only low power and high speed but also full-swing operation at a low supply voltage and the driving capability. The simulation results show that the proposed Tramsreciever core (design-1) is superior to other designs. It consumes 17.69% to 36.21% less power than three previous designs excluding 7.87% penalty than CMOS scheme, while it is 1.88% to 53.64% faster for sum and 11.64% to 40.67% faster for carry-out than all reference Tramsrecievers[12].

The software is designed to be easy to develop on small, cheap microprocessors. The radio design used by ZigBee has been carefully optimized for low cost in large scale production. It has few analog stages and uses digital circuits wherever possible. Even though the radios themselves are cheap, the ZigBee Qualification Process involves a full validation of the requirements of the physical layer. This amount of concern about the Physical Layer has multiple benefits, since all radios derived from that semiconductor mask set would enjoy the same RF characteristics. On the other hand, an uncertified

physical layer that malfunctions could cripple the battery lifespan of other devices on a ZigBee network. Where other protocols can mask poor sensitivity or other esoteric problems in a fade compensation response, ZigBee radios have very tight engineering

The new hybrid Tramsreciever is composed of pass-transistor logic and static CMOS logic. The main design objectives for the Tramsreciever core are providing not only low power and high speed but also with driving capability. Using TSMC CMOS 0.35-μm technology, the characteristics of the experimental circuit compared with prior literature show that the new adder improves 1.8% to 35.6% in power consumption, 11.7% to 41.2% in time delay of *Co*, and 13.7% to 91.4% in power-delay product of *Co*. The circuit is proven to have the minimum power consumption and the fastest response of carry out signal among the adders selected for comparison. Due to the low-power and high-speed properties, both the new exclusive OR circuit and the new Tramsreciever can be efficiently integrated in a system-on-a-chip (SoC) or an embedded system[14]. A new structure of a hybrid Tramsreciever, namely, the branch-based logic and pass-transistor (BBL-PT) cell, which we implemented by combining branch-based logic and pass-transistor logic. Evolution of the proposed cell from its original version to an ultralow-power (ULP) cell is described. Quantitative comparisons of the optimized version, namely, the ULP Tramsreciever (ULPFA), are carried out versus the BBL-PT Tramsreciever and its counterparts in two well-known and commonly used logic styles, i.e., conventional static CMOS logic and complementary pass logic (CPL), in a 0.13μm PD SOI CMOS with a supply voltage of 1.2 V, demonstrating power delay product (PDP) and static power performance that are more than four times better than CPL design. This could lead to tremendous benefit for multiplier application. The implementation of an 8-bit ripple carry adder based on the ULPFA is finally described, and comparisons between adders based on Tramsrecievers from the prior art and our ULPFA version demonstrate that our development outperforms the static CMOS and the CPL Tramsrecievers, particularly in terms of power consumption and PDP by at least a factor of two[15].

Research Methodology

The proposed system is the implementation of the zigbee in cmos technology. The system is infected with the phase error and we will perform an analysis of error rate and the power consumption in ActiveHDL environment. The system will work on QPSK signal. We basic system is presented here. The frequency hopping spread spectrum transmitter has a global clock and reset. The input given is of 8-bits which is then encrypted using the pseudo noise sequence of 8-bits.So the encrypted data is of 8-bits. The transmitted data is of 8-bits length. The basic architecture of proposed work is shown in figure 1.

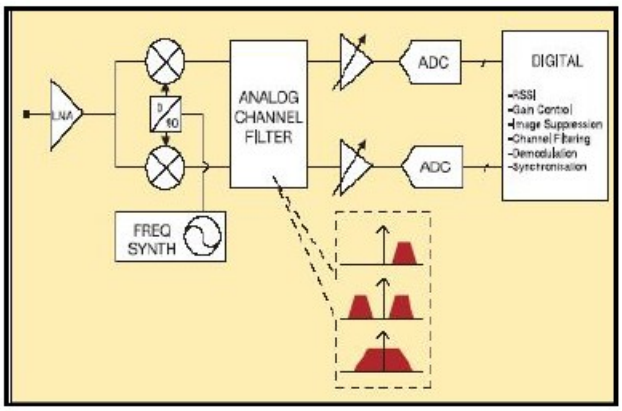

Figure 1 : Proposed Architecture

The transmitter has a global clock and reset. The input given is of 8-bits which is then encrypted using the pseudo noise sequence of 8-bits.So the encrypted data is of 8-bits. The transmitted data is of 8-bits long. Zigbee uses a variation called Gaussian Minimum Shift Keying; Quadrature phase shift keying changes a sine wave's normal pattern. The receiver expects these shifts and decodes them in the proper sequence. Again, we put digital information on a carrier wave. We are shaping a carrier wave to do this, to carry more pulses more efficiently.

The data to be transmitted is given to the modulator input and the shifter unit gets the 8 bit data. This data is then segregated as four Di-bits (00, 01, 10, and 11). The segregation is based on selection input of the splitter block. The Di-bits are given to the multiplexer unit to select the respective Waveforms. The selection Input of the Splitter block is controlled by the Address Generator block.

Tool

VHDL stands for VHSIC (Very High Speed Integrated Circuits) Hardware Description Language. In the mid-1980's the U.S. Department of Defense and the IEEE sponsored the development of this hardware description language with the goal to develop very high-speed integrated circuit. It has become now one of industry's standard languages used to describe digital systems. The other widely used hardware description language is Verilog. Both are powerful languages that allow you to describe and simulate complex digital systems. A third HDL language is ABEL (Advanced Boolean Equation Language) which was specifically designed for Programmable Logic Devices (PLD). ABEL is less powerful than the other two languages and is less popular in industry. This tutorial deals with VHDL, as described by the IEEE standard 1076-1993. Although these languages look similar as conventional programming languages, there are some important differences. A hardware description language is inherently parallel, i.e. commands, which correspond to logic gates, are executed (computed) in parallel, as soon as a new input arrives. A HDL program mimics the behavior of a physical, usually digital, system. It also allows incorporation of timing specifications (gate delays) as well as to describe a system as an interconnection of different components.

Conclusion

In this paper, we have presented construction of a low power transreciever for zigbee protocol for Wireless Sensor Network. The hardware will be implemented using Verilog in Active HDL environment based on CMOS technology. The blocks were designed also using conventional Complementary Metal Oxide Semi-Conductor (CMOS) logic.

Reference

1. Chang T. -S., Chu Y.-H. and Jen C.-W., "Low-power FIR filter realization with differential coefficients and inputs," IEEE Trans. Circuits Syst. II, vol. 47, pp. 137-145, February 2000.
2. Choi J. R., Jang L. H., Jung S. W., and Choi J. H.,"Structured design of a 288-tap FIR filter by optimized partial product tree compression", IEEE Journal on Solid-State Circuits, 32, (3), pp. 468–476, 1997.
3. Dan Wang., Maofeng Yang., Yintang Yang. and Wu Cheng. "Novel Low Power Tramsreciever Cells in 180nm CMOS Technology", IEEE Trans. ICIEA 2009.
4. Eshraghian K. and Weste N. "Principles of CMOSVLSI Design", A system Perspective. Published by Dorling Kindersley (india) Pvt. Ltd., licensees of Pearson Education in South Asia,pp. 304-307, 1993.
5. Morgenshtein A., Fish A, and Wagner I. A. "Gate-Diffusion Input (GDI) – A Power Efficient Method for Digital Combinatorial Circuits: A Design Methodology", 14th ASIC/SOC Conference, Washington D.C., USA, 2001.
6. Mahesh Mehendale, and Venkatesh G. "Low Power Realization of FIR Filters on Programmable DSPs", lEEE Tran, (VLSI Systems) vol.6, no.4, Dec1998.
7. Pearson D. J., Reynolds S. K., Megdanis A. C., Gowda S., Wrenner K. R., Immediato M., Galbraith R. L., and Shin H. J., "Digital FIR filters for high speed PRML disk read channels", IEEE Journal on Solid-State Circuits, 30, (12), pp. 1517–1523, 2005.
8. Shivaling S. Mahant-Shetti, Poras T. Balsara, and Carl Lemonds "High Performance Low Power Array Multiplier Using Temporal Tilting", IEEE Transaction on VLSI systems, vol. 7, No 1, Mar 1999,
9. I-Chyn Wey," A New Low-Voltage CMOS 1-Bit Tramsreciever for High Performance Applications", 0-7803-7363-4/02/02002 IEEE
10. Chip-Hong Chang," A Review of 0.18-_m Tramsreciever Performances for Tree Structured Arithmetic Circuits", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1063-8210© 2005 IEEE
11. M. Aguirre Hernández," A Low-Power Bootstrapped CMOS Tramsreciever", 2nd International Conference on Electrical and Electronics Engineering (ICEEE) and XI Conference on Electrical Engineering (CIE 2005) 0-7803-9230-2/05©2005 IEEE

12. Chiou-Kou Tung," High-Performance Low-Power Full-Swing Tramsreciever Cores with Output Driving Capability", 1-4244-0387-1/06©2006 IEEE
13. Jin-Fa Lin," A Novel High-Speed and Energy Efficient 10-Transistor Tramsreciever Design", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS1549-8328© 2007 IEEE
14. Chiou-Kou Tung," A Low-Power High-Speed Hybrid CMOS Tramsreciever for Embedded System", 1-4244-1161-0/07©2007 IEEE
15. Ilham Hassoune," ULPFA: A New Efficient Design of a Power-Aware Tramsreciever", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS1549-8328© 2010 IEEE
16. Omid Kavehei," Design of Robust and High-Performance 1-Bit CMOS Tramsreciever for Nanometer Design", IEEE Computer Society Annual Symposium on VLSI 978-0-7695-3170-0/08© 2008 IEEE
17. I.F. Akyildiz, William Su, Sankarasubramaniam, E. Cayirci, A survey on sensor networks, IEEE Communications, Aug 2002.
18. K.S.J. Pister, J.M. Kahn and B.E. Boser, "Smart Dust: Wireless networks of millimeter scale sensor nodes", 1999.
19. L.Doherty, B.A. Warneke, B.E.Boser, K.S.J.Pister. Energy and performance consideration smart dust, 2001.
20. Ioannis Chatzigiannakis, Athanassios Kinalis, Sotiris Nikoletseas, Power Conservation Schemes for Energy Efficient Data Propagation in Heterogeneous Wireless Sensor Networks.
21. Azzedine Boukerchey Ioannis Chatzigiannakis zx Sotiris Nikoletseaszx, Power-Efficient Data Propagation Protocols for Wireless Sensor Networks, February 28, 2005.
22. IEEE Std 802.15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs), 2003.
23. A. Alheraish, "Design and implementation of home automation system," IEEE Trans. on Consumer Electronics, vol. 50, no. 4, pp.1087-1092, Nov. 2004