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FPGA Based GPS Data Acquisition And Processing System

N.Mohammad subhani
M.Tech Student, Department of ECE, Prakasam Engineering College, kandukur, India

R.Giri Prasad
Associate professor, Department of ECE, Prakasam Engineering College, kandukur, India

Abstract:

Global Positioning System (GPS) is a space-based global navigation satellite system. It provides time and location information to users anywhere on the Earth. The GPS receivers are placed in any embedded systems to continuously calculate current time, velocity and location information. Hence, real-time synchronous systems can be designed. The GPS receiver module is used for getting the location and time information in a predefined message frame through UART asynchronous serial communication. The main objective of this project is to design and development of FPGA based GPS data acquisition and processing system. FPGA is a better option to acquire the receiver data and it is to be processed further. FPGA will be interfaced to the GPS receiver module and the decoded received message like GPS latitude, longitude, altitude and velocity, with the proper Baud Rate. The internal signals are analyzed by using chipScope pro tool. By using Geo-fencing concept we will generate Alarm and send information when the vehicle/objective exceeds the boundary. The FPGA data acquisition modules will be developed in hardware description language (VHDL) using Xilinx ISE Design suite and implemented and verified in Xilinx Development Board.

Keyword: *GPS Receiver; data acquisition and processing system; FPGA (SPARTAN-3)*

Introduction

GPS (the full description is: NAVigation System with Timing And Ranging Global Positioning System, NAVSTARGPS) was developed by the U.S Department Of Defense (DoD). The GPS works on three segments. They are space segment, control segment and user segment. The space segment consists of currently 28 operational satellites orbiting the earth at a height of 20,180km on 6 different orbital planes. Their orbits are inclined at 55° to the equator, ensuring that a least 4 satellites are in radio communication with any point on the planet. Each satellite orbits the earth in approximately 12 hours and has four atomic clocks on board. The control segment having Master control station, four dedicated ground antennas and six dedicated monitor stations. The user segment consists of hundreds of thousands of users. GPS is a high-precision three-dimensional real-time global satellite navigation system, is a more advanced navigation and positioning system. According to the received navigational satellite signal, GPS receiver can calculate the body's position and velocity, and it is small and light; positioning accuracy and velocity accuracy are high, not accumulating with time; regardless of time, geographical constraints, and work around the clock , with good long-term stability. GPS play an important role in the human life .On land, it can be used for a variety of vehicles, tanks, ground force position; at sea, it can be used for the positioning of various ships; additionally ,GPS is also widely used in geodesy, field search and exploration and so on. GPS receiver outputs world time, three-dimensional positions, velocities, positioning satellites and other information, the information is large, while in actual use, only the position and velocity information was concerned. The distance between GPS receiver and satellite was three times of velocity of light. FPGA collected and extracted position and velocity information and then outputted them in real time through the serial port. The design module of FPGA based GPS data acquisition and processing system will be developed on VHDL using Xilinx ISE design suite. FPGA having the greater advantages like re-programmability, low cost, time to market and easy to implement any design. The PC transmitted movement information of the object in real-time by displaying. Additionally, the system can also be applied to integrated navigation system, which can effectively reduce the subsequent processing of the information, save a lot of resources.

Block Diagram

The block diagram of FPGA based GPS data acquisition and processing system is given bellow. Which consist of GPS Receiver+ FPGA kit + Alarm generation. The interfacing unit is used as RS-232.

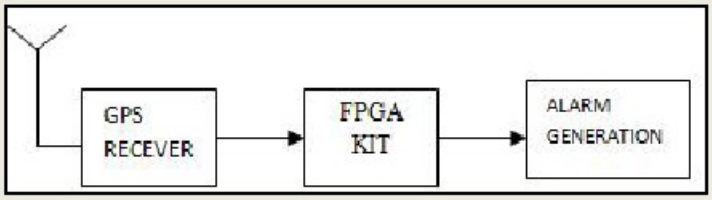

Figure 1: Block diagram of FPGA based GPS data acquisition and processing system

As show in figure 1 which having the major components of FPGA based GPS data acquisition and processing system. The 9-Pin package is used as interfacing unit. UART plays major role in serial communication. Asynchronous serial communication protocol regulates the same bits for each data to serial transmission, each serial data was constituted by the start bit, data bits, parity bits, and the specific format is shown in Figure 2:

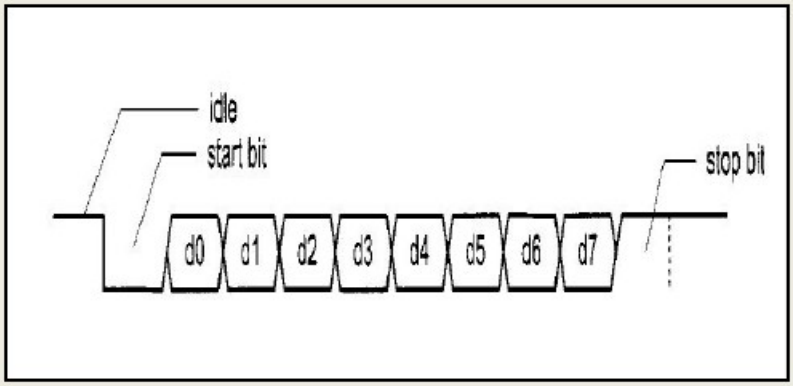

Figure 2: Asynchronous serial communication data format

GPS Data Format

GPS receiver positioning information was sent through the UART asynchronous serial communication port stand for antenna's latitude, longitude and altitude; in VTG **statement, 7 that the velocity field. Included in GPGGA data are GPS data information like date, time, longitude, dimension and speed etc. There are seven frames of data is available, which is given below.**

- $GPGGA,101229.487,3723.2475,N,12158.3416,W,1,07,1.0,9.0,M,,,0000*3E
- $GPGLL,2446.8619,N,12100.2579,E,060725.000, A,A*7E
- $GPGSA,A,3,05,02,26,27,09,04,15,,,,,1.8,1.0,1.5*1
- $GPGSV,3,1,,161229.487,A,3723.2475,N,12158.3416,W,0.13,309.62,120598,, *10
- $GPRMC,161229.487,A,3723.2475,N,12158.3416,W,0.13, 309.62,120598, ,*10
- $GPVTG,,T,,M,0.00,N,0.0,K,A*13
- $GPZDA,060526.000,20,06,2006,,*51

Implementation

The serial communication is implemented by using RS-232 interface. There are several types of serial communication devices are available such as RS-232, USB, Bluetooth and Ethernet, etc. The RS-232 interface is the Electronic Industries Association (EIA) standard for the interchange of serial binary data between two devices. i.e. it connects DCE and DTE. The pin packages are available in the form of 9-pin and 25-pin. Three wires are sufficient for communication. They are transmitting data, receiving data and signal ground. The RS-232 standard specifies that logic"1" is to be sent as a voltage in the range -15v to+15v and that logic"0" is to sent as a voltage in the range +5v to +15v. The serial communication is established in between GPS receiver and FPGA kit. In serial communication UART (Universal Asynchronous Receiver and Transmitter) plays major role. UART is a circuit that sends parallel data through serial line. The data transmission is in the form of 1-start bit, 8-data bits and 1-stop bit. Each bit is sampled by 16 times. So, that 16*baud rate. Therefore, clock divisions= frequency /16(baud rate). These calculations are shown above. The data transmission depends on the baud rate like 4800,9600,19600.... etc. The start bit is always low and the stop bit is always high.

A Geo-fence is a virtual boundary on a geographic area. When that boundary is entered or exited it can be recognized as an event and the user can be notified of that event. By using Geo-fence concept we will generate an alarm based on the range of the vehicle. In which we will kept one reference point, so based on reference point we will calculate distance. If the objective exceeds that particular boundary or within that boundary, then we will made an automatic alarm generation. The notification will tell the user which

vehicle/person has entered/left the area. This event information will be sent via a SMS to the instructor's mobile telephone. The diagrammatic **example is shown bellow figure3.**

Figure 3: The Geo-Fencing area

The implementation of the FPGA based GPS data acquisition and processing system having several blocks as shown figure4. This is also known as internal design of FPGA. The VHDL programming of RS-232 will be developed on different blocks. They are baud rate generator, UART Receiver, UART Transmitter, GPS data processing and alarm generation unit etc. By extracting latitude and longitude values from GPS receiver, then we will easy to determine distance between two points. After successfully dump the program into FPGA kit through IMPACT (JTAG chain). Now, interface the GPS receiver, Pc and FPGA kit through RS-232 cable. The internal signals of FPGA monitored by using chip scope pro analyzer. Here, whatever we are observing GPS data in hyper terminal, that respective hex values are observed in chip scope pro analyzer. These simulation results are shown in bellow.

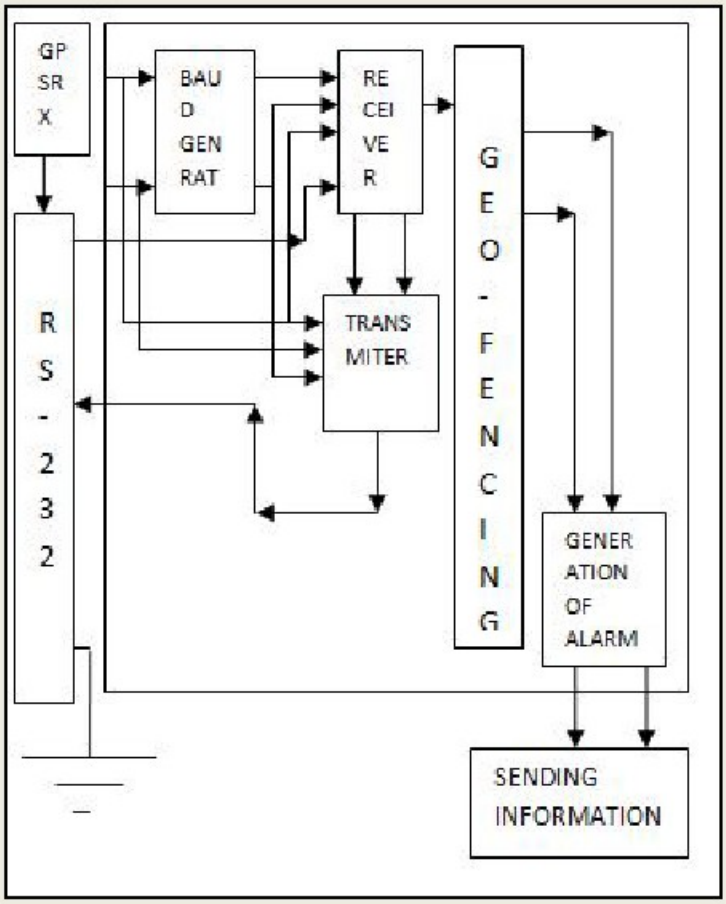

Figure 4: The internal design in FPGA

Simulation Results

The GPS receiver's data observed in HyperTerminal is shown in below figure5. **This contains standard seven frames of GPS data format. The respective chip scope result for GPS data is shown in figure6.**

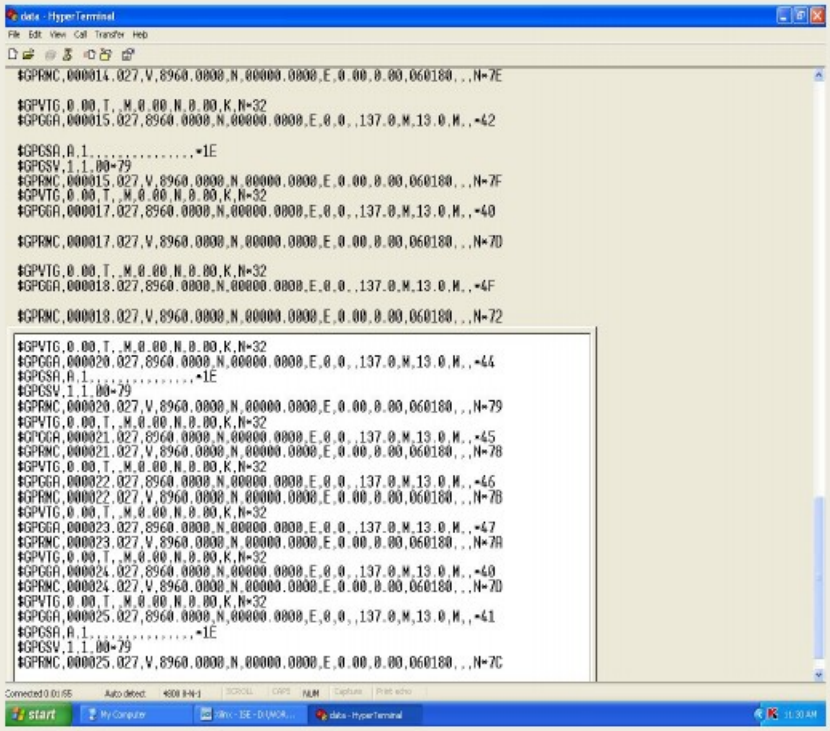

Figure5: GPS data format observed in hyper terminal

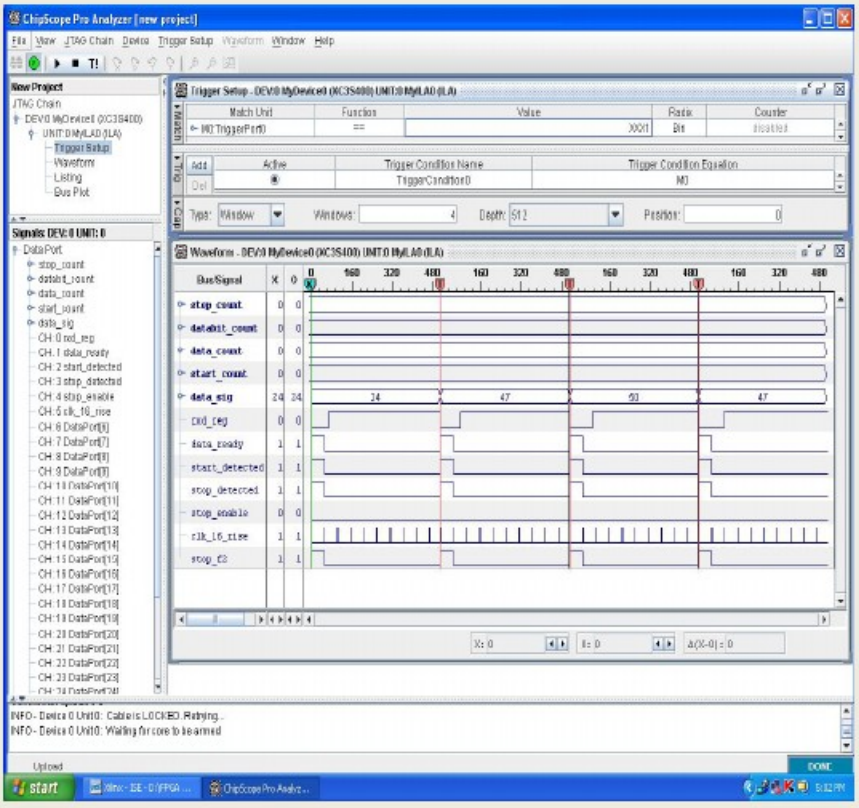

Figure 6: Chip Scope pro results for GPS data

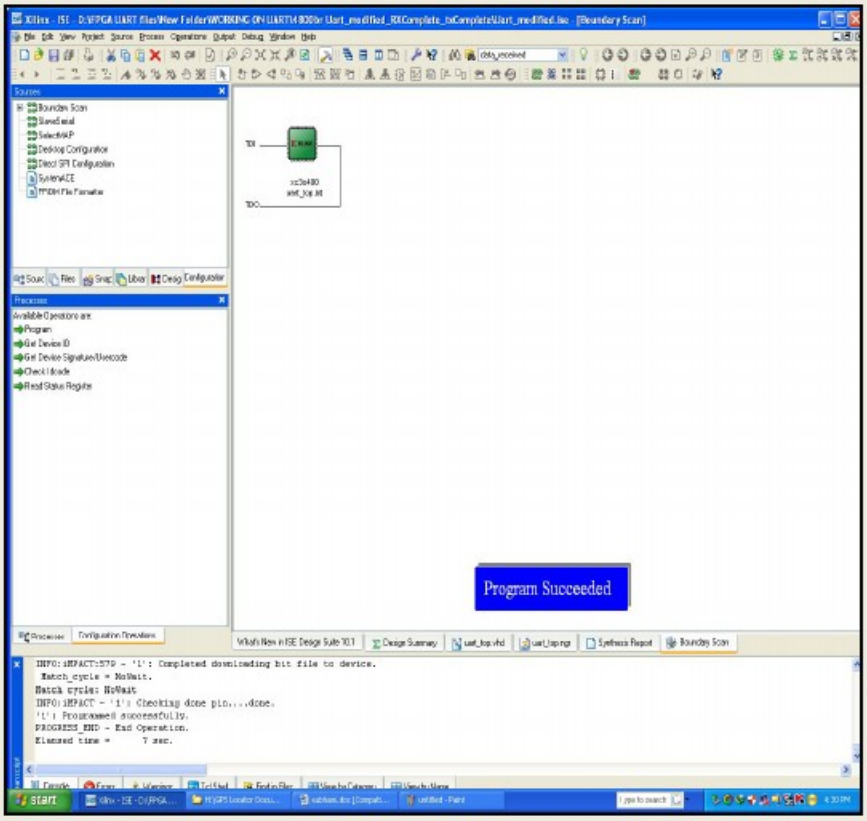

Figure 7: Configure the FPGA by using JTAG chain

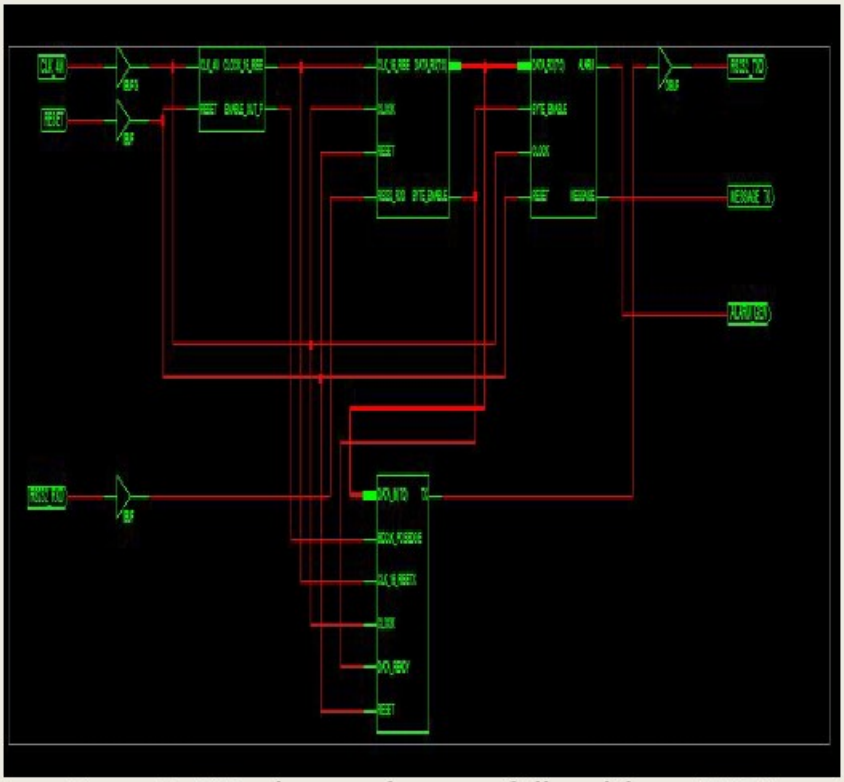

Figure 8: RTL schematic diagram of all modules in VHDL

Conclusion

This paper introduces a GPS positioning system design based on FPGA. As Compared with the Traditional orientation navigation system, the advantages are: using the FPGA which leads to high integration, low power consumption, low cost, short development cycle, convenient to upgrade the product, long life cycle, high precision, small volume, very easy personal carry. It has a good future in the fields such as car navigation, transportation, field work, public security, electric power, and the metallurgy industry. This design gives the object data (like latitude, longitude, N/S, Velocity, date and time) on the Earth. This design can effectively extract the position and speed information from all the GPS data, reducing the subsequent processor operations, improving the speed of the processor. By using Geo-Fencing concept, we will generate an alarm, and send the information to user. Which will helpful in navigation etc. Therefore, FPGA is better option for data acquisition system.

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