



## **Implementation Of Ultra Low Power High Speed 4-2 Compressor Using Single Phase Adiabatic Dynamic Logic**

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**Abstract:** *The paper presents the implementation of ultra low power 4-2 Compressor circuit operated by single-phase adiabatic Dynamic logic (SPADL) which, unlike any other existing Adiabatic logic family uses single sinusoidal supply-clock. This not only ensures high energy efficiency, but also simplifies the clock design which would be otherwise more complicated due to the signal synchronization requirement. Static logic resembled characteristics of SPADL logic substantially decreases circuit complexity with improved driving ability and circuit robustness. In TSMC 0.18 $\mu$ m CMOS technology. CADENCE simulations show that SPADL saves 65% to 50% and 30% to 40% of total energy compared to Conventional CMOS and other existing single phase adiabatic logic based 4-2 Compressor for a frequency of 1MHz to 100MHz.*

**Keywords:** *Single-phase, Adiabatic Logic, Energy efficiency, High speed, 4-2 Compressor*

## Introduction

As the semiconductor process has stepped into the deep submicron phase, the transistor counts integrated in a single chip are increasing continuously. Significant reduction of on chip power density, therefore, has received considerable favour. The dynamic switching is accounted the ring leader of the total power dissipation. As a response, over the past decade, though many techniques have been developed to reduce such an unwanted power overhead, yet adiabatic logic becomes the promising alternative. Adiabatic circuits achieve low energy dissipation by restricting the current flow across devices with low voltage drop and by recycling the energy stored on their load capacitance by using a time varying AC supply voltage. Recent years have seen various Energy Recovery Circuits (ERCs) toward adiabatic circuitry for ultra-low power implementation. Most of them require a four-phase or two phase power-clock. Typical examples are four-phase CPAL [1] and two-phase 2N2N2P2D [2], CEPAL [3], GFCAL [4]. In multiphase clocking scheme, implementation of complex control schemes [5]-[7] distribution of multiple clock phases[3]-[7], the management of data dependent clock capacitance fluctuations make the multiphase clocking schemes sensitive to clock skew and may severely limit their high frequency performance [8]-[9]. In contrast to multiphase circuits, single phase adiabatic circuit relies on just one phase of a power clock waveform for low power and synchronization. Simply a sinusoidal signal can be used as a power clock in a single phase adiabatic circuit. This sinusoidal waveform can be generated with higher energy efficiency than trapezoidal waveforms. In order to make adiabatic logic circuits more feasible and practical in VLSI CMOS applications, single phase operation of the circuits would be needed.

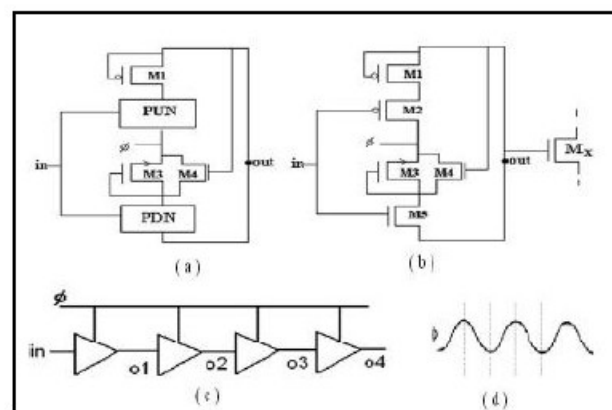


Figure 1: (a) SPADL general block (b) SPADL Inverter  
(c) SPADL inverter chain (d) Single phase supply clock

Previously reported SCALD [11] and SCAL [12] circuits use a single-phase power-clock, but the additional reference voltage and current increase the design complexity. Moreover these logic styles are difficult to design due to the optimal value of reference voltage concerning about clock frequency [11], [12]. An inverter chain using CAL logic is discussed in [13] with additional timing control clocks to ensure correct operation, resulting in complicated clock tree design and more energy dissipation. Moreover as CAL logic is based on differential signalling, its higher switching activity reduces energy efficiency. Another typical single-phase ERC family is PAL [16], which is not considered as a real single-phase based ERC since its cascaded circuits need two complementary sinusoidal power clocks. Also PAL [16] logic gates suffer from undesired capacitive couplings, since the output nodes are kept floating instead of zero. Though QAPG [14] has reported as single phase adiabatic logic, yet transistor overheads decrease the energy efficiency. Motivated by the advantages of single phase adiabatic logic the authors have proposed a quasi-static single phase adiabatic dynamic logic (SPADL) [10] recently and also implemented the sequential subsystem. In this paper an 8 bit CLA has implemented by using SPADL logic all the simulations are done by Cadence Spice spectra in TSMC 0.18 $\mu$ m technology and CMOS n-well process and results are compared with some imperative adiabatic logic styles (CAL, QAPG and 2N2N2P2D) including static CMOS also.

### Overview Of Spadl Logic

SPADL requires only one sinusoidal power clock supply, Has simple implementation, and performs better than the Previously proposed diode based logic families [2]-[4] in terms of energy consumption. SPADL logic features Simplicity and static logic resembled characteristics, which Substantially decreases transistor overheads and the circuit Complexity.

#### *Configuration and Operation*

Fig. 1(a) and (b) shows the general configuration of SPADL logic block and SPADL inverter. In Fig. 1, on basis of applied logic inputs, either pull up or pull down network (PUN or PDN) will be ON at any time instant. The charging and discharging operations of output (out) node of Fig. 1(a) can be described as follows:

a) When PUN is ON and 'out' is low, if supply clock ( $\phi$ ) ramps up 'out' node will be charged through PUN $\rightarrow$ M1 by following  $\phi$  closely and higher logic will be obtained at

out node. When  $\phi$  ramps down, charges will be stored at 'out' node, as **they cannot flow** back to the supply clock ( $\phi$ ) due to reverse biased M1.

b) When PDN is ON and 'out' is high, if  $\phi$  ramps down, Charge stored at 'out' node flows back to the supply clock ( $\phi$ ) through the PDN  $\rightarrow$  M3 and M4.

c) When PUN is ON and 'out' is high, if  $\phi$  ramps up 'out' node will not transit for that clock period. So voltage level of 'out' node will not vary.

d) When PDN is ON and 'out' is low, 'out' node voltage will not transit for that **complete clock cycle. Hence**

$$V(1) = (\phi)_{\max} - |V_{TP}|$$

$$V(0) = \Delta V \quad (1)$$

Where  $\Delta V$  is proportional to  $f(R_d)$ .  $R_d$  is the discharging path resistance. As discharging path consists of parallel combination of M3 and M4,  $R_d$  will be very low, which improves the lower swing.

Also due to finite voltage drop across M5, gate to source voltage swing of M4 increases.

ON resistance ( $R_d$ ) of a NMOS can be expressed as

$$R_d \propto (V_{GS} - V_T)^{-1} \quad (2)$$

So increased gate to source swing reduces the ON

Resistance of M4. The output wave forms are shown in Fig. 2.

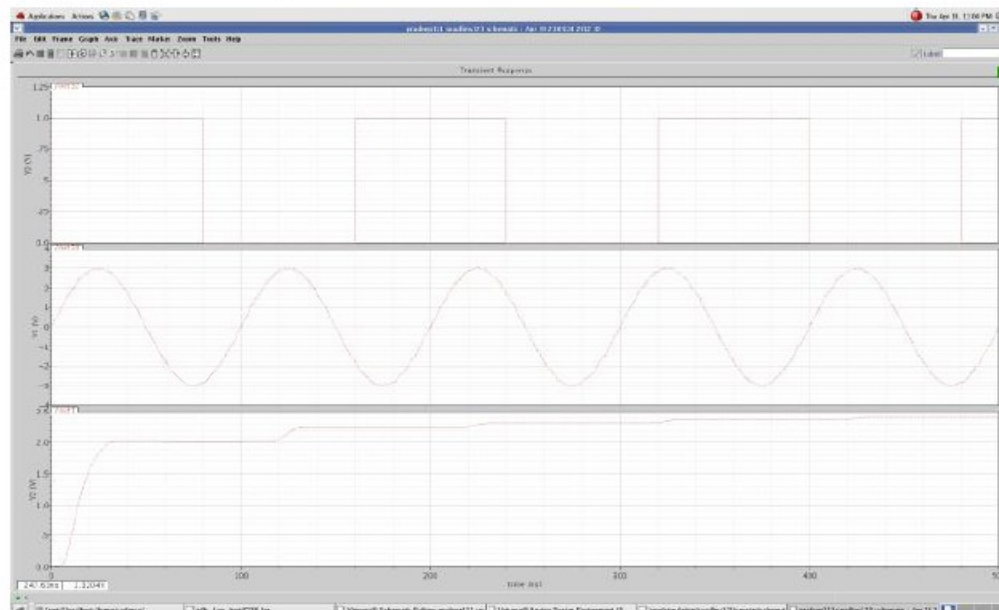


Figure: 2 Output waveform of SPADL inverter

Fig. 3 illustrates the operation of the SPADL inverter circuit. Assuming the applied inputs of the circuit are all valid at  $t=0$  time instant. The 1st stage produces its valid-1 and valid-0 outputs at  $t=T/2$  time and  $t=T$ , respectively. The 2nd stage produces its valid-0 output at  $t=T$ . Similarly, valid-1 outputs of the 2nd and 3rd stages are both produced at  $t=3T/2$ , while the valid-0 outputs of the 3rd and 4th stages are both produced at  $t=2T$ , and so on. Thus, the total time,  $T_{total}$ , needed for data to pass through the 4-stage circuit is  $5T/2$ , where  $T$  is the period of  $\Phi$ . In general, for an  $N$ -stage circuit, we have  $T_{total} = (N+1)T/2$ . When  $N \gg 1$ ,  $T_{total} = NT/2$ , which ensures higher speed of SPADL logic. Also in SPADL by using low clock frequency we can drive high frequency input signal.

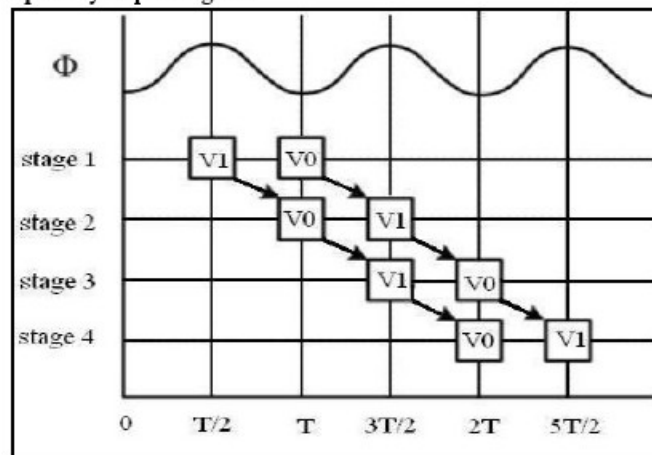


Figure: 3 Operation of SPADL inverter, V1 and V0 are valid '1' and valid '0' output

#### Energy Consumption of SPADL Logic Circuit

In this section, energy consumption of SPADL logic block, say inverter, are analysed. From Fig 1, on the basis of input logic level when the supply clock ( $\phi$ ) ramps up (or down) energy dissipation occurs across PMOS diodes (or NMOS diodes) and PUN (or PDN). As PMOS diodes with PUN (or NMOS diodes with PDN n/w) provide the charging (or discharging) path, energy dissipation across diodes can be

Expressed as;

$$\begin{aligned}
 E_{\text{Diode}} &= \int_0^{T_1} |V_{TP}| i(t) dt \\
 &= \int_0^{C_L(V_{DD} - V_{TP})} |V_{TP}| dq \\
 &= [C_L |V_{TP}| (V_{DD} - |V_{TP}|)] \quad (3)
 \end{aligned}$$

Where  $T_1$  is the time taken by the supply clock to raise From 0 to  $V_{DD}$ ,  $|V_{TP}|$  is threshold voltage of PMOS diodes,  $C_L (= C_{D1} + C_W + C_{GX})$  is the output load capacitance.  $C_{GX} (= \beta L C_{OX})$  is the gate capacitance of next stage NMOS  $M_X$ .  $\beta$  and  $L$  are aspect ratio and length of the channel of  $M_X$  and  $C_{OX}$  is the gate oxide capacitance per unit area.  $C_W$  is the wiring capacitance.  $E_{Diode}$  is independent of operating frequency of supply clock. As clock frequency goes higher, the “diode transistors” have to be sized up proportionately. Moreover threshold voltage drop across PUN and finite ON resistance produce the energy dissipation ( $E_{Tx}$ ) in charging event and can be shown by the following expression

$$E_{Tx} = \left[ \frac{1}{2} C_L |V_{TP}|^2 + (R_{PCL}/T) C_L (V_{DD} - |V_{TP}|)^2 \right] \quad (4)$$

Therefore for each logic transition total energy dissipation ( $E_{Total}$ ) in charging path becomes:

$$E_{Total} = E_{Diode} + E_{Tx} \\ \approx [C_L |V_{TP}| (V_{DD} - |V_{TP}|)] + \left[ \frac{1}{2} C_L |V_{TP}|^2 \right] \quad (5)$$

$$(As RC/T \ll 1 \text{ for moderate fan-out}) \quad (8)$$

During discharging almost same amount of energy dissipates in the discharging path. So the maximum possible energy saving of SPADL logic over CMOS in a full clock cycle is

$$\eta\% = \left\{ \frac{[C_L |V_{TP}| (V_{DD} - |V_{TP}|)] + \left[ \frac{1}{2} C_L |V_{TP}|^2 \right]}{C_L V_{DD}^2} \right\} \times 100 \\ \approx 2\alpha [1 - \alpha^2/2] \times 100 \text{ where } \alpha = \{|V_{TP}|/V_{DD}\} \quad (6)$$

It is seen that there is no significant improvement in energy efficiencies of SPADL logic by lowering threshold voltage of PMOS and NMOS diode. However to achieve higher integration density or to maintain high drive current, voltage scaling is important. Still we cannot reduce threshold or supply voltage arbitrarily. As aggressive scaling of technology results in different leakage components become a significant issue of total power dissipation in adiabatic CMOS logic circuit measures proportionately more than is customary. This measurement and others are deliberate, using specifications that anticipate your paper as one part of the entire proceedings, and not as an independent document. Please do not revise any of the current designations.

#### 4-2 Compressor By Spadl Logic

In this section, we first describe SPADL gates, and then we Present the design of adiabatic gates and 4-2 compressor using SPADL logic

##### *SPADL Complex gate Design*

Complex gates can be easily implemented by using simple CMOS pull-up and pull-down network. In Fig. 1(a), by replacing the PUN (pull up network) or PDN (pull down network) we can implement the AND gate, XOR gate, 2 to 1 MUX with SPADL circuit topology. Fig. 4 shows implementation of all these gates with simple buffer circuit also. Static logic resembled characteristics of SPADL logic Substantially decreases the transistor overheads in complex gate design. In buffer circuit we have modified our logic slightly shown in Fig. 4 (d). When  $\Phi$  ramps up and 'in'=1 (or 0), NMOS (or PMOS) (having gate i/p 'in') is turned ON and 'out' node is charged (or discharged). So we get same logic as 'in' at out node and hence the circuit acts as buffer. Thus Complex gate design can be made very modular and simple. The layouts of SPADL AND, OR, XOR and NOT gates are shown in Fig. 5. These layouts are created by using CADENCE suite based on TSMC 0.18 $\mu$ m CMOS n-well process technology. A design rule checking (DRC) and the circuit structure *extraction* are performed on the layout view of the adiabatic system. Then, the *view extracted* from the layout and the original schematic view is compared with the *layout versus schematic* (LVS) tool Layout of SPADL gates are shown in Fig. 5

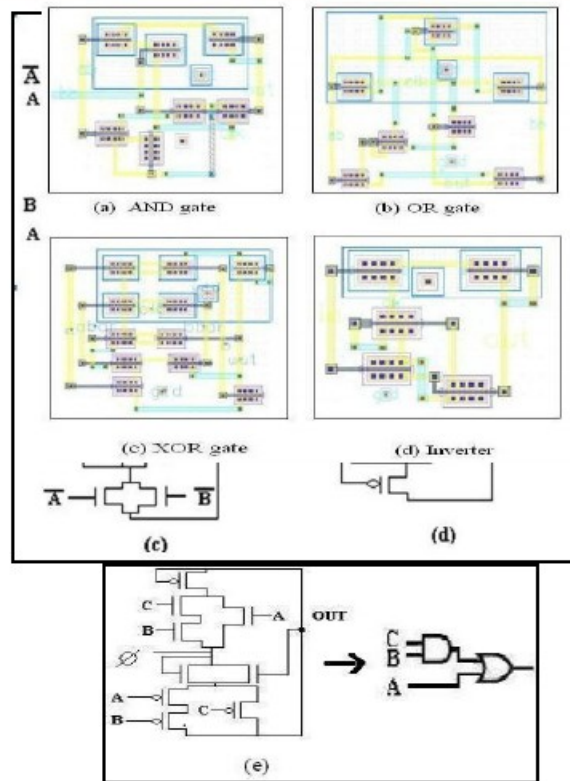


Figure: 4 SPADL gates (a) XOR (b) 2 to 1 MUX (c) AND (d) buffer (e) AND\_OR having o/p  $(A+BC)$

*SPADL 4-2 Compressor implementation*

The 4-2 compressor has 4 inputs X1, X2, X3 and X4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Fig 6. The input Cin is the output from the previous lower significant compressor. The Cout is the output to the compressor in the next significant stage. We can make XOR-XNOR simply connecting the inverter to the XOR gate output, also MUX\* can make connecting inverter to the MUX gate output.

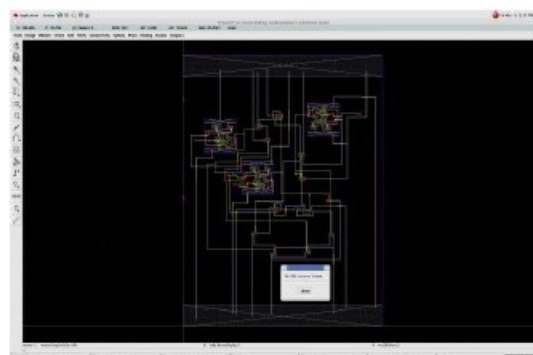


Figure: 5 Layout of SPADL gates (a) AND (b) OR (c) XOR (d) Inverter (e) Mux



We can be observed that the overall delay is decreased .the fact that both the output and its complement are available at every stage, is neglected thus replacing some XOR blocks with multiplexer's results in a significant improvement in delay. Also the MUX block at the SUM output gets the select bit before the inputs arrive and thus the transistors are already switched by the time they arrive. This minimizes the delay to a considerable extent. This is shown in Fig.6 A significant speed improvement in the implementation of 4-2 Compressor.

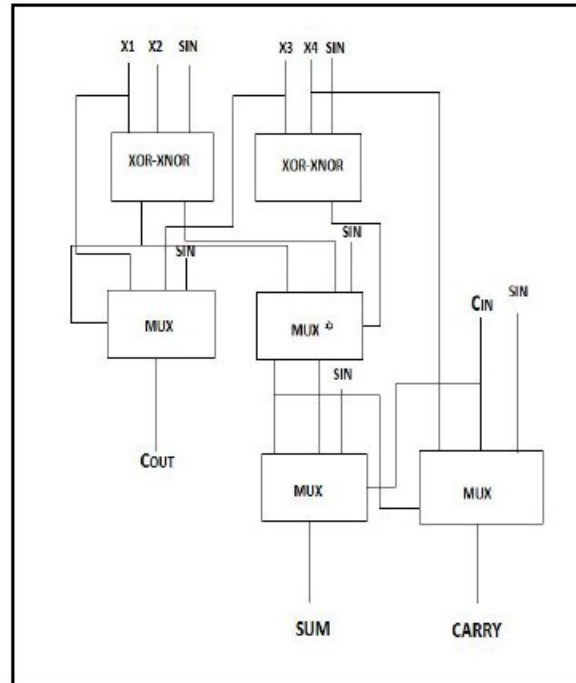


Figure: 6 Proposed 4-2 Compressor Architecture

The equations governing the outputs in the proposed architecture are shown below

$$\text{Sum} = (x1 \oplus x2) \bullet \overline{x3 \oplus x4} + (x1 \oplus x2) \bullet (x3 \oplus x4) \bullet \overline{\text{Cin}} + \overline{(x1 \oplus x2) \bullet x3 \oplus x4} + (x1 \oplus x2) \bullet (x3 \oplus x4) \bullet \text{Cin}$$

$$\text{Cout} = (x1 \oplus x2) \bullet x3 + \overline{(x1 \oplus x2) \bullet x1}$$

$$\text{Carry} = (x1 \oplus x2 \oplus x3 \oplus x4) \bullet \text{Cin} + \overline{(x1 \oplus x2 \oplus x3 \oplus x4) \bullet x4}$$

The critical path delay of the proposed implementation is -XOR + 2\*-MUX. We have designed and simulated a 4-2 compressor using SPADL the simulations are done by

CADENCE spice spectra, using TSMC 0.18 $\mu$ m CMOS technology. A 5V peak-to-peak sinusoidal voltage supply was used as the power clock F throughout our simulation for SPADL logic. The other adiabatic compressor blocks are simulated under different clocks provided by the literatures all the output nodes are loaded by 25 fF or 5pF capacitors to get more stable waveform. The simulated waveforms are shown in Fig. 7. In order to fairly compare the energy efficiency of SPADL, CAL, QAPG, 2N2N2P2D and static CMOS, we have optimized the transistor sizes for each circuit style with the purpose of making them consume the least energy. Fig 8 show that the layout of the SPADL 4-2 compressor.

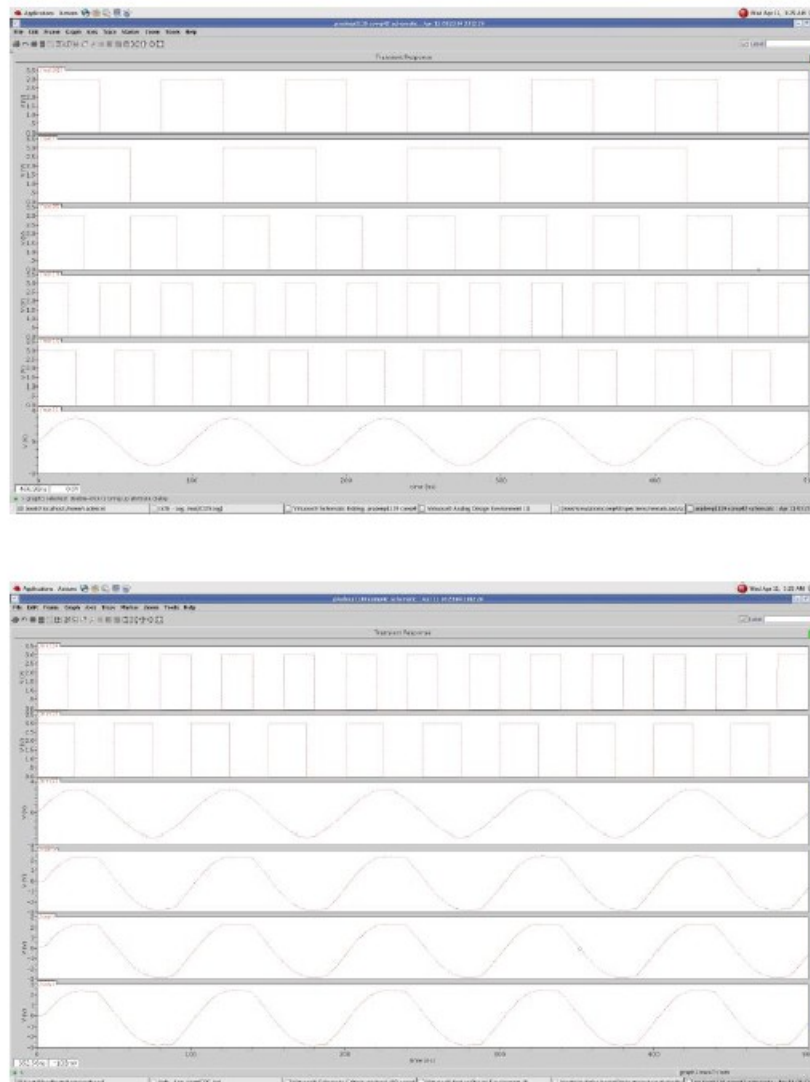
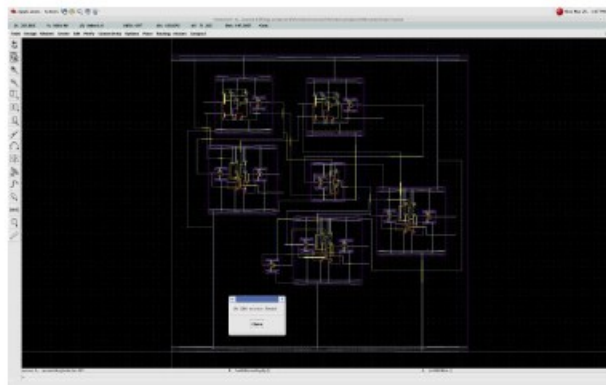


Figure: 7 Output waveforms of 4-2 adiabatic Compressor

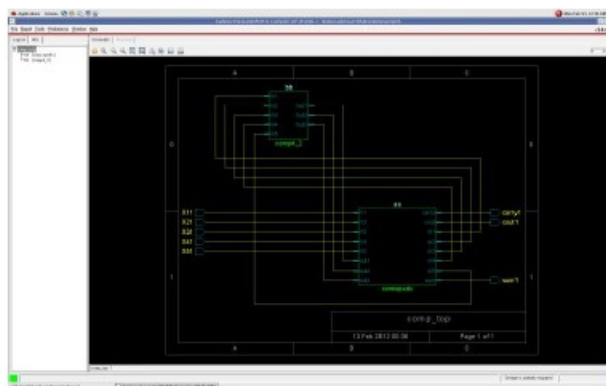
### Simulation Results And Discussion

The results of the RTL compilation are shown below:

The results coming from the CADENCE simulation of the SPADL arithmetic units described above are presented and Discussed in this section and different aspects of SPADL logic has been explored due to the simulation. In this section energy dissipation measurements were determined directly from the CADENCE simulations outputs, by integrating the power over the period of oscillation. For the adiabatic circuits we have initially assumed a 100% energy- efficient power- clock generator, in order to compare the Results with the literature.



*Figure: 8 Layout of SPADL 4-2 compressor*



*Figure: 9 IO PAD of SPADL 4-2 compressor*

We take it into our account then SPADL shows better efficiency as it uses energy efficient sinusoidal source, compared to other multiphase clocked logic at low frequency, all single phase logic styles (CAL QAPG and SPADL) promise substantial energy savings compared to static CMOS, with the lowest energy consumption from SPADL. SPADL based compressor consumes only 34% and 52% of total energy consumed by conventional 4-2 compressor at 10MHz and 100 MHz frequencies respectively as diodes using MOS transistors are weak in driving capability, hence in SPADL based compressor, latches are introduced at the end of 3 stages to improve the driving ability. That causes some extra power dissipation. Still at 100 MHz frequency, SPADL logic based compressor consumes only 62% and 69% energy of the CAL and QAPG Based 4-2 compressor respectively. In general energy consumption of SPADL logic does not depend on the

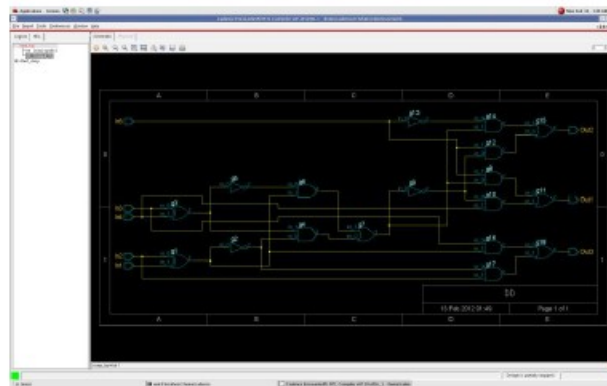


Figure: 10 RTL schematic of SPADL 4-2 compressor

Operating frequency so much at low frequencies as it is mainly due to the diodes and conventional clocks. As clock frequency goes higher, the “diode transistors” have to be sized up proportionately, which increases the capacitances. The resistive dissipation (which is proportional to  $RC/T$ ) increases as well. On the other hand, 2N2N2P2D compressor does not show much power savings since 2N2N2P2D logic circuit has floating output node during part of the clock cycle. Simulation shows that this circuit can only work well if there is substantial capacitance to ground. Otherwise, capacitive coupling between the floating output node and clock would cause inadequate operating margins, which is undesirable as the output is directly connected to the input of the next stage logic in 2N2N2P2D. In QAPG compressor transistor overheads increase the power dissipation in path hence decrease the efficiency at high frequency regime. Though CAL

and QAPG logic based compressor promise substantial energy saving at low frequency yet in high frequency regime both circuit consume much more power compared to proposed SPADL compressor circuit. SPADL based compressor save almost 30% to 40% of total energy compared to CAL and QAPG at 100MHz frequency.

### **Conclusion**

This paper presents the SPADL 4-2 COMPRESSOR circuits using single phase ac power supply. This SPADL logic style can enjoy minimal control overheads and are thus capable of Operating at high speeds, while achieving high-energy efficiency. Compared to other existing single phase based Logic SPADL COMPRESSOR saves 30% to 40% of total energy for clock frequencies ranging from 1MHz to 100 MHz frequency. High energy efficiency of SPADL makes it suitable for implementing performance efficient VLSI circuitry.

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