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Comparative Study Of Different Pll Frquency Synthesizers

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Abstract:

Thanks to the advance of semiconductor and communication technology, the wireless communication market has been booming in the last two decades. It evolved from simple pagers to emerging third-generation (3G) cellular phones. In the meanwhile, broadband communication market has also gained a rapid growth. As the market always demands high performance and low-cost products, circuit designers are seeking high integration communication devices in cheap CMOS technology. The phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converters in the analog-and-digital signal interface.

Keywords: *PLL,*

1.Introduction

In the last decade, the rapid growth of wireless applications has led to an increasing demand of fully integrated, low-cost, low-power, and high performance transceivers. The applications of wireless communication devices include pagers, cordless phones, cellular phones, global positioning systems (GPS), and wireless local area networks (WLAN), transmitting either voice or data. A standard specifies how devices talk to each other. Numerous standards emerged and are optimized for certain applications. For voice, examples include AMPS, NMT, TACS, D-AMPS, DECT, GSM, DCS, PCS, PDC, TDMA, CDMA, etc. It has evolved from analog to digital, from the 1G (first generation) to the current existing 2.5G, such as GPRS and EDGE. Devices in the 3G wireless standards, which include UMTS (WCDMA), CDMA2000 and TD-SCDMA, are also emerging in some areas of the world. For data, there are 802.11a/b/g WLAN, Hiper LAN, Bluetooth, Home RF, and so on. More recently, a significant interest has grown in the ultra wideband communications.

There are still many difficulties, however, in the process of integration of RF front-end due to the lack of high-quality components on chip. This review paper focuses on the design of the frequency synthesizer, one of the key building blocks of the RF front-end in CMOS technology. The frequency synthesizer is used as a local oscillator for frequency translation and channel selection in the RF front-end of wireless transceivers. It is a critical component in terms of the performance and cost of a wireless transceiver.

2.Implementations Of Frequency Synthesizer

As shown in Table I, frequency synthesizers can be grouped into four classes: direct analog synthesizer (DAS), direct digital synthesizer (DDS), phase-locked loop frequency synthesizer (PLL-FS), and delay-locked loop frequency synthesizer (DLL-FS).

<table>
<tr><td rowspan="9">Frequency Synthesis</td><td rowspan="2">Direct Synthesis</td><td>DAS</td><td colspan="2">multiplier + mixer+ divider</td></tr>
<tr><td>DDS</td><td colspan="2">NCO+ DAC</td></tr>
<tr><td rowspan="7">Indirect Synthesis</td><td rowspan="6">PLL-based</td><td colspan="2">Integer-N</td></tr>
<tr><td rowspan="5">Fractional-N</td><td>Phase estimation by DAC</td></tr>
<tr><td>Random jittering</td></tr>
<tr><td>Noise shaping by $\sum\Delta$</td></tr>
<tr><td>Phase interpolation</td></tr>
<tr><td>Pulse generation</td></tr>
<tr><td>DLL-based</td><td colspan="2">Frequency multiplied by the number of equal spacing phases</td></tr>
</table>

Table 1: Classification of Frequency Synthesizers

2.1.Direct Synthesis

2.1.1.Direct Analog Frequency Synthesizer

The direct analog synthesizer is realized by cascading stages of frequency multipliers, dividers, mixers and band-pass filters (BPF). A large number of separate frequencies or channels can be generated from a single reference. The desired output signals can be rapidly switched between any set of frequencies. Many manufactures of commercial test equipment use mix-and-divide design for their synthesizers and they report that excellent phase noise and spurious performance can be achieved with adequate physical/electrical isolation between the stages. The major drawback of this scheme is the sheer size and power that would be required to make a synthesizer of this type for certain applications. Fig 1 shows an example of DAS. The output frequency is

$$f_{out} = f_1 + 0.1f_2 + 0.01f_3 \quad (1)$$

Since f_1,f_2 and f_3 can be 0 to 9 times of the input frequency, f_{in} and f_{out} can be varied from 0 to $1.99f_{in}$ with a resolution of $0.01f_{in}$.

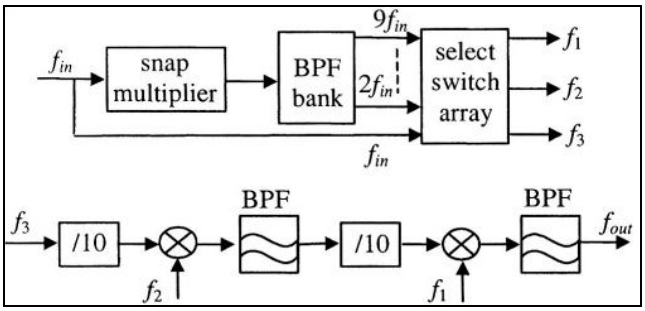

Figure 1: An Example Of DAS

3.Direct Digital Frequency Synthesizer

The direct digital synthesizer is a technology that has been around since the early 1970's. The two major components of the DDS are a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). The NCO consists of an adder-register pair (also known as phase accumulator) and a ramp-to-sine wave lookup ROM. Figure 2 shows the block diagram of a DDS. The output of the DDS is related to the phase accumulator input by the following equation:

$$f_{out} = \frac{K}{2^N} \cdot f_{clock} \qquad (2)$$

where *N* is the bit-length of the accumulator and K is the accumulator's input. The DDS typically provides a low frequency output with extremely high resolution and excellent frequency switching speed. The resolution of DDS can be made arbitrarily small with very little additional circuitry or added circuit complexity. Due to sampling theory a DDS can only generate frequencies up to a maximum of half of the clock rate of the digital circuitry. The primary disadvantage of most direct digital synthesizers is the typically high spurious content caused by quantization and linearity limitation of the DAC. A rough rule of thumb is that the spurious level generated by DAC quantization equals 6*dB* times the number of input bits (e.g. an 8-bit DAC would have quantization spurious 48*dB* lower than the carrier). However, as the DAC is clocked at frequencies approaching its upper limit, spurs caused by non-linearities in the DAC become dominant.

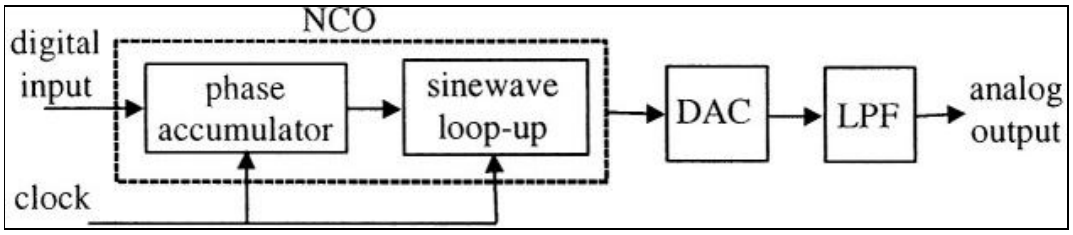

Figure 2: Block diagram of DDS

3.1.Indirect Frequency Synthesizers (PLL-Based Frequency Synthesizers)

3.1.1. Integer-N PLL-FS

Fig 3 depicts a PLL-based integer-N frequency synthesizer. It consists of a phase-frequency detector (PFD), a charge-pump (CP), a loop filter, a voltage-controlled oscillator (VCO), and a programmable frequency divider. For an integer-N frequency synthesizer, the output frequency is a multiple of the reference frequency:

$f_{out} = N. f_{ref}$ (3)

where N , the loop frequency divide ratio, is an integer. Whereby the frequency resolution of the integer-N frequency synthesizer is equal to the reference frequency. Due to the limitation of frequency resolution equal to the reference frequency, for narrow-band applications, the reference of the synthesizer is very small and the frequency divide ratio is very large. For example, for 900*MHz* GSM and 2.4*GHz* Bluetooth, the reference frequencies are 200 *kHz and 1 MHz*, respectively, and the corresponding divide ratios are around 4500 and 2400, respectively. The conventional integer-N PLL with low reference frequency has several disadvantages. First, the lock time is long due to its narrow loop-bandwidth. Second, the reference spur and its harmonics are located at low offset frequencies. Third, the large divide ratio (*N*) increases the in-band phase noise associated with the reference signal, the PFD, the charge-pump and the frequency divider by 20log*(N) dB*. Finally, with a small loop-bandwidth, the phase noise of the VCO will not be sufficiently suppressed at low offset frequencies.

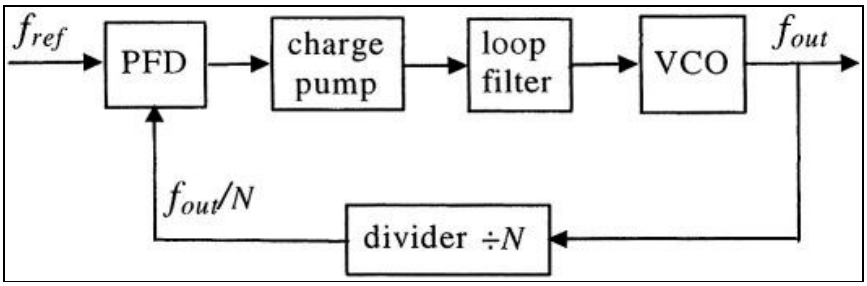

Figure 3: Integer-N PLL-FS

4.Fractional-N PLL-FS

Fractional-N frequency synthesizers (FN-FS) are used to overcome the above-mentioned disadvantages of integer-N synthesizers. In the fractional- N synthesizer, the frequency divide ratio can be a fractional number, so a large reference can be used to achieve a small frequency resolution. However, the principle disadvantage of the fractional-N frequency synthesis is the unwanted low-frequency spurs due to the fixed pattern of the dual modulus (or multi-modulus) divider. Since these spurs can reside inside the loop bandwidth, fractional-N synthesizers are not practical unless fixed in band spurs are suppressed to a negligible level. Five main spur reduction techniques are addressed in the literature. Their prominent features and problems are summarized in Table 2 .

Technique	**Feature**	**Problem**
DAC phase estimation	Cancel spur by DAC	Analog mismatch
Random jittering	Randomize divide ratio	Quantization noise
∑Δ noise shaping	Modulate divide ratio	Quantization noise
Phase interpolation	Inherent fractional divider or multiphase VCO	Interpolation jitter
Pulse generation	Insert pulses	Interpolation jitter

Table 2: Spur Reduction Techniques for Fractional- N Synthesis

The block diagram of a fractional-N synthesizer using DAC phase estimation is illustrated in Fig. 4. An accumulator is used to control the instantaneous divide ratio. If the overflow *(OVFL)* is 1, the divide ratio is N_B+1.otherwise the divide ratio is N_B .Since the average of the overflow is k / M , where k is the input to the accumulator and M is the modulus of the accumulator. Thus, the fractional divide ratio is $N= N_B + k / M$ and the frequency resolution is f_{ref}/M .Since the instantaneous divide ratio varies periodically, strong fractional spurs would appear at the synthesizer output. The DAC is used to convert the instantaneous phase error, which is proportional to the residue of the accumulator, into an equivalent amount of charge-pump current to compensate the phase error. The accuracy of this compensation is limited by the DAC and is sensitive to process variations.

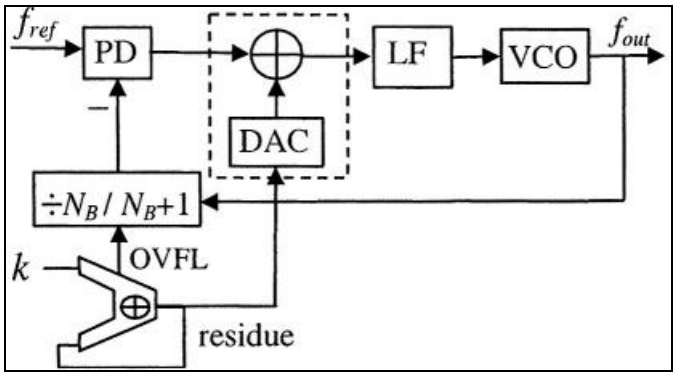

Figure 4: FN-FS using DAC phase interpolation

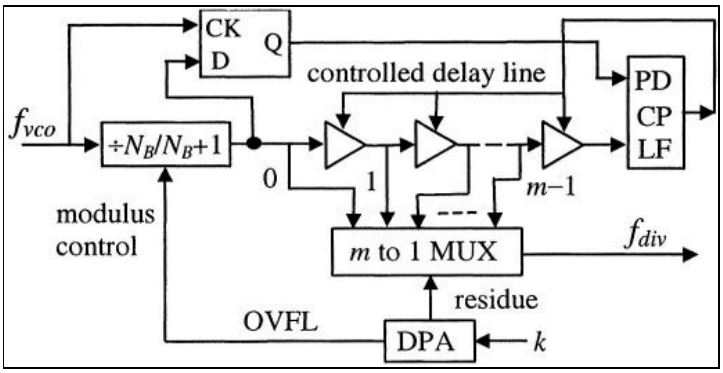

Figure 5: An inherent fractional divider for FN-FS

Fig 5 shows an inherent fractional divider for fractional-N synthesizer using phase interpolation. An *m*-stage delay-line is used to produce a total delay of one input VCO signal cycle; The modulus of the digital phase accumulator (DPA) is also *m.* Therefore,

the frequency resolution of a fractional-N synthesizer using this fractional divider is f_{ref}/m. Although fractional spurs generated from the mismatches of the delay stages are usually negligible, the number *m* cannot be made large as f_{vco} goes high. When f_{vco} is very high, a single stage delay would be more than $1/ f_{vco}$ .Thus, the corresponding fractional divider does not exist at all. Phase interpolation can also be based on a multiphase VCO. Since the phase mismatch of the multi-phase VCO is often a concern, phase calibration is needed to reduce the fractional spurs caused by phase mismatch.

The phase noise shaping by modulation is similar to the random jittering method which just randomizes the jitter of the divider output. However, it does not have a phase noise spectrum due to the noise shaping property of the modulator. As shown in Fig. 6, fractional division based on an accumulator is similar in concept to the modulator for dc inputs. Since the order or higher-order modulator does not generate fixed tones for dc inputs, they can more effectively shape the phase noise spectrum than the first-order modulator. The effective over-sampling ratio (OSR) can be defined by the ratio of the reference frequency to the PLL bandwidth. When high-order modulators are used, the PLL needs more poles in the loop filter to suppress the quantization noise at high frequencies.

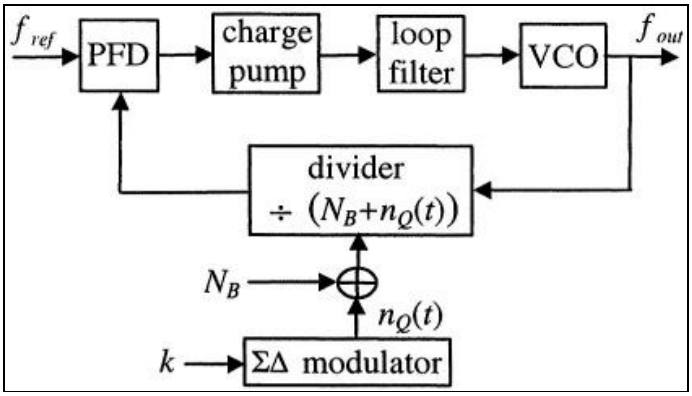

Figure 6: Fractional-N Frequency Synthesizer

5.Multi-loop PLL-FS

To avoid the large division ratio in an integer-N PLL synthesizer, one alternative is to use multiple loops to reduce the division ratio. Dual-loop PLL is frequently used to improve the tradeoff among phase noise, channel spacing, reference frequency and the locking speed. Some dual-loop PLL frequency synthesizer architectures are shown in Fig. 7. In Fig. 7 (a), PLL1 is used to generate reference frequencies for PLL2. In Fig. 7

(b) PLL1 output is up-converted by PLL2 and a single-sideband (SSB) mixer. PLL1 generates tunable IF frequencies, while PLL2 generates a fixed RF frequency. In Fig. 7 (c) and (d), PLL2 and a SSB down-conversion mixer are used to reduce the divide ratio in PLL1. Recent works used the dual-loop PLL topology shown in Fig. 7 (e) for GSM receivers.

The drawback of the dual-loop PLL is that it may require two references, and/or at least one SSB mixer, which might introduce additional phase noise. Moreover, when one PLL is used as a reference for the other, the reference noise is much higher than that of crystal oscillators.

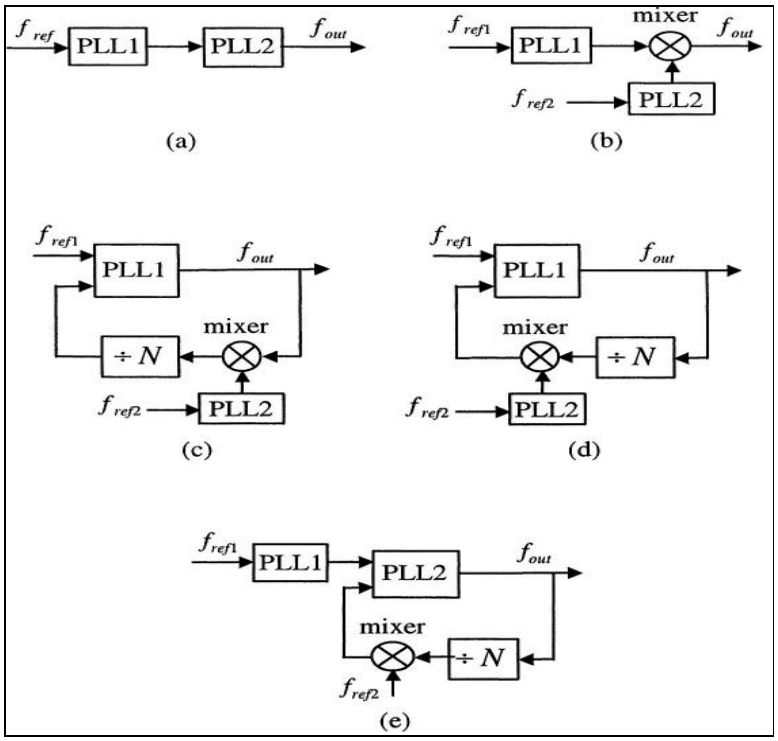

Figure 7: Dual-loop PLL frequency synthesizers

6. DLL-Based Frequency Synthesizer

More recently, designers use DLL as a frequency multiplier or for multiphase generation. Unlike PLL, there is no phase accumulation in DLL and extremely low phase noise can be achieved. The big drawback of the DLL frequency synthesizer is that it is not programmable. Other problems, such as limited multiplication factor and high power consumption also limit its application. With self-calibration, DLL-based synthesizers can achieve extremely low phase noise. The block diagram of a DLL-FS is shown in Fig. 8.

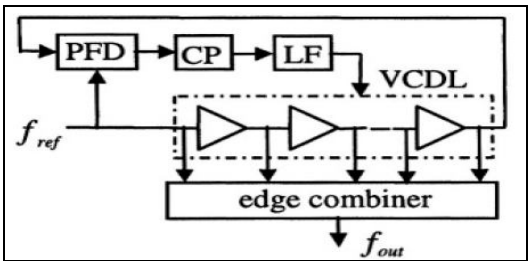

Figure 8: Block diagram of DLL-FS

7.Hybrid frequency synthesizer

Many systems incorporate a mixture or hybrid of these basic approaches in order to take advantage of the benefits of increased speed or improved resolution that one approach may have over another. For example, sometimes a PLL synthesizer may incorporate a DDS in its reference circuitry to increase resolution or to reduce switching time. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurs in its reference and a DDS may have high spurs. The resulting noise at PLL output can seriously degrade system performance.

8.Summary And Comparison Of Synthesizers

The most widely used frequency synthesizer architecture is based on PLL. It can be easily integrated in current technologies, consumes reasonable power, and meets most of the wireless and wired RF applications. The brought fractional-N synthesis into maturity and is the dominant fractional-N synthesizer architecture. Direct analog synthesizers may find their applications in microwave, where very high frequencies need to be generated. Direct digital synthesis is used where frequency switching-time is very short, like frequency-hopping spread spectrum (FHSS) systems. A brief comparison of different synthesizer architectures can be found in Table 3 & 4.

Architecture	Pros	Cons
DAS	Fast switching, low noise and spur, good for microwave	Big size and power
DDS	Fast switching, fine resolution	Big power, high spur
Integer-N	Low power, low noise	Slow switching
FN-PLL	Relatively faster switching	Fractional spur
DLL	Very low noise	Non programmable, big power
Hybrid	Fast switching, low noise	More complex

Table 3:Comparison of Frequency Synthesizer Architecture

Parameters	PLL	DLL	DDFS
Phase Noise	PLL can shape phase noise from different contributors.	Good close-in spectrum	Phase noise roughly equals phase noise of digital clock
Spurious tones	f_{ref} away from carrier for fixed or integer-N $f_{channel}$ away from carrier for fractional-N	f_{ref} away from carrier	Caused by truncation in lookup table.
Channel resolution	Good for fractional-N based PLL, not directly related to reference.	Fixed frequency	Excellent
Switching time	Based upon reference frequency and loop bandwidth.	N/A	Fastest
Power	Low to moderate. VCO and dividers consume most power.	Moderate. Long VDL and edge combiner consume most power.	High. High-speed, high-resolution DAC and fixed-frequency PLL consume most power.
Others	Different architectures can be chosen based upon application.	Modulus determines number of stages in VDL. Not attractive for very high frequencies.	Complicated. Requires fixed-frequency oscillator and single-sideband mixer.

Table 4: Comparison of different synthesizers

9.Reference

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