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Design Of Low Power And High Speed RCA Using Boosting CMOS Differential Logic Style

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Abstract:
The low-voltage CMOS differential logic operating with supply voltage approaching the MOS threshold voltage. The logic style which is proposed improves switching speed. It has been done boosting the gate–source voltage of transistors along timing-critical signal paths. This logic style minimizes area overhead which is achieved by using the single boosting circuit is shared by complementary outputs. The proposed logic style improves Energy delay product compared with conventional logic styles. The supply voltage scales down toward the threshold voltage, the speed performance of conventional CMOS circuits, such as static CMOS logic, differential cascode voltage switch (DCVS) logic and domino CMOS logic is still severely degraded due to the reduced overdrive voltage (VGS − VTH) of transistors. To overcome this Problem, a bootstrapped CMOS large capacitive-load driver was proposed CMOS bootstrapped dynamic logic (BDL) was proposed. However, the speed of this logic style was not so much improved since the latency of bulky bootstrapping circuit was superimposed on the overall latency of the circuit. To overcome the problems and to further improve the switching performance, Boosting CMOS differential logic style is proposed .The BCDL provides higher switching speed than the conventional logic style at low supply voltage. The BCDL also minimizes area overhead by allowing a single boosting circuit to be shared by complementary outputs. The experimental result for Ripple Carry Adder using BCDL design with the proposed logic style.

Key words: *Adder, low power, low voltage, voltage boosting, Sequential Circuits.*

1.Introduction

The energy consumption of modern digital CMOS circuits has been traditionally dominated by switching energy having quadratic dependence on supply voltage; voltage scaling is an effective way to minimize the overall energy consumption of system-on-a-chip. In the extreme case, circuits can be made to be operated in the subthreshold region for maximum energy efficiency. However, the approach is limited to be only used in a low-end design, where speed is a secondary concern, because of severe speed degradation due to small switching current and high performance variability due to process, temperature, and threshold voltage variations. For medium- and high-end designs, where speed performance and energy efficiency are both important, that much aggressive voltage scaling is not acceptable, and instead, a near-threshold voltage design is more suitable for achieving relatively high energy efficiency without severe speed degradation.

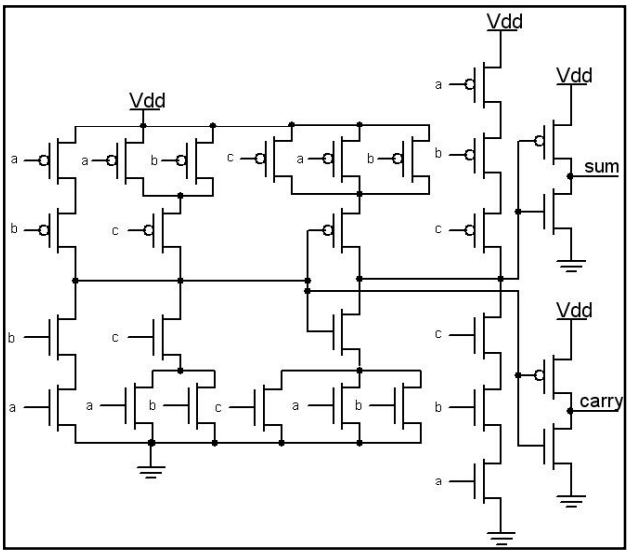

Figure1. 1: Conventional Cmos Full Adder

Figure1.1 shows the conventional CMOS 28-transistor adder. we are using this circuit for Differential logic tree and logic tree block for Fig. 1.2 and Fig. 1.3. The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may consist of several sub-branches. Mutually exclusiveness of pull-up and pull-down networks is of a great concern.

One possible implementation of the full adder is the Mirror Full Adder. This circuit device consists of 28 total transistors (4 transistors used for the construction of two inverters). Since the full adder acts as a fundamental building-block component to larger circuits units, timing and power consumption optimization efforts at the adder level can lead to improved circuit throughput ratings, enhanced speed performance, and lowered power consumption requirements. Thus at this fundamental level it is very important to minimize latency and resolve any timing issues in order to avoid issues inevitably brought about by scaling.

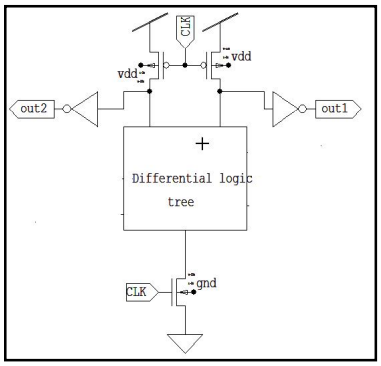

Figure1.2: Differential Cascode Voltage Switch (DCVS) Logic

As the supply voltage scales down toward the threshold voltage, the speed performance of conventional CMOS circuits, such as static CMOS logic, differential cascode voltage switch (DCVS) logic Figure.1.2, and domino CMOS logic Figure.1.3, is still severely degraded due to the reduced overdrive voltage (VGS − VTH) of transistors.

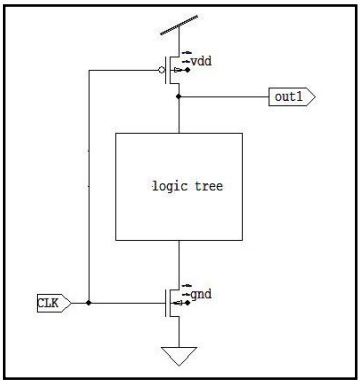

Figure1.3: Domino CMOS Logic

To overcome this Problem, a bootstrapped CMOS large capacitive-load driver was proposed. It can improve the switching speed at low supply voltage by allowing the

voltage of some internal nodes to be boosted beyond the supply rails. However, since the circuit was proposed for use as a large capacitive-load driver, logic functions cannot be efficiently embedded into the circuit.

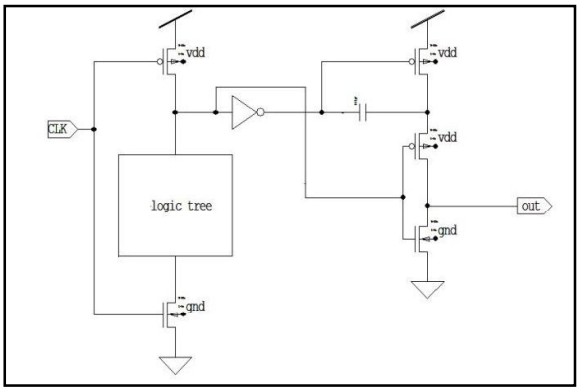

Figure1.4: Bootstrapped Dynamic Logic

For fast logic operation at low supply voltage, CMOS bootstrapped dynamic logic (BDL) Figure.1.3 was proposed. However, the speed of this logic style was not so much improved since the latency of bulky bootstrapping circuit was superimposed on the overall latency of the circuit. Moreover, logic composition of this logic style is constrained since it is configured as a single ended structure. Although some recent circuit techniques adopting bootstrapped operation have been proposed, they are all not for logic composition but for large capacitance driving.

To overcome the aforementioned problems and to further improve the switching performance, a novel boosting CMOS differential logic style is proposed in this brief. Section II describes the circuit structure and operation of the proposed logic style. In Section III, comparison results for some representative logic gates are presented to assess the performance of the proposed logic style. Section IV describes the experimental result for 64-bit adders as a design example to prove the practicality of the proposed logic style. Finally, we present the conclusion in Section V.

2.Circuit Structure And Operation

Figure. 2.1 shows a generic structure of the proposed logic style, i.e., boosted CMOS differential logic (BCDL). It consists of a precharged differential logic block and a voltage-boosting block. The voltage-boosting block, which is shown in the dotted box at

the lower part of the circuit, is composed of transistors MN2, MN3, and MP3 and boosting capacitor CBOOT and is used to boost the voltage of NP below the ground.

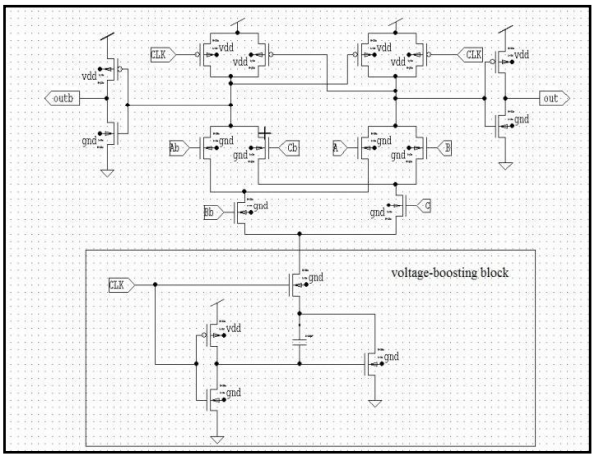

Figure.2.1: boosted CMOS differential logic (BCDL)

The Precharged differential logic block, which is composed of a differential logic tree with bottom transistor MN1, precharge transistors MP1 and MP2, and output inverters, receives the boosted voltage at NP and swiftly evaluates the output logic values. Let us explain the operation of BCDL. It has two phases of operation, namely, a precharge phase and a boosted evaluation phase. The circuit is in the precharge phase when CLK is low. During this phase, the precharged differential logic block is separated from the voltage-boosting block since MN1 is fully off. Precharge nodes P and PB in the differential logic block are then precharged to the supply voltage by MP1 and MP2, letting outputs OUT and OUTB identically low. At the same time, transistors MP3 and MN2 in the voltage-boosting block turn on, allowing NS and NP to be high and low, respectively. Then, a voltage identical to the supply voltage is applied across CBOOT. When CLK changes to high, the circuit goes into the boosted evaluation phase.

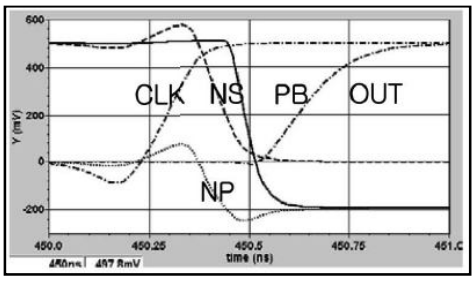

Figure 2.2: Simulated Waveforms of BCDL

The simulated waveforms of BCDL in this phase are shown in Figure. 2.2, where a supply voltage of 0.5 V is used. Since CLK goes high, MN1 turns on and connects the differential logic tree to the voltage-boosting block. At the same time, NS is pulled down toward the ground, allowing NP and NT to be boosted below the ground by capacitive coupling through CBOOT. As shown in Figure. 2.2, NP temporally reaches −250 mV and settles at around −200 mV by the boosting action. Then, the gate–source voltages of MN1 and transistors that are on in the logic tree are enlarged, resulting in an increased driving strength of these transistors. Moreover, a slightly forward source–body voltage established in these transistors by boosting source voltages below the ground leads to a reduction in threshold voltages of these transistors, further increasing their driving strength. In turn, the boosted voltage at NT is then transferred to P or PB through the logic tree, depending on input data. [In Figure. 2.1, input data are such that PB is pulled down below the ground.] Then, the gate–source voltage of the driver pMOS transistor is also enlarged, enhancing its driving strength. All these driving strength-enhancing effects by boosting are combined together along the timing-critical signal paths from the inputs to the outputs via precharge nodes, resulting in significantly improved switching speed at a low-voltage region.

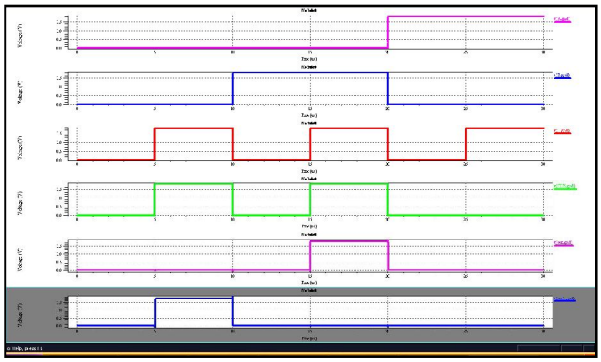

Figure 2.3: Waveform of Boosted CMOS Differential logic

Figure 2.3 show that Waveform of Boosted CMOS Differential logic. The waveforms for the input A, B & C and the output sum, carry and OUT are shown in figure. And this circuit Power output is 3.664276 in $e^{-005.}$

3.Simulation Comparison

To assess the performance of the proposed circuit technique,Various multi-input logic gates are designed using the conventional and proposed logic styles in a 0.18-μm CMOS

process. The nominal threshold voltages of p- and n-channel MOS transistors are −0.45 and 0.42 V, respectively. The boosting capacitor was implemented using the gate-oxide capacitance of a pMOS transistor. Transistor widths in each logic gate and the amount of boosting capacitance were individually optimized at each supply voltage for each logic style to provide a minimum energy–delay product (EDP).

CIRCUITS	**POWER** in e^{-005}	Power Delay Product in e^{-008}	Energy Delay Product in e^{-016}	Area Of Transistors in μn^2
DCVL	3.044238	6.268880718	39.298865457	1540
DOMINO CMOS	3.018206	23.84438770	56.855482491	1320
BDL	5.878986	4.297720875	18.470404722	1540
BCDL	3.664276	2.829166311	8.0041820169	792

Table 1.1: Simulated Power, PDP, EDP, Area of Full Adder circuits

The table 1.1 summarizes the simulated performance of various logic gates designed with the conventional and proposed logic styles. The simulation was executed at 100-MHz frequency with 1.8V supply. The domino CMOS and BDL, only the non-inverting outputs are available. For Full adder having the same input counts designed
with differential logic styles, the BCDL gates has larger energy than domino CMOS and DCVS gates due to the extra circuit to perform the boosting operation, it consumes still less energy than BDL gates. As for EDP, BCDL gates show the best performance, improvement over the conventional logic gates.The power analysis in different types of Circuits,

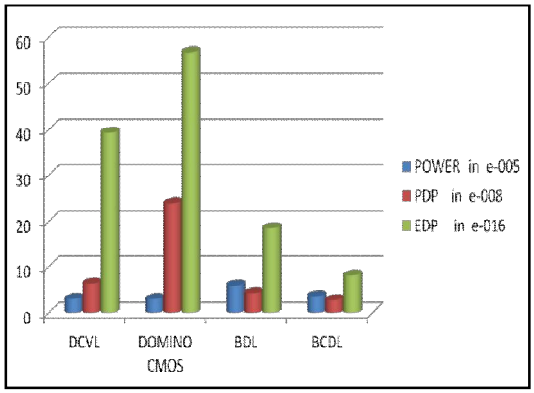

Figure 3.1: Power Comparison Chart

The Figure 3.1 shows the power analysis in different types of Circuits such as DCVL, DOMINO, BDL, BCDL on power PDF and EDP in milli watts.

4.Experimental Result

The 64-bit adder consisting of eight 8-bit adder subsections adopts the carry selection scheme for high-speed carry propagation. An 8-bit ripple carry chain was used in the BCDL adder to allow boosting operation at each carry chain stage, whereas an 8-bit Manchester carry chain was used in the DCVS and BDL adders for high-speed carry propagation.

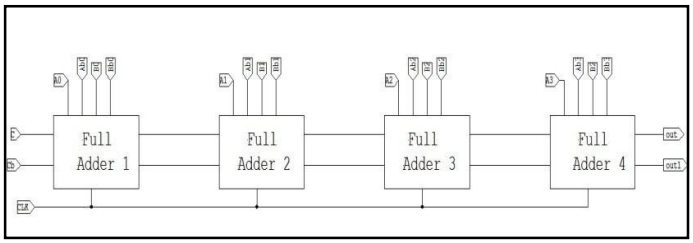

Figure 4. 1:Four Bit Ripple Carry Adder

Fig 4.1 shows 4 bit ripple carray adder with 4 full adders consisting of four inputs and a clock provided. The output of first full adder is given as input of second full adder. The prosses is repeated upto fouth full adder.

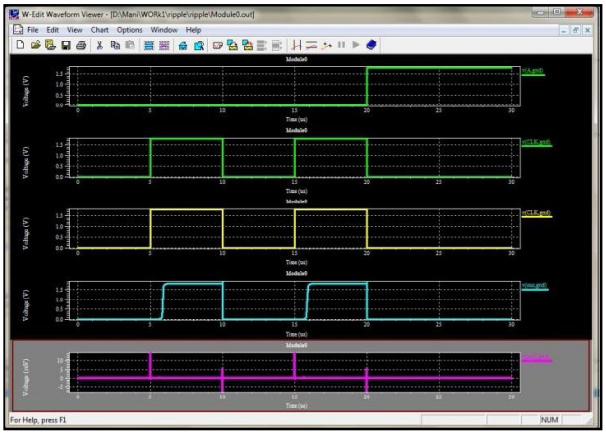

Figure4. 2: Waveform of Four Bit Ripple Carry Adder

Fig 4.2 shows simulated result of 4bit ripple carry adder Average power consumed by 4bit ripple carry adder is $1.175823e^{-002}$ watts, prower delay product is $2.865614694822\ e^{-008}$ and Energy delay product is $8.21166336e^{-016}$

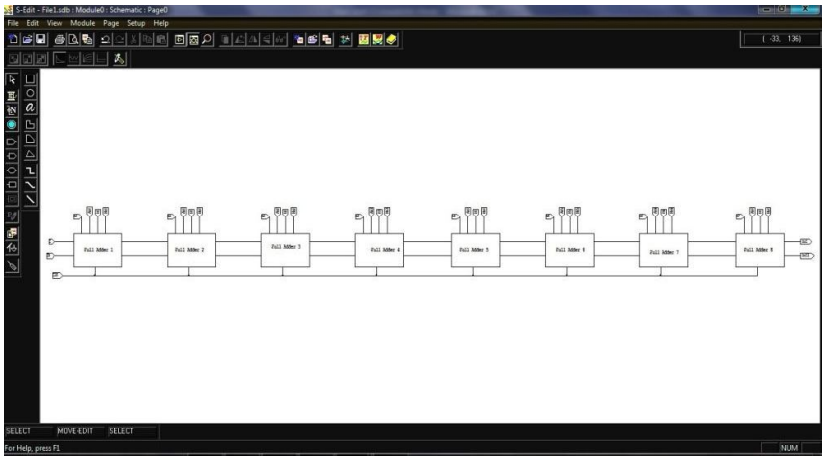

Figure 4. 3: Eight Bit Ripple Carry Adder

Fig 4.3 shows 8 bit ripple carray adder with 8 full adders. The output of first full adder is given as input of second full adder. The prosses is repeated upto Eight full adder.

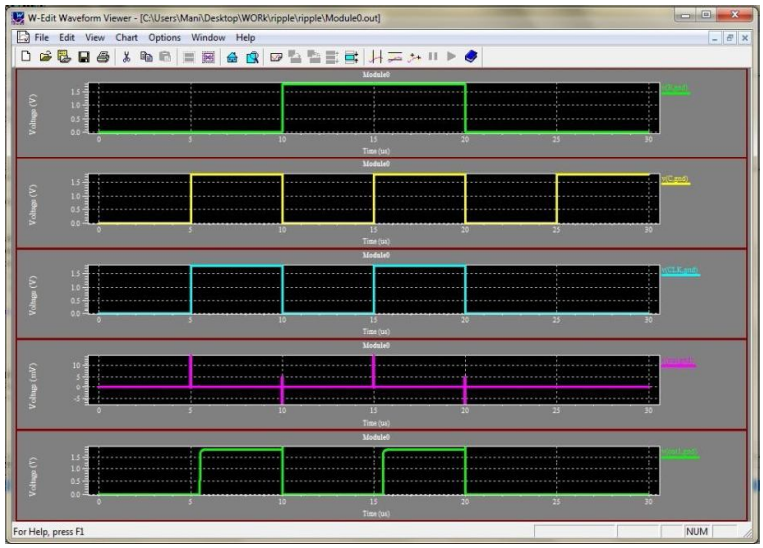

Figure 4. 4: Waveform of Eight Bit Ripple Carry Adder

Fig 4.4 shows simulated result of 8 bit ripple carry adder Average power consumed by 8 bit ripple carry adder is $2.595673e^{-002}$ watts, prower delay product is 5.521305 e^{-008} and Energy delay product is 30.49090616-^{016}

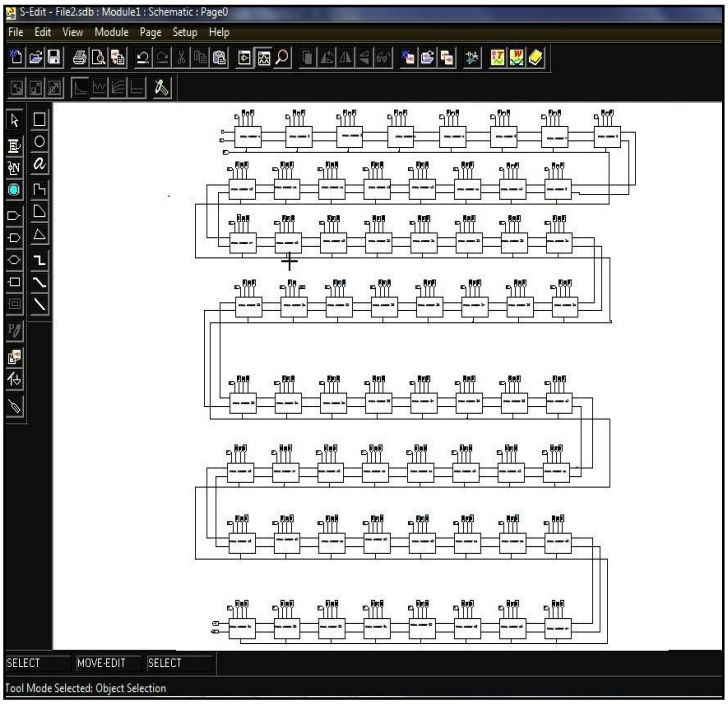

Figure 4.5: 64 Bit Ripple Carry Adder

Fig 4.5 shows 64 bit ripple carray adder with 64 full adders . The output of first full adder is given as input of second full adder. The prosses is repeated upto 64 full adder.

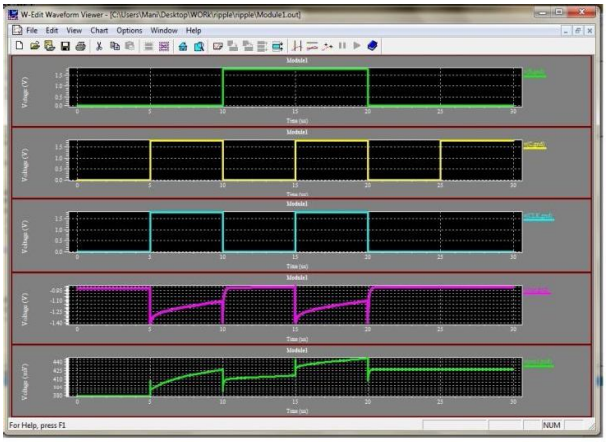

Figure 4. 6: Waveform of 64 Bit Ripple Carry Adder

Fig 4.6 shows simulated result of 64 bit ripple carry adder Average power consumed by 64 bit ripple carry adder is $4.993016e^{-002}$ watts, prower delay product is $11.41546e^{-008}$ and Energy delay product is $130.3128595e-^{016}$ Fig. 4.6 shows the structure of the 8-bit ripple carry chain used in the 64-bit BCDL adder. At 1.5-V supply voltage, the 8-bit

carry chain in the BCDL adder requires 2.13ns for propagating a carry value from the lowest to the highest bit positions, whereas the 8-bit carry chains in the DCVS and BDL adders require 8.95 and 7.49 ns, respectively, indicating 76% and 72% improvements.

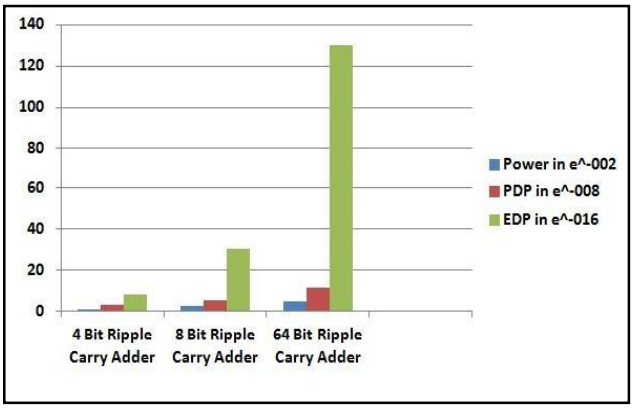

Figure 4.7: Output Of 4 Bit , 8 Bit And 64bit Ripple Carry Adder Chart

Fig 4.7 shows Output Of 4 Bit, 8 Bit And 64bit Ripple Carry Adder Chart. The power, EDP, and PDP levels all are reduced compared to Exciting methods of DCVL, DOMINO CMOS, BDL. from each 8-bit subsection goes into block-carry generators (BCG). There is a pair of BCGs in each 8-bit subsection in the upper half of the adder, and block carries are selected using the carry bit propagated from the lower half.

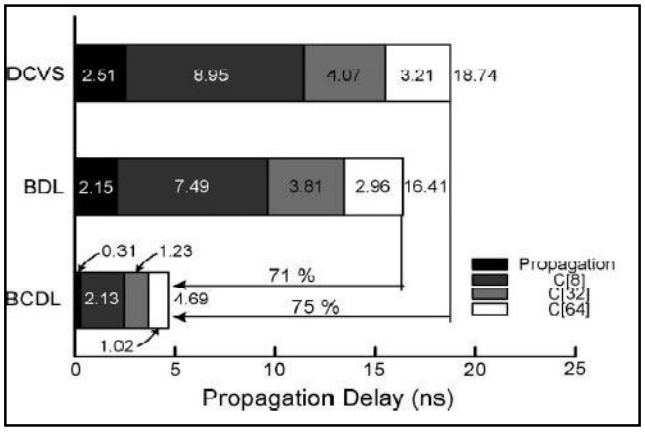

Figure 4.8: Addition Times Of The Adders

Fig. 4.8 compares the simulated addition times of the adders. The 64-bit BCDL adder achieves 4.69 ns at1.5-V supply. It indicates 75% and 71% improvements, as compared with the 64-bit DCVS and BDL adders having 18.74 and 16.41 ns, respectively. The

layout picture of the 64-bit BCDL adder occupying 1.39 × 0.39 mm2 is shown in Fig. 9(a) (64-bit DCVS and BDL adders occupy 1.16 × 0.41 and 1.61 × 1.41 mm2, respectively).

5.Conclusion

CMOS differential logic style with voltage boosting has been described. The BCDL provides higher switching speed than the conventional logic style at low supply voltage. The BCDL also minimizes area overhead by allowing a single boosting circuit to be shared by complementary outputs. Comparison results in a 0.180-μm CMOS process indicated that the energy–delay product of the proposed logic style was improved. We present two high-speed and low-power full-adder cells designed. Logic styles that lead to have a reduced power-delay product (PDP). We carried out a comparison against other full-adders reported as having a low PDP, in terms of speed, power consumption and area. 64-bit BCDL adder designed with the proposed logic style with a 0.18- m CMOS technology, and were tested. They provide high switching speed by low power consumption.

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