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Electrical Properties Of Thin Film Al-(N)Cdse/(P)Si-Al Heterojuction And Its Performance As A Photovoltaic Converter

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Abstract:
To fabricate the (n)CdSe/(p)Si heterojunctions, Ag-doped CdSe thin films of doping concentration up to 7.23×10^{16} cm^{-3} have been deposited onto p-type silicon wafer by sequential thermal evaporation technique. Different junction parameters such as diode ideality factor (n), built in potential (V_{bi}), reverse saturation current density (J_0), Richardson's constant (A^*), short-circuit current (V_{oc}), etc. were determined from current-voltage (I–V) characteristics. The ideality factor was found greater than unity with high series resistance (R_s). These parameters show significant changes with variations of doping concentration and temperature. The I-V characteristics under illumination showed poor photovoltaic (PV) effect. However the structures showed the change of PV effect, giving a fill factor (FF) 0.43 for annealed sample with an open-circuit voltage (V_{oc}) 100 mV, a short-circuit current density (J_{sc}) 13.2 μAcm^{-2} on increasing the doping concentration up to $N_d = 7.23\times10^{16}$ cm^{-3}. Large series resistance, high defect density and presence of interfacial layer are thought to be responsible for higher values of ideality factor and poor PV conversion efficiency. Proper doping and annealing are necessary to reduce the series resistance so as to achieve an ideal and high efficiency PV device.

Keywords: *Cadmium selenide (CdSe), thermal evaporation technique, diode ideality factor, photovoltaic effect.*

Introduction

Cadmium selenide with a 1.74eV direct gap is a promising II-VI semiconductor for optoelectronic devices [1-5] and its large absortion coeffient to visible region of solar spectrum gives good theoretical conversion efficiency and has led to the investigations of efficient solar cells. There are a number of reports on the structural, optical and electrical properties of polycrystalline thin films of CdSe [6-9]. Extensive studies have been made on different semiconductor/Si structures [10-12], but little attention has been focused on the fabrication of CdSe/Si structure. Hence there is a scope to study CdSe/Si heterojunction in the thin film form. Silicon with a 1.2 eV band gap is amphotaric whereas CdSe can be made n-type with small lattice mismatch between them. Various carrier transport mechanisms in semiconductor/Si junctions have been proposed so far. These properties have lead to the investigations of CdSe/Si heterojunctions for PV applications. Earlier we have reported photovoltaic properties of thin film heterojunctions of (n)CdSe/(p)CdTe [13], ITO/(p)Si [11] and ITO/(n)CdSe-Al [14]. In this work an effort has been made to investigate the heterojunction of polycrystalline CdSe thin film thermally deposited on Si wafer. Different junction parameters, doping effect, annealing and PV performance of the junction have been discussed here.

Experimental details

The samples were prepared on chemically cleaned glass substrates by sequential thermal evaporation (10^{-5} Torr) using suitable musk. The specifications of Si wafers used for fabrication of (n)CdSe/(p)Si heterojunction were: boron-doped (p-type), orientation (100), resistivity 10-20 ohm-cm, thickness 50000-55000 Å. Before junction preparation, the Si wafers were etched chemically by hydrofluoric acid. Initially, three Al electrodes, each of 1×15 mm^2 size, as back contacts were vacuum deposited on one side of (p)Si wafer (3×3 cm^2 size) to make ohmic contacts. On the top, Ag-doped CdSe films of 15×15 mm^2 area were thermally deposited by co-evaporation of CdSe powder (99.996%, Sigma Aldric, USA) from an electrically heated molybdenum boat and Ag metal (99.99%) from tungsten spiral filament as reported elsewhere [15]. The Ag doping makes CdSe an n-type semiconductor. During deposition, the substrate temperature was kept at 473K. Two sets of CdSe:Ag films of different doping concentrations were prepared by maintaining a constant deposition rate for CdSe and changing the evaporation rate of Ag. Before deposition of counter electrodes, the (n)CdSe/(p)Si structure was annealed in high vacuum for 1 hr at

373K in order to ensure crystallization of the film. Finally three upper electrodes of Al were vacuum deposited separately over the two sets of CdSe:Ag films, having the same geometry as that of the lower ones but being placed perpendicularly. The effective area, formed by the overlap of two perpendicular electrodes was 1 mm^2. Thus, two sets of Al-(n)CdSe/(p)Si-Al structures with nine junctions could be obtained (Fig.1).

For conductivity type measurement, thickness and other properties, separate films were deposited during respective CdSe film preparation by placing additional glass substrates. Al electrodes were deposited on CdSe films to measure conductivity. The film thicknesses measured by multiple interference technique [16] were found to be around 3500Å. The transmittance was studied using a UV-visible spectrophotometer (Cary 300, Varian, Australia). The conductivity type and carrier concentration of the films were determined by Hall effect measurement and analysis of the capacitance-voltage (C−V) plots [15] of the Schottky barriers. For films of lower doping, the hot probe method [17] was also used to confirm conductivity type.

To avoid humidity effects, noise and light, all electrical and PV measurements were made in a vacuum (10^{-2} Torr). The detailed experimental arrangement has been discussed elsewhere [18]. A Kiethley system Electrometer (model 6514) was used to measure current. The I−V plots of the junctions were recorded in vacuum at room temperature as well as at higher temperatures using a temperature-controller. To study I−V plots under illumination, the samples were illuminated through a glass window using white light from a tungsten-halogen lamp.

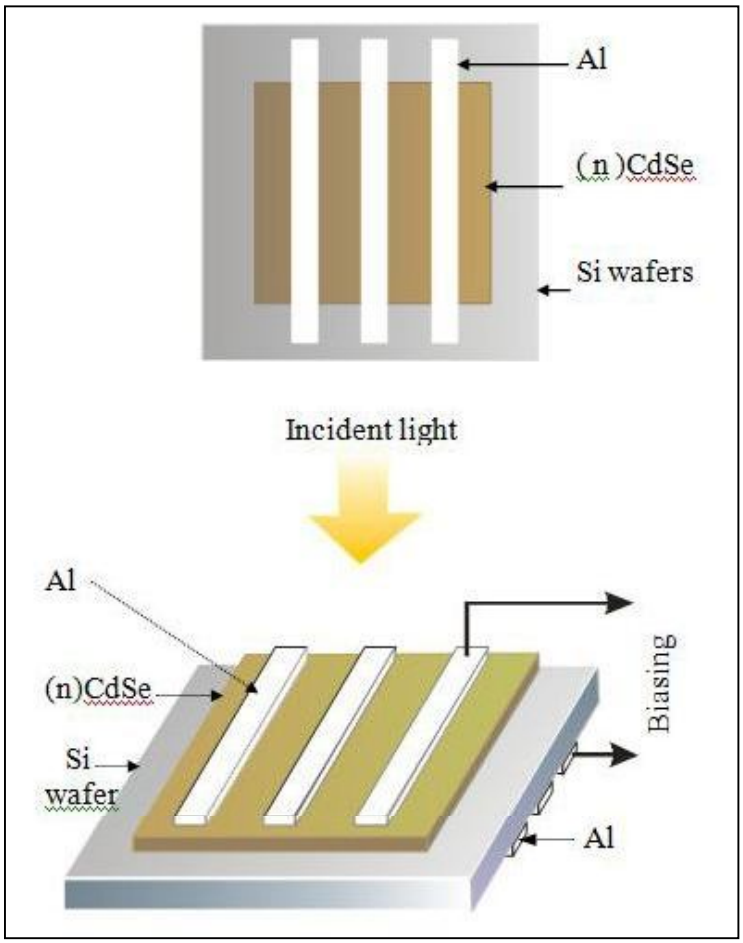

Figure 1: Al-ITO/(n)CdSe-Al structure (a) top view and (b) side view (not to scale)

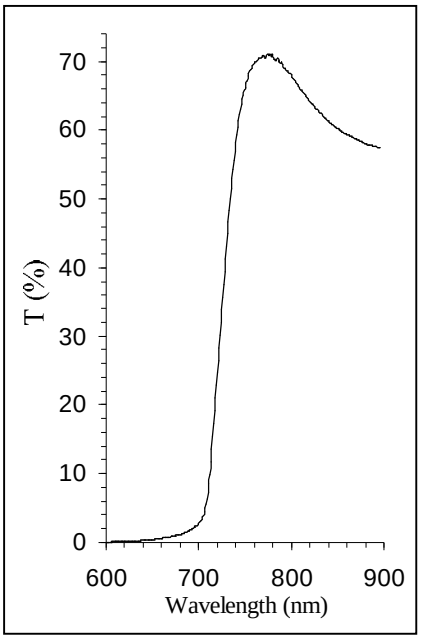

Figure 2(a): Transmittance vs wavelength of CdSe films of thickness 3500Å

Results And Discussion

The (n)CdSe films used to fabricate the junctions was found to possess the electrical conductivity of 8×10^{-3} $\Omega\square^{-1}cm^{-1}$, optical transmittance more than 75% beyond wavelength 750nm (Fig 2a). The best film performance was also thought to be associated with preferred orientation. As can be seen in figure 2 (b), the strongest peak of an XRD spectrum of a typical CdSe film used for fabrication is (002). We have not yet determined a dependence of film performance on orientation, but we have achieved however excellent electronic properties with the mixed orientation (fig. 2(b). The surface morphology of the CdSe films deposited at 473K shows a compact and fine-grained morphology without cracks or pinholes and uniform distribution of grains over total coverage of the substrate. The grains are packed very closely and the film has polycrystalline character. Fig. 2 (c) shows the SEM image of Ag-doped CdSe films. The morphologies of the CdSe and CdSe:Ag are quite distinct. After Ag doping, the increase in grain density favours coalescence between individual grains during lateral growth and explains an increase of the compactness of the deposits. Coalescence between grains is clearly seen in Fig. 2 (c). The larger grains appeared to grow by coalescence of smaller ones.

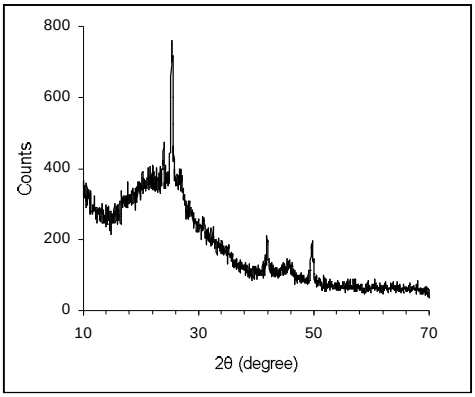

Figure 2(b): XRD spectrum of a typical CdSe film

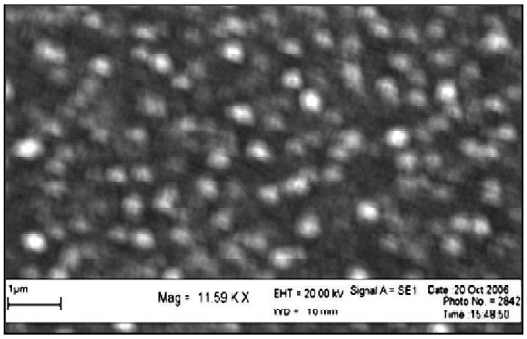

Figure 2 (c): SEM of Ag:CdSe film (3000Å thick) deposited at T_s= 473K (Magnification 11.59kX)

Hall-effect and hot-probe measurements confirmed n-type conductivity. The observed linearity of I-V characteristics up to 5 V of a sandwich structure of Al/(n)CdSe/Al indicates good ohmic contact upto ±5V. The dark current density (J)–voltage (V) plots of an annealed junction (M13) at room temperature exhibited rectifying nature (Fig. 3) indicating a barrier existing at the junction. Assuming thermoionic emission to be dominant over the junction barrier, J–V relation is

$J = J_0 (1-V/V_{bi})[\exp(qV/kT)-1]$ where $J_0 = (qA^*TV_{bi}/k) \exp(-qV_{bi}/kT)$ (1)

The n factor and J_0 values calculated respectively from the slope and intercept of linear regions of InJ-V plots (Fig. 4) are tabulated in table 1. The n >1 for both the structures.

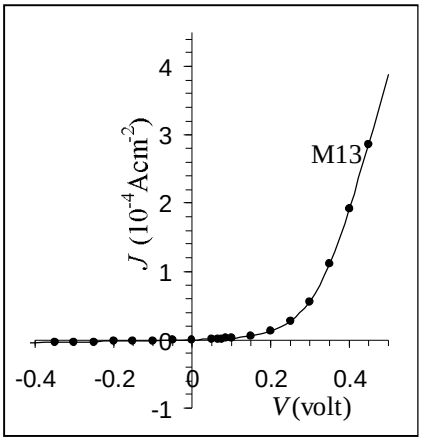

Figure 3: Dark J-V plots of a typical (n)CdSe/Si junction at room temperature

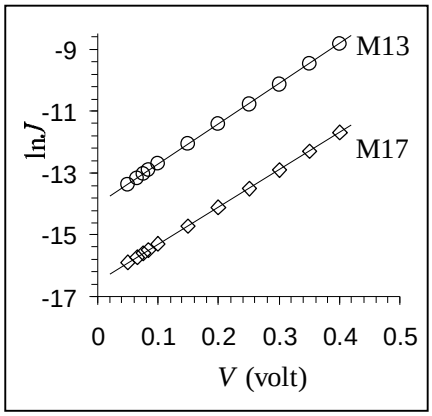

Figure 4: Dark lnJ–V plots of two typical (n)CdSe/(p)Si junctions at room temperature

Sample no.	N_d (cm^{-3}) (CdSe)	n	J_0 ($10^{-8}Acm^{-2}$)	R_s (KΩ)	V_{bi} from J-V study
M13	7.23×10^{16}	2.66	34	1.63	0.77
M17	1.18×10^{16}	4.10	1	8.32	0.76

Table 1: Junction parameters of typical (n)CdSe/(p)Si junctions in dark at room temperature

The presence of an interfacial layer, image-force lowering, and carrier recombination due to surface states or defect levels are responsible for $n > 1$. However higher doping (M13) was found to enhance diode quality. The V_{bi} values calculated from J_0 values are given in table 1.

At forward voltages > 0.4V, the deviation of ln$I$–V plot from linearity (Fig.5) indicates series resistance (R_s) associated with the semiconductor neutral region [19]. At a large forward current (I), the voltage drop across R_s causes the actual voltage drop across the barrier to be less than that applied to the device terminals. Various defects crept into the film during deposition, lower doping and an interfacial layer contributes large series resistance of the order of KΩ (Table. 1) that decreased on increasing doping and heat treatment, thereby improving diode quality.

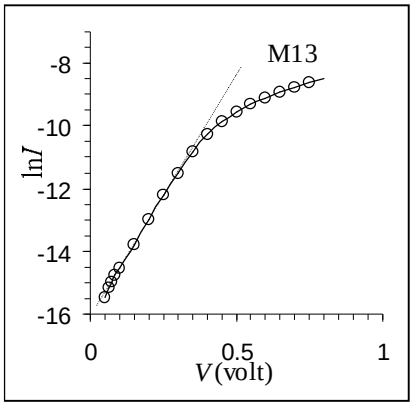

Figure 5: Dark lnI–V plot of a typical (n)CdSe/(p)Si junction at room temperature (305K)

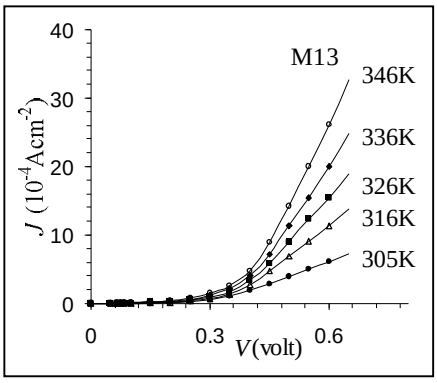

Figure 6: J–V plots of a typical (n)CdSe/(p)Si junction at different temperatures.

Temp. (K)	J_0 (10^{-5}A.cm^{-2})	n	Built in potential (eV)	A^* (Am^{-2}K^{-2})
305	34	3.66	0.77	62
316	84	3.65	0.78	
326	182	3.67	0.78	
336	288	3.67	0.79	
346	562	3.65	0.78	

Table 2: Variation of junction parameters of a typical junction (M13) with temperature in dark

Figure 6 shows the temperature dependence of *J-V* plots of (n)CdSe/(p)Si junction. Beyond room temperature; thermal generation of extra carriers causes a gradual increase of forward current. The J_0 values calculated from the linear portions of dark *lnJ–V* plots (not shown) for a typical junction (M13) at different temperatures were found to increase with temperature (Table 2) and n factor was found to be nearly same. The $\ln(J_0/T)$-T^{-1} plot (Fig.7) is a straight line and intercept on the vertical axis gives a Richardson's constant A^* around 62 (Table 2). Thus at this moderate doping the thermoionic emission is believed to be dominate current transport [20].

The increase of doping concentration slightly affects V_{bi} value (Table 1). For junctions of sputtered CdSe/(p)Si, Koshy *et. al*. reported exactly a 0.76 eV barrier height [21] which slightly deviated from the expected value due to non-stoichiometry caused by the dangling bonds [22]. Presently the barrier height is less dependent on work function [23]. Only for stoichiometric surfaces, the barrier height depends on the work function [24]. Also the thin interfacial oxide layer formed on air exposure may influence the barrier height [25].

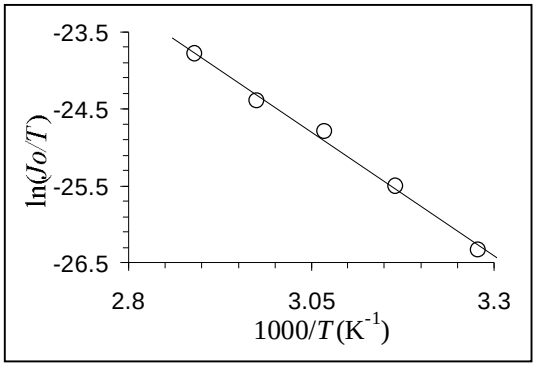

Figure 7 : $\ln(J_0/T)$–T^{-1} plots of (n)CdSe/(p)Si junction (M13)

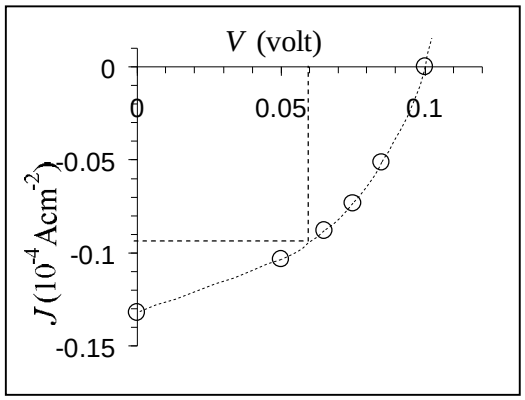

Figure 8: Photovolaic plot of a typical annealed (n)CdSe/Si junction (M13) at room temperature

Photovoltaic Effect

The annealed (n)CdSe/(p)Si junctions (M13) were observed under illumination (50 $mWcm^{-2}$) for PV performance (Fig 8). The nearly linear J-V plot indicates a high series resistance. The V_{oc} and J_{sc} values strongly depend on R_s as well as on n as per equations [26]

$$I_{sc} = I_0 [\exp\{q(V-IR_s)/kT\}-1]-I \quad \text{and} \quad V_{oc} = (nkT/q)\ln(I_{sc}/I_0 + 1)$$

where, I is total output current and I_0 the saturation current. Very low values of V_{oc} (100mV), J_{sc} (13.2 μAcm^{-2}) with FF 0.43 has been found. In the polycrystalline films, the grain boundary potential may be responsible for high series resistance and open-circuit voltage [27]. The photo generated carrier recombination at grain boundary reduces J_{sc} values [28]. High defect density, presence of interfacial layer and lower doping cause poor PV performance.

Conclusion

The rectifying (n)CdSe/(p)Si heterojunction diode can be fabricated by thermally depositing CdSe films on Si substrate. The poor conductivity of CdSe films contributes to the high series resistance of the diode. The photo generated carrier recombination, surface states, low doping concentration are also responsible for deviation of the J-V characteristics from ideality as well as for poor PV performance. The works are on progress to improve the diode quality and PV performance by optimizing the deposition parameters of CdSe film and post deposition annealing for suitable conductivity, transmittivity and best quality CdSe polycrystalline film.

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