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Reducing Leakage Current And Improving SRAM Cell Stability Using Independent –Gate Finfet Technology Over Conventional CMOS Technology

Kalpana Agrawal
Dept. of VLSI, Mewar University, Gaziabad, India
Gaurav Jain
Dept. of ECE, RKGIT College of Engg., Gaziabad, India
Prof.K.K Tripathi
Dept. of ECE, RKGIT College of Engg., Gaziabad, India

Abstract:
In VLSI technology conventional CMOS transistors are continuously scaling down to obtain faster speed of devices and very large scale integrated circuits. But the main drawbacks of CMOS scaling are high leakage current and heavy channel doping. So using CMOS SRAM beyond 45nm cell stability and controlling leakage current are becoming difficult in today's fast low power applications. FinFET may be an alternative of conventional CMOS transistor. In this paper independent double -gate FINFET structure based SRAM 6-Tcell has been proposed to controlling leakage current and improving SRAM cell stability . By adjusting threshold voltage(V_t) without affecting cell ratio we can reduce leakage current so that power during off state of transistor. In conventional CMOS due to heavy channel doping carrier mobilities are reduced which also increases process variations. In independent double gate FINFET technology, two separate gates are used. Threshold voltage of one gate can be altered by varying the voltage at the other gate. In this technology nearly intrinsic channel is used so carrier mobilities will be higher which results in higher speed of devices. Using the thin silicon fin, ratio of I_{ON}/I_{OFF} can also be increased. Due to vertical gate, there will no overlapping between source-gate and drain-gate so depletion and junction capacitances will be effectively eliminated. Wiring delay and bitline capacitance of SRAM will also be reduced .
Keywords: *conventional CMOS, FinFET, SRAM, leakage current, threshold voltage(V_t).*

1.Introduction

As SRAM occupies a large area in any memory chip so it consumes a large power. It is necessary to scale down conventional CMOS 6-T SRAM cell to obtain high speed. As the channel length of a conventional CMOS is reduced to the nanometer scale, main obstacles are short channel effects, sub-threshold leakage current, reduced carrier mobilities due to heavy channel doping and device-to-device variations [1]. At sub-45nm channel lengths, obtaining a large current drive while maintaining a low off-state leakage current becomes challenging [2]. The use of independent gate FinFET can provide better control of short-channel effects, lower leakage current and better carrier mobilities [3,4]. In the FinFET, independent control of front and back gate can be used to improve the performance and reduce power consumption[5].The cell leakage is commonly suppressed by using a higher transistor threshold voltage . Utilizing a higher transistor threshold voltage also helps to improve the read margin[15].

This paper explores the use of independent gate FinFETs for SRAM, which have emerged as promising substitutes for conventional CMOS at the 32nm technology and beyond. FinFETs are reported to have much shorter delay and less power consumption compared to traditional CMOS devices at the 32nm technology [13].

The paper is organized as follows. FinFET structure and modes are described in Section II; Conventional CMOS SRAM design challenges are described in Section III; CMOS 6-T design tradeoff's in Section IV; The new independent – gate FinFET SRAM 6-Tcell is presented in Section V; Results are given in VI;Finally ,some conclusions are offered in Section VII.

2. Finfet Structure And Modes

FinFETs are double-gate devices.There are two types of FinFETS : shorted gate (SG) and independent –gate(IG) FinFETs. The two gates of FinFET can either be shorted for higher perfomance or independently controlled. In SG FinFET, both gates are tied with each other. In IG FinFET, both gates are independent so can be controlled separately for lower leakage or reduced transistor count. Figure 1 shows the basic structure of FinFET for SG and IG mode.

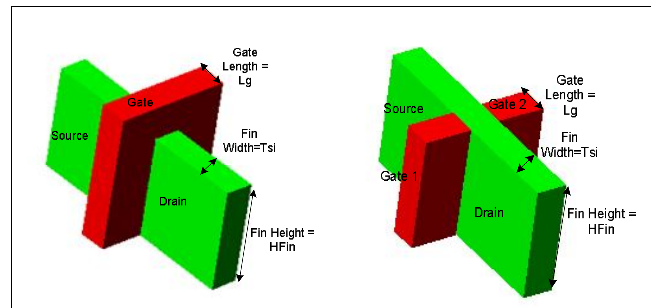

Figure 1(a): FinFET Structure SG Mode. Figure 1(b): FinFET Structure IG Mode

Rather than a plane Si surface, FinFET structure has a Si fin as the channel, the two gates are on the both sides of channel which are electrically isolated from the channel using a thin insulator. These two gates can allow for the independent operation[15]. The various dimensions of FinFET structure are as follows:

H_{FIN} :Height of silicon fin, Lgate:Physical gate length, T_{si}:Thickness of silicon fin, T_{ox}:Thickness of the oxide layer, Wg:Width of source/drain; W_{FIN}:Width of silicon fin defined as W_{FIN}=2H_{FIN} + T_{si} . For example if H_{FIN} =45nm, T_{si} =5nm then W_{FIN} =95nm.By using very thin silicon fin, short channel effects(SCE) can be suppressed greatly[19]. Due to light doping and thin body of FinFET depletion and junction capacitance will also be lower. Additional factor of FinFETs double gates are self aligned to each other and to source and drain which gives high performance and better control of channel length.

3.Conventional Cmos Sram Design Challenges

CMOS scaling has traversed many anticipated barriers over the past 20 years to rapidly progress from 2 μm to 90nm . For further CMOS scaling, subthreshold and gate-dielectric leakages have become the dominant barrier . Conventional CMOS scaling beyond the 45 nm channel length requires heavy channel doping to control Short Channel Effects (SCE) and heavy super-halo implants to control sub-surface leakage currents. Heavy doping degrades the carrier mobility and increases parasitic junction capacitance.

In the power consumption equation $P = CV^2f$, operating voltage is main factor for reduction of power but if we decrease operating voltage,the gate delay t_d and maximum clock frequency f_{max} of a chip degrade by the equations(1) &(2)[16].

$$t_d \propto \frac{V_{dd}}{(V_{dd}-V_t)^2} \quad (1)$$

$$f_{max} \propto \frac{1}{t_d} \propto \left(1 - \frac{V_t}{V_{dd}}\right)(V_{dd} - V_t) \quad (2)$$

A better solution to scale down is to decrease threshold voltage V_t but decreasing threshold voltage increases leakage current exponentially. Also process variations of threshold voltage does not scale accordingly[17].

Independent gate FinFETs, in which a second gate is added opposite the traditional (first) gate, have better control over short-channel effects [SCEs]. SCE limits the minimum channel length at which an FET is electrically well behaved.

4.Conventional Cmos Sram Cell Stability

4.1.Read Failure

The read stability of the cell can be defined using the static noise margin (SNM). SNM is calculated by the side of the largest square inside the SRAM cross-coupled inverter characteristic measured during the read condition [15]. A read failure occurs in the SRAM cell when enough charge on the bitline is transferred to the internal cell storage node and flips its state during a read access. In CMOS scaling, to improve the read stability is to increase the cell ratio (β)by upsizing the NMOS pulldown transistor or downsizing the NMOS access transistor[7].

4.2. Write Failure

The write stability of the cell can be quantified using the write noise margin (WNM), given by the smallest square

that can fit between the butterfly curves from both a read and a write simulation [18]. A write failure occurs when insufficient charge is transferred from one of the storage nodes to the grounded bitline . Write stability can be improved using a weaker pull-up transistor or larger access transistor[7]. So there is trade off between read stability and write stability.

5.The Proposed Independent – Gate Finfet Sram 6-Tcell

Figure 2 shows the independent gate FinFET SRAM with additional feature level shifter(LS). Two threshold voltage control lines V_{G2n} and V_{G2p} are connected with LS. Second gate of each transistor in SRAM is connected with V_{G2n} or V_{G2p}

correspondingly. These two control lines are parallel with world line(WL). WL is also connected with LS.A level shifter is coupled between the first gate and the second gate of each transistor. The level shifter is configured to select a supply voltage output for a circuit including one of the first supply voltage and the second supply voltage in accordance an input signal, where the input signal depends on at least one of an operation to be performed .

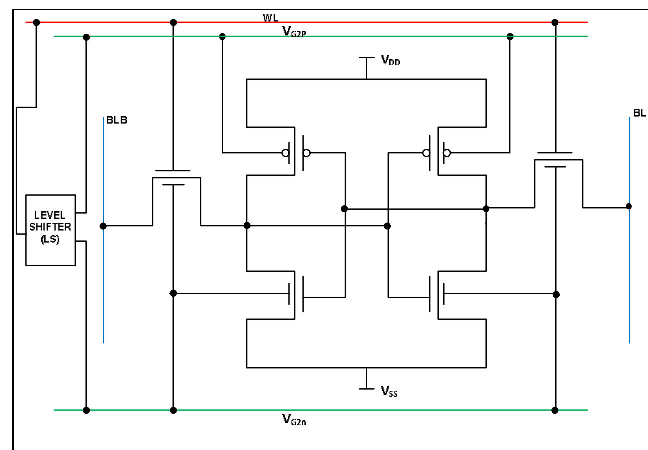

Figure 2: Proposed Independent Gate FinFET 6-T SRAM Cell

When read or write operation is to be accessed, threshold voltage(V_t) of each transistor is decreased using LS. This gives high I_{ON} current and improves static noise margin(SNM). During standby mode, V_t of each transistor is increased using LS through control lines which reduces I_{OFF}. Threshold voltage V_t is flexible and control the whole operation.

6. Results

In proposed FinFET SRAM, apart from WL , BL and BLB lines, the cell has two other control gates for the access, the pull-down, and the pull-up transistors. Figure 3 shows the curve for short circuit current. To balance the drivability of the transistors, both of the VG2n and VG2p need to be controlled in the opposite direction. The butterfly curves of the FinFET SRAM do not change with the bias voltages because the beta ratio of access to the pull-down transistor is unchanged. The short circuit current in the circuit can be flexibly controlled by the second gate bias voltage . By controlling threshold voltage V_t of each transistor not only the static leakage current, but also the dynamical power consumption can be controlled by independent gate FinFET SRAM.

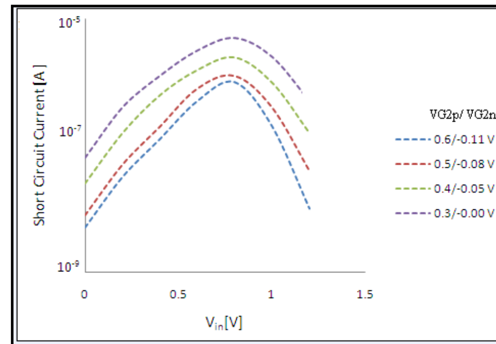

Figure 3: Short Circuit Current Curve for Different Values of Control Gates

7.Conclusion

This paper proposed independent gate FinFET SRAM using Level Shifter(LS). By controlling the threshold voltage V_t of FinFET transistor using double gate, standby leakage current can be greatly suppressed. Dynamic power consumption can also be reduced.Two control lines VG2n and VG2p are used to control the threshold voltage of every transistor. VG2N control line is used to control access and pull down transistor. VG2p control line is used to control pull up transistor. So FinFET technology is the future of faster devices.

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