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Performance Characteristics Of Cmos Circuits In Sodel(Silicon On Depletion Layer) Cmos Over Conventional Cmos Technology

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Abstract :

In this paper, the switching performance of SODEL(silicon on depletion layer) CMOS is investigated with a view to realizing high speed and low power CMOS applications. Due to smaller parasitic capacitance , the propagation delay time in SODEL CMOS has been improved by up to 25% compared to that of conventional CMOS in 5 stacked NFET inverters at the same Vdd . Also, power-delay product is better by 30% in SODEL CMOS. Latch-up immunity for alpha particle irradiation in SODEL is found to be better than conventional CMOS. So SODEL CMOS device's circuit technology is expected to provide a better solution for low power system-on-chip applications.

1.Introduction

Recently, partially depleted SOI (PD-SOI) CMOS devices have emerged as one of the promising solutions for high-performance CMOS applications[1]. It is offering many advantages over conventional bulk CMOS, such as larger I_{dsat} (saturation current)due to the floating body effect (FBE), smaller junction capacitance (Cj) and less body effect[2]. However, there are many disadvantages to be overcome concerning PD-SOI CMOS devices , such as the history effect , wafer quality and cost , gate oxide integrity , self-heating , and additional option of body contact to fix the body potential [3][4]. If desirable SOI CMOS device characteristics were realized using conventional bulk CMOS technology, a better solution would be available for high-performance and low-power CMOS , and especially so for system-on-a-chip(SoC) applications[5].

The new MOSFET device concept of silicon on depletion-layer FET(SODEL FET) has been proposed to achieve high-performance in future CMOS applications. For example , SODEL FET on a bulk silicon wafer has an artificial depletion layer which works as an insulator like a buried oxide(BOX) in SOI MOSFET[3]. The artificial depletion layer is formed by n/p-/n junction beneath the channel region. In contrast to PD-SOI devices , the holes generated by impact ionization can be swept away from channel region to substrate , and therefore , the kink effect or the history effect will be suppressed in SODEL FET[7].

2.Fabrication Of Sodel Cmos

SODEL CMOS device has the depletion layer region beneath the channel region which works as an insulator like a buried oxide (BOX) in SOI CMOS device.[8] SODEL CMOS is fabricated with bulk CMOS compatible process; however , fabrication of the depletion layer region requires the silicon epitaxy technique in the channel region to optimize the impurity profiles , and also requires two additional mask and ion implant processes in both NFET and PFET[5]. By forming stacked p/n-/p region beneath the channel region , the depletion layer is extended below the source/drain region. Therefore , smaller junction capacitance and smaller body effect have been achieved in SODEL NFET. Figure 1 shows the fabrication process of SODEL CMOS[6].

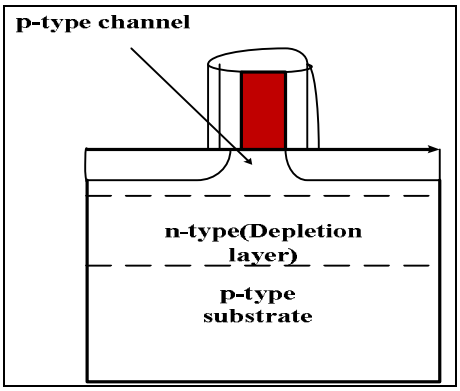

Figure 1: Fabrication Process of SODEL CMOS

Process sequence of SODEL CMOS fabrication :

- Isolation
- Well / Channel dopant ion implant
- Counter dopant ion implant(for depletion region formation)
- Channel Si epitaxial growth(selective,thickness~60nm)
- Vt adjustment ion implant
- Polysilicon gate formation(tox~1.1nm,Lpoly~30nm)
- Optional halo implant
- S/D extension ion implant
- Gate sidewall formation
- S/D deep junction ion implant
- Activation RTA
- NiSi salicide process
- Metallization(single metal process)

3. 5-Stacked Nfet Inverters

In these circuits , there are 2 circuits (top switching and bottom switching). Logically , the result will be same but due to different switchings , due to different parasitics such as body effect , the propagation delays due to inverters in top switching and bottom switching will be different[7].

Circuit diagram of 5-stacked NFET inverters is shown in Figure 2.

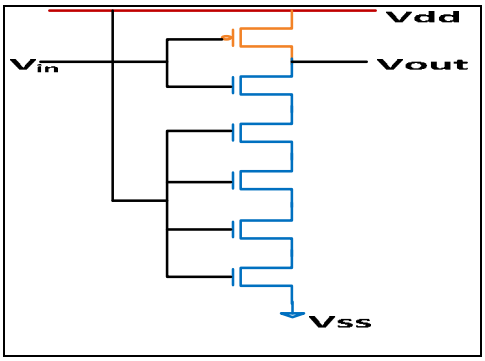

Figure 2 (a): Top switching

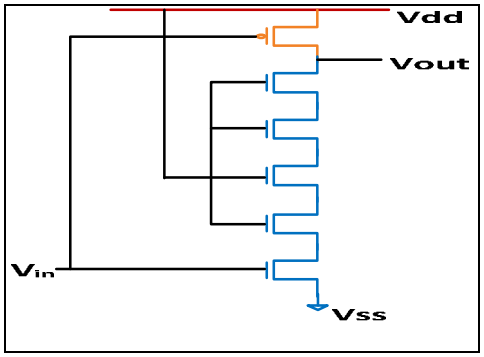

Figure 2 (b): Bottom switching

Also, the relative comparisons between SODEL CMOS device and conventional CMOS device , the top switching is better by 11% and bottom switching is better by 25% in SODEL CMOS. Also , the bottom switching propagation delay is higher than top switching in both the cases because in bottom switching , the body effects of all the 4 NFETs come into effect as a result the threshold voltage is increased , which results in an increase in propagation delay[2]. While in top switching , the body effects come into picture but in that case , the output voltage Vout is discharged to Gnd at a fast rate since all the 4-bottom NFETs are already having a path to ground since their gates are connected to Vdd[6]. So, the discharge rate is faster. While in case of bottom switching , as soon as Vin=1, the NFETs discharge Vout to Gnd , but the rate of discharge is slower since initially , the NFETs sources were floating. Also, in top & bottom switching , there is a difference in parasitics capacitances.

4. Result

In Figure 3,circuit simulations of 5-stacked NFET inverters shows that the SODEL CMOS device gives 11% reduction in top switching and 25% reduction in bottom switching. Also, the power-delay product is reduced by 30%. Also, the write-data times in SODEL CMOS SRAM is 98ps compared to 130ps in conventional bulk CMOS as shown in Figure 4. Applying SODEL CMOS to logic circuit, the faster switching speed at fixed Vdd can be also converted to the low-power dissipation operation mode, by reducing Vdd while keeping the same switching speed. Better bitline delay performance can be achieved in SODEL CMOS SRAM due to the smaller bitline capacitance. The generated current by α-particle irradiation is also negligble for the SCR current and the latch-up immunity in SRAM cell is not degraded SODEL CMOS structure.

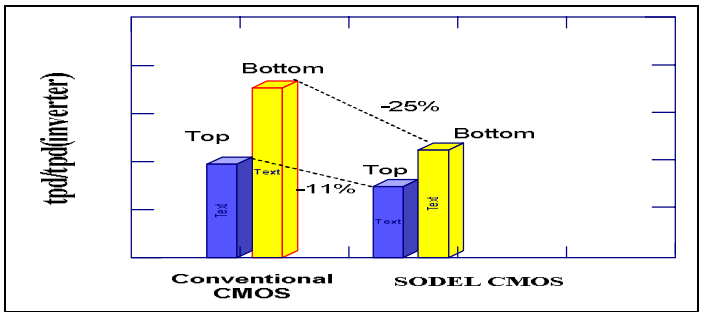

Figure 3: Relative comparisons of propagation delay times in top switching and bottom switching in SODEL

CMOS as well as conventional CMOS technology

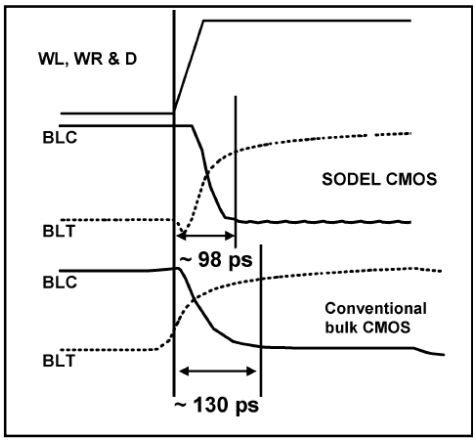

Figure 4: Comparison of bit line voltage waveforms between SODEL CMOS and conventional CMOS.

5. Conclusion

SODEL CMOS is a viable solution for high speed and low-power applications. SODEL CMOS technology

can realize higher AC performance. Propagation delay time and power-delay in SODEL CMOS will be about 20% smaller than in conventional CMOS. The write-data times in SODEL CMOS SRAM is 98ps compared to 130ps in conventional bulk CMOS. The performance is also improved due to smaller parasitic capacitance and smaller body effect.

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