INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN: 2278 – 0211 (Online)

Design Of Low Power Reversible Multiplier

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Abstract:

Reversible logic has received great attention in recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. The classical set of gates such as AND, OR and EXOR are not reversible. This paper proposes a 4x4 bit reversible multiplier circuit using Peres gate which can multiply two 4-bit numbers. It is faster and has low hardware complexity compared to the existing designs. In addition, this reversible multiplier is better than the existing counterparts in terms of delay and power because the Peres gate reduces the garbage output. It is based on two concepts, The partial products can be generated in parallel using Peres gates and thereafter the addition is done by using reversible parallel adder designed from Peres gates. Thus, this paper provides the initial threshold to building of more complex system which can execute more complicated operations using reversible logic.

1. Introduction

Power dissipation is one of the important parameters in the digital circuit design. In VLSI circuit designing power dissipation plays an important role. The conventional combination logic circuits dissipate heat for every bit of information that is lost during operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit if it is constructed using reversible logic gates will allow the recovery of the information. In 1960s R.Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. It provided that the loss of one bit of information dissipates KTln2 joules of energy were K is the Boltzmam's constant and T is the absolute temperature at which the operation is performed. Later Bennett, in 1973 showed that in order to avoid KTln2 joules on energy dissipation in a circuit it must be built from reversible circuits. This is because reversible computation does not require erasing any bit of information and computation requires reversible logic circuits and synthesis of reversible logic circuits differs significantly from its irreversible counter part because of different factors.

It is clear that reversible circuits will play dominant role in future technologies. These facts motivated many researchers to work in this domain. A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern. Thus reversible logic circuits avoid energy loss by uncomputing the computed information by recycling the energy in the system. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of counts and garbage generation. Reduction of these parameters is the main design focus. Reversible circuits for different purpose like half adder, full adder, and multiplier have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio video devices. It is important for every processor to have a high speed multiplier. Multiplier circuits essentially have two components: partial product generation and parallel full adder. Several 4x4 reversible gates have been used in reversible multiplier designing to construct the full adder. The two major constrains in reversible logic are to minimize the number of constant input and garbage output. The extra input that is added to make function reversible called constant input whereas extra output that is not necessary for further computations is called garbage output

2. Basic Reversible Logic Gates

In Reversible Logic Function for each input pattern there must be a unique output pattern and the Reversible logic operations do not lose information and dissipate very less heat, Thus, Reversible logic is likely to be in demand in high speed circuits. The basic important reversible gates are, Feynman Gate (FG) which is the only 2*2 reversible gate which is as shown in figure 1(a) and it is used most popularly by the designers for fan out purpose. There is also a double Feynman gate (F2G) depicted in figure 1(b), Fredkin Gate (FRG) depicted in figure 1(c), Toffoli gate depicted in figure 1(d) , all of which can be used to realize important combinational functions and all are 3*3 reversible gates. This figures also shows the switching functions for terminals.

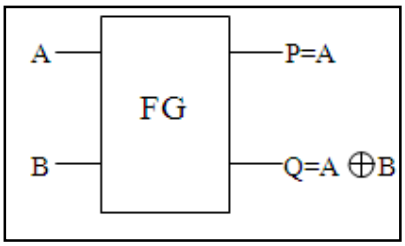

Figure 1(a) : Feynman Gate

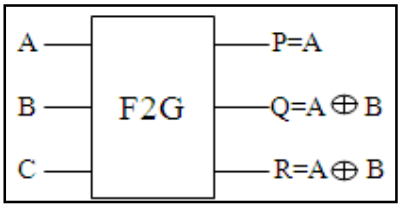

Figure 1(b) Double Feynman Gate

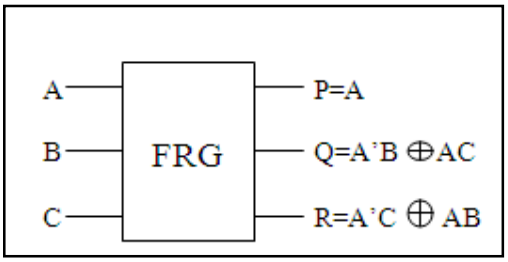

Figure 1(c): Fredkin Gate

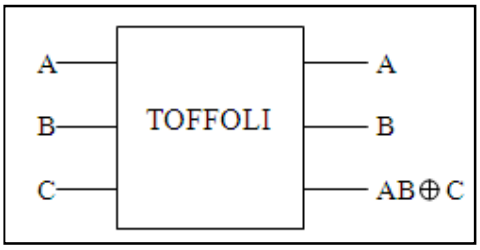

Figure 1(d): Toffoli Gate

3. Proposed Contributation

The design of proposed multiplier is based on parallel operation is done using two steps

Part I : Partial Product Generation (PPG) Part II: Summation Network

As mentioned before, the purpose of this paper is the design of Reversible multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency. The proposed multiplier is implemented using Peres gates. The operation of a 4*4 Reversible Multiplier is shown in figure 2. It consists of 16 Partial product bits of the four input bits X and Y to perform 4*4 multiplications.

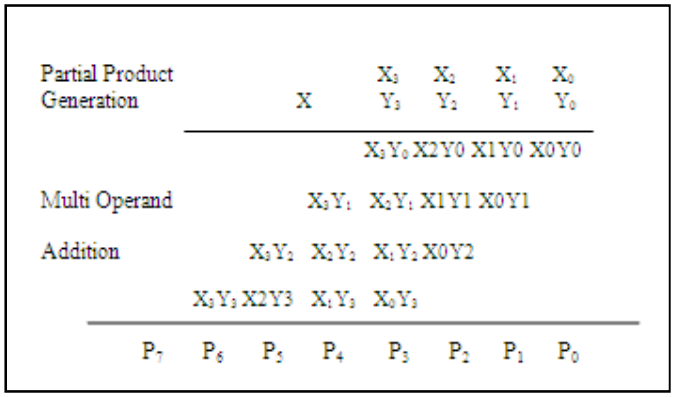

*Figure 2: Working of 4*4 parallel multiplier*

3.1 Partial product Generation

For partial product term generation the Peres gate is used. The Peres gate is used to perform AND operation by forcing one constant input as logic 0 whereas it produces required product term along with two garbage outputs. Here by forcing the input C as logic 0 we get the product of inputs A and B in the output R. The P and Q are the garbage Outputs. The figure 3(a) shows the AND operation using Peres gate and quantum representation of Peres gate is shown in figure 3(b).

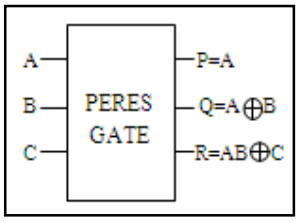

Figure 3(a): Peres gate

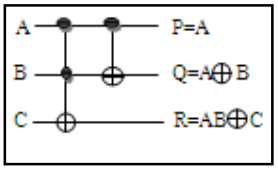

Figure 3(b): Quantum representation of Peres gate

Multiplier partial products are generated in parallel using 16 Peres gates shown in figure. This uses 16 Peres gates for better circuit as it has less hardware complexity compared to other gates and moreover it posses parity preserving logic.

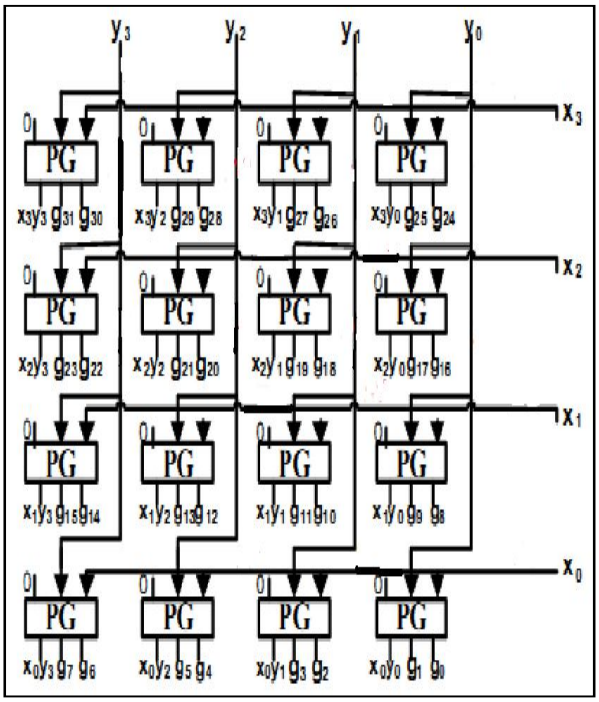

Figure 4: Partial Product Generation Using Peres Gate

3.2.Summation Network

The summation network needs Peres gate as a full adder (PFAG) and half adder. Many reversible full adders have been proposed in the past. For example TSK, MKG and HNG gates can singly perform the full adder operation Design of multipliers with these gates indicates the different critical parameters for reversible multipliers. Experimental results of different reversible multiplier circuits in terms of speed, number of garbage outputs and constant inputs show the multiplier circuits with adders designed using IG gates have better results than multiplier circuits with MKG or TSG gates.

The Peres gate used as half adder is shown in the figure 5(a). It requires two constant inputs of logic 0 and produces the required sum and carry term with one garbage output. By forcing the input C as 0 it produces the sum and carry terms in outputs Q and R. Here A is the garbage output. It can also be further extended to implement full adder circuit which requires two constant inputs of logic 0 and two garbage values is shown in figure 5(b). The full adder implementation using Peres gate is shown in figure 5(c).

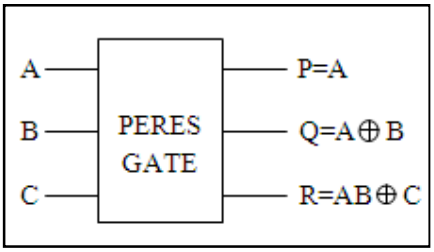

Figure 5(a) : Peres gate as a half adder

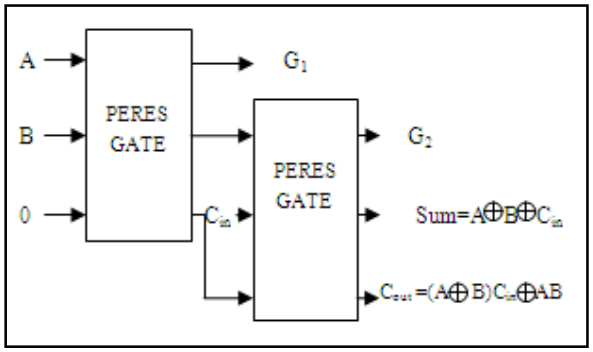

Figure 5(b): PFAG connection

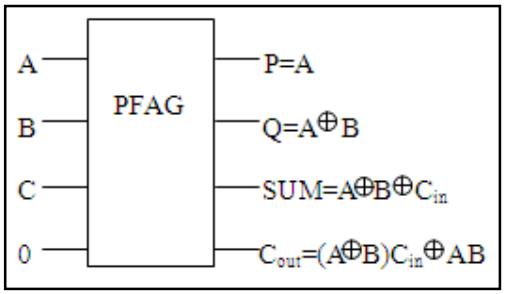

Figure 5(c): Peres gate as a Full adder

The circuit of proposed summation network is shown in the figure 6. It requires four Peres gate as half adder and eight Peres gate as full adder logic implementation. P_0 toP_7 is the product terms.

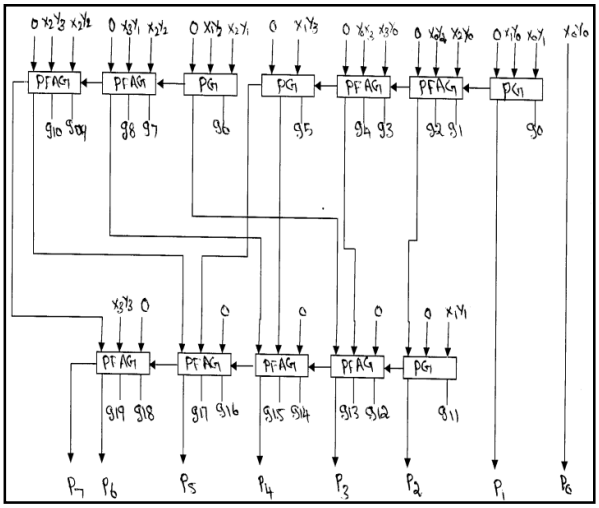

Figure 6: Summation Network

4. Result And Discussion

The architecture is modeled using VHSIC hardware description language (VHDL). The coding is done on Xilinx ISE8.2i. For simulation purpose the Modelsim 6.2h has been used. The efficiency of proposed reversible multiplier depends on the choice of reversible gate. The efficient parallel adders will significantly improve the multiplier efficiency. The proposed multiplier is efficient in terms of number of Garbage outputs. The proposed 4*4 bit reversible multiplier is designed with minimum of 19 garbage outputs while the existing multiplier has 32 garbage outputs. Because of this garbage outputs the proposed multiplier will lead to a great reduction in power consumption. The

simulation result for proposed multiplier is shown in figure 7 and the comparison table is also given in table1.

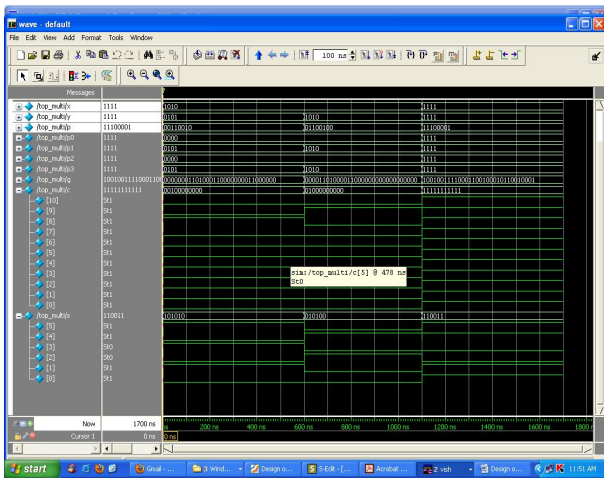

Figure 7: Simulation output of Proposed Multiplier

Paper	Garbage output	Constant input	Number of Gates	Power
Fault tolerant multiplier	64	37	36	0.160
Proposed Multiplier	52	28	28	0.057

*Table 1: Comparison of 4*4 Multiplier*

5. Conclusion

Multiplier is a basic arithmetic cell in computer arithmetic units. The energy consumption in computation turns out to be deeply linked to the reversibility of the computation. The focus of this paper is to reduce the number of garbage output. The reduction of garbage output reduces the power consumption. It is proved that the proposed multiplier architecture using the Peres gate is better than the existing multiplier. In the proposed multiplier we synthesized a parity preserving reversible multiplier circuit with the help of Peres gate. This circuit can be also helpful for high speed multiplier for dedicated hardware. The prospect for further research includes the reversible implementation of more complex arithmetic circuits such as function evaluation and multiplicative division circuits using this multiplier.

6.Reference

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