INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN: 2278 – 0211 (Online)

Network Failure Identification System

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Abstract:
In this paper, a remedy to reduce the man power when there is failure in the network is presented. Communication (network) faults can cause delays or even shutdown of the entire manufacturing process. The current process of detecting and diagnosing communication faults is mostly manual, cumbersome, and inefficient. Detecting early symptoms of potential problems is very important but automated solutions do not yet exist. Our research goal is to automate the process of detecting and diagnosing the communication faults as well as to prevent problems by detecting early symptoms of potential problems. To achieve our goal, we have first investigated real-world fault cases and summarized control network failures and also defined alarm conditions to detect early symptoms. Researchers have approached this problem using various techniques such as artificial intelligence, machine learning, and state machine modelling. But we are using processing technique based on abrupt change detection. The application of processing techniques to this area is still in its infancy, and we believe that it has great potential to enhance the field, and thereby improve the reliability of IP networks.

Key words*: Sensors, GSM, GPS, Buzzer*

1.Introduction

NETWORKS are complex interacting systems and are comprised of several individual entities such as routers and switches. The behavior of the individual entities contributes to the ensemble behaviour of the network. The evolving nature of internet protocol (IP) networks makes it difficult to fully un- derstand the dynamics of the system. Internet traffic was first shown to be composed of complex self-similar patterns by Le-land et al. Multiracial scaling was discovered and reported by Levy-Vehel et al. To obtain a basic understanding of the performance and behavior of these complex networks, vast amounts of information need to be collected and processed. Often, network performance information is not directly avail-able, and the information obtained must be synthesized to obtain an understanding of the ensemble behavior. In this paper, we review the us processing techniques to address the problem of measuring, analyzing, and synthesizing network information to obtain normal network behavior. The normal net-work behavior thus computed is then used to detect network anomalies. There are two main approaches to studying or characterizing the ensemble behaviour of the network: The first is the inference of the overall network behaviour through the use of network probes and the second by understanding the behaviour of the individual entities or nodes. In the first approach, which is often referred to as network tomography, there is no assumption made about the network, and through the use of probe measurements, one can infer the characteristics of the network. This is a useful approach when characterizing non cooperative networks or networks that are not under direct administrative control. In the case of a single administrative domain where knowledge of the basic network characteristics such as topology is available, an entity-based study would provide more useful information to the network administrator. Using some basic knowledge of the network layout as well as the traffic characteristics at the individual nodes, it is possible to detect network anomalies and performance bottlenecks. The detection of these events can then be used to trigger alarms to the network management system, which, in turn, trigger recovery mechanisms. The methods presented in this paper deal with entity-based measurements.

2.System Architecture

The main server is maintained at main office, from there the wired connections are given to various departments and this continues. By this, link is established between the departments based on different IP addresses. The main purpose of paper is to find the

exact location of errors where the failure happened. Here main Microcontroller sends data to sub microcontrollers and from sub microcontroller to client servers through wire connections. If any wire breakage occurs in this process, that wire connected to particular microcontroller's port gets information and that information is send to its main microcontroller and particular IP address is displayed in LCD. LED's are used for an indication. Red color indicates the normal functionality; if it stops blinking it indicates failure.

When the network gets failed due to breakage of wire, technicians checks the connections right from beginning of the source. This is a time taking task and the work gets delayed and employees are required in more number. In order to overcome the above mentioned disadvantages we proposed this paper.

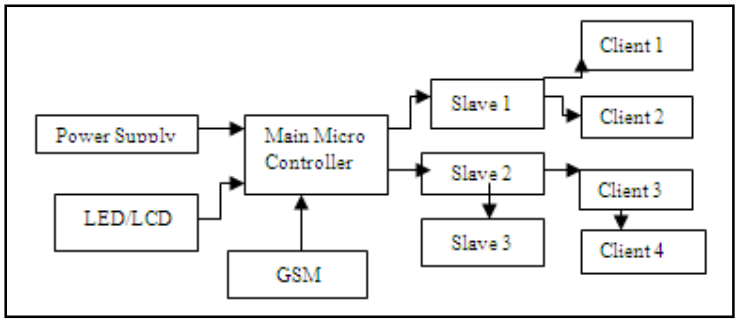


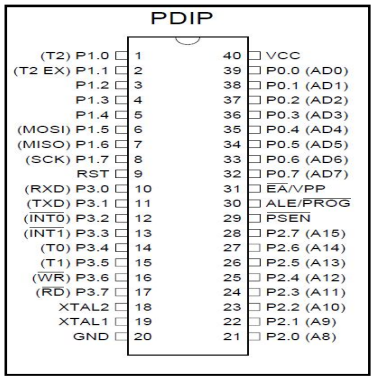
Figure 1: Block Diagram

3.Hardware Design

3.1.Microcontroller(AT89S52)

Microprocessors and microcontrollers are widely used in embedded systems products. Microcontroller is a programmable device. A microcontroller has a CPU in addition to a fixed amount of RAM, ROM, I/O ports and a timer embedded all on a single chip. The fixed amount of on-chip ROM, RAM and number of I/O ports in microcontrollers makes them ideal for many applications in which cost and space are critical. 8052 is an 8-bit processor, meaning that the CPU can work on only 8 bits of data at a time. Data larger than 8 bits has to be broken into 8-bit pieces to be processed by the CPU. 8052 is available in different memory types such as UV-EPROM, Flash and NV-RAM.The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller with 8K bytes of in-system programmable Flash memory. The device is manufactured using Atmel's

high-density non volatile memory technology and is compatible with the industry-standard 80C51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non volatile memory programmer. By combining a versatile 8-bit CPU with in-system programmable Flash on a monolithic chip, the Atmel AT89S52 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications. The AT89S52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.The pin description is discussed in the following section.



Figuer 2

3.2.LED/LCD

LCD stands for Liquid Crystal Display. An image in an LCD is formed by applying an electric field to alter the chemical properties of each LCC (Liquid Crystal Cell) in the display in order to change a pixel's light absorption properties. These LCC's modify the image produced by the backlight into the screen output requested by the controller. Through the end output may be in color, the LCC's are monochrome, and the color is added later through a filtering process. Modern laptop computer displays can produce 65,536 simultaneous colors at resolution of 800 X 600.

3.3.Message Transmission Module GSM

Global system for mobile communication (GSM) is a globally accepted standard for digital cellular communication. GSM is the name of a standardization group established in 1982 to create a common European mobile telephone standard that would formulate specifications for a pan-European mobile cellular radio system operating at 900 MHz frequency. Cellular is one of the fastest growing and most demanding telecommunications applications. GSM (Global System for Mobile communication) is a digital mobile telephony system that is widely used in Europe and other parts of the world. GSM uses a variation of time division multiple access (TDMA) and is the most widely used of the three digital wireless telephony technologies (TDMA, GSM, and CDMA). GSM digitizes and compresses data, then sends it down a channel with two other streams of user data, each in its own time slot. It operates at either the 900 MHz or 1800 MHz frequency band.

The structure of a GSM network:

- The network is structured into a number of discrete sections:
- The Base Station Subsystem (the base stations and their controllers).
- The Network and Switching Subsystem (the part of the network most similar to a fixed network). This is sometimes also just called the core network.
- The GPRS Core Network (the optional part which allows packet based Internet connections).
- The Operations support system (OSS) for maintenance of the network.

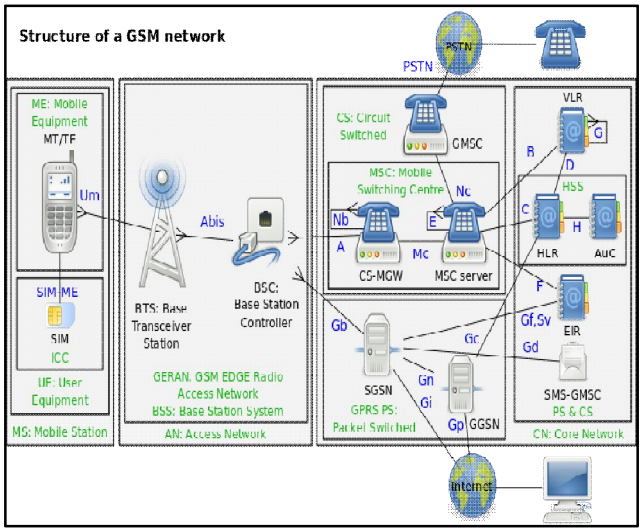


Figure 3

4.Schematic Diagram

4.1.Power Supply

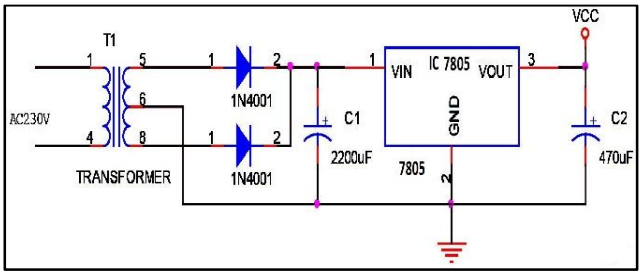


Figure 4

The input to the circuit is applied from the regulated power supply. The ac input i.e., 230V from the mains supply is step down by the transformer to 12V and is fed to a rectifier. The output obtained from the rectifier is a pulsating d.c voltage. So in order to get a pure dc voltage, the output voltage from the rectifier is fed to a filter to remove any ac components present even after rectification. Now, this voltage is given to a voltage regulator to obtain a pure constant dc voltage

4.2.Complete Schematic

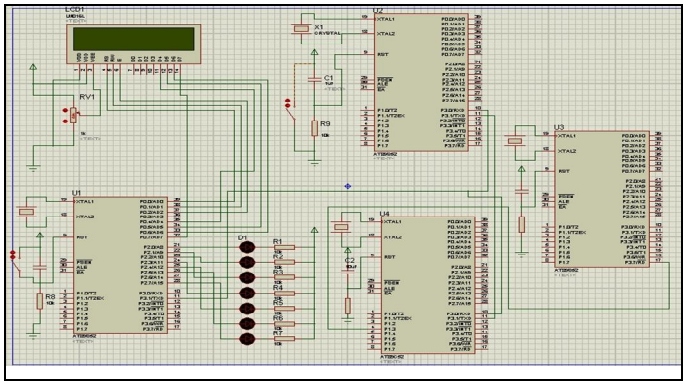


Figure 5

5.Conclusion

Here two technologies are used, at first microcontroller sensing technology is used to sense or detect the failure and information is transferred to microcontroller in engine. Then GSM technology is used to transmit information about failure to concerned authorities and emergency services.

6.Reference

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