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Design and Synthesis of Sequential Circuit Using Reversible Logic

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Abstract:

The reversible logic will be having more importance in today's era due to its low power consumption. It will be having more applications in quantum computing and low power VLSI design. This paper proposes the different reversible sequential circuits. Proposed circuits are simulated using Xilinx ISim simulator and implemented on Xilinx FPGA platform.

Key words: *Reversible Logic, Reversible Logic Gates, D-Latch, T-FlipFLop, Asynchronous Up/Down Counter.*

1.Introduction

According to R. Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where $K=1.3806505*10^{-23}m^2kg^{-2}K^{-1}$ (joule/Kelvin^{-1}) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

2.Reversible Logic

A reversible logic gate will be having n-input n-output with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely retrieved from the outputs. In the synthesis of reversible circuits direct fan-Out is not. In reversible logic gates feedback paths are not allowed. However fan-out in reversible circuits is achieved using additional gates. Optimized or efficient reversible logic circuits will be minimum number of reversible gates, garbage outputs, constant inputs and minimum quantum cost. There are several basic reversible logic gates are available in the literature. In the below section we discuss some basic reversible logic gates that are used for our proposed work

3.Basic Reversible Logic Gates

3.1.Feynman Gate (FG)

Feynman gate [3] is a 2*2 reversible gate is shown in Figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A □ B. Quantum cost of a Feynman gate is l.

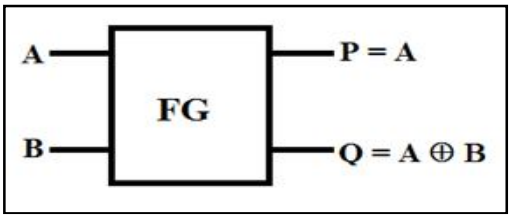

Figure 1: Feynman Gate (FG)

3.2.Fredkin Gate (FRG)

Fredkin Gate (FRG) [3] is a 3*3 reversible gate is shown in Figure 2. The input vector is I (A, B, C) and the output vector is O(P, Q, R). The output is defined by P=A, Q=A'B□AC and R=A'C□AB. Quantum cost of a Fredkin gate is 5.

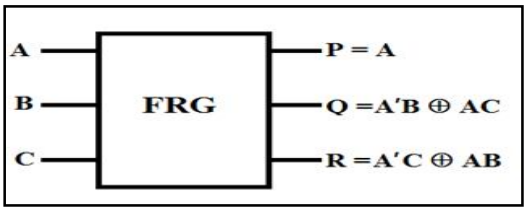

Figure 2: Fredkin Gate (FRG)

3.3.Sayem Gate (SG)

Sayem gate (SG) [4] is a 4x4 reversible gate is shown in Figure 3. The input vector is I (A, B, C, D) and the output vector is O(P, Q, R, S). The output vector is defined by P = A, Q = A'B □ AC, R = A'B □ AC □ D, S = AB □ A'C □ D. Quantum cost of a Sayem gate is 6.

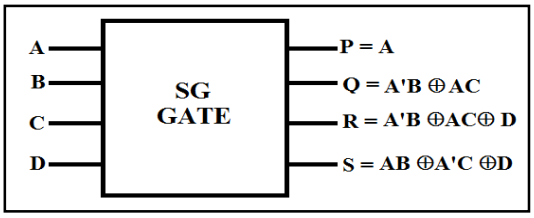

Figure 3: Sayem Gate (SG)

4.Proposed Work

4.1.D-Latch

The D flip-flop [5] is a circuit that needs only a single input and clock pulses. The action of the D flip-flop is straightforward. The Figure 4 shows the proposed reversible D-Latch.

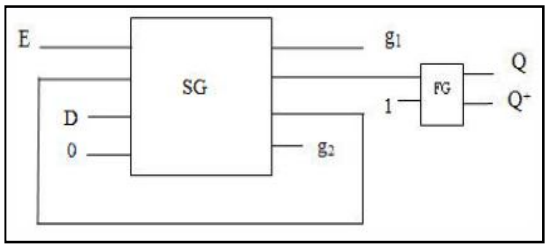

Figure 4: Proposed D-Latch

4.2.T-FlipFlop

As the name suggests, T flip-flop [6] circuit used to toggle the output when input is high (1) and retains the output when input is low (0), thus it does two operation, it either holds the last state or toggles the output. Essentially, it has a logical symmetry with controlled NOT kind operation. Table I shows the truth table of T-FlipFlop. Figure 5 shows proposed reversible T-FlipFlop.

T	**Q_{T+1}**
0	Qt
1	$\overline{Qt}$

Table 1: Truth Table of T-FlipFlop

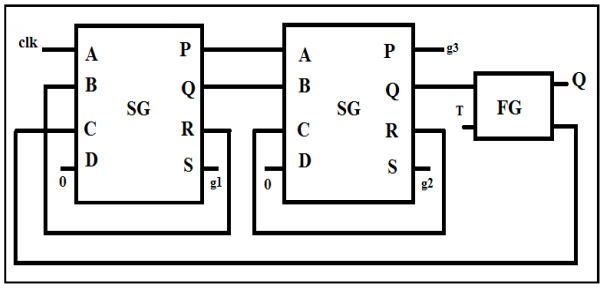

Figure 5: Proposed T-FlipFlop

4.3.Asynchronous Up/Down Counter

The implementation of 4-bit reversible asynchronous Up/Down Counter is shown in Figure 6 [6]. The Up/Down operation of this reversible circuits is controlled by the control input UP/DOWN. For UP operation, the control input should be 1 and for down operation, the control input should be 0.

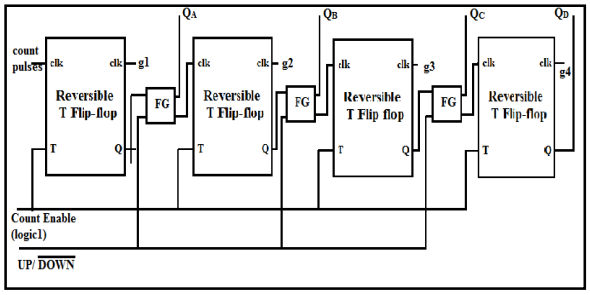

Figure 6: Proposed 4-Bit Asynchronous Up/Down Counter

5.Simulation Results

The entire architecture is modeled using VHSIC hardware description language (VHDL). The coding is done on Xilinx ISE13.2 on Spartan 3 using target device: XC3S50-PQ208 at speed grade of -5. For simulation purpose the Xilinx ISim simulator has been used. The simulation result for D-Latch is shown on Figure 7 for T-FlipFlop is shown on Figure 8 and for 4-Bit Asynchronous Down counter is shown on Figure 9.

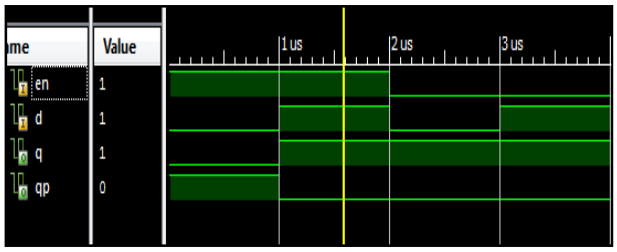

Figure 7: Simulation result of proposed reversible D-Latch

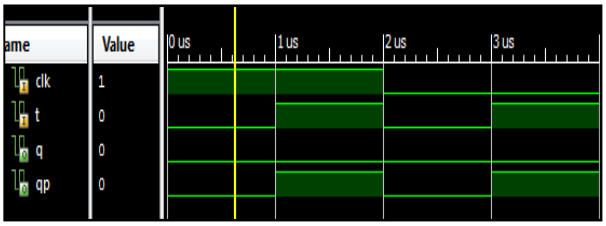

Figure 8: Simulation result of proposed reversible T-Latch

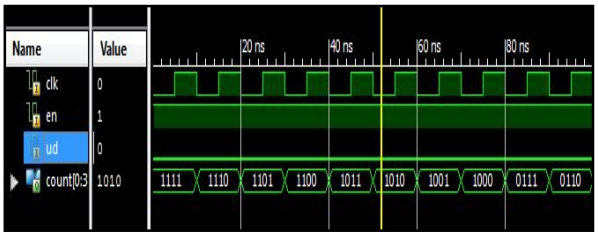

Figure 9: Simulation result of proposed reversible 4-bit asynchronous down counter

TABLE II, TABLE III and TABLE IV shows comparative experimental results of Different Reversible D-Latch, T-FlipFlop and 4-Bit Asynchronous Up/Down Counter.

	No. Of gates	**No. of Constant Inputs**	**No. of Garbage Bits**	**Quantum Cost**
Existing Work [6]	2	2	2	7
This Study	2	2	2	7

Table 2: Comparative Experimental Results of Different Reversible D-Latch

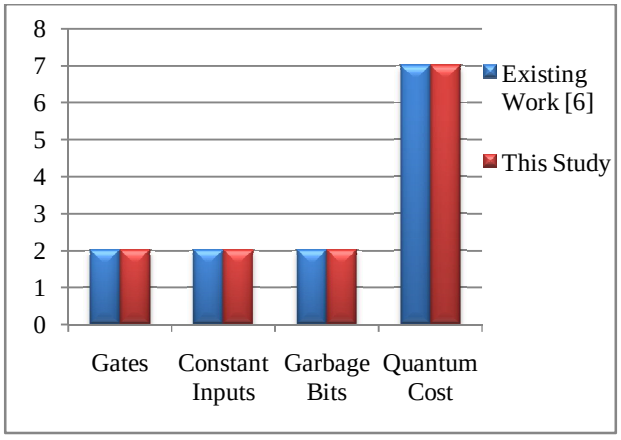

Figure 10: Graphical representation of comparison of two design works of Reversible D-Latch

	No. Of gates	**No. of Constant Inputs**	**No. of Garbage Bits**	**Quantum Cost**
Existing Work [6]	5	2	3	13
This Study	3	2	3	13

Table 3: Comparative Experimental Results of Different Reversible T-FlipFlop

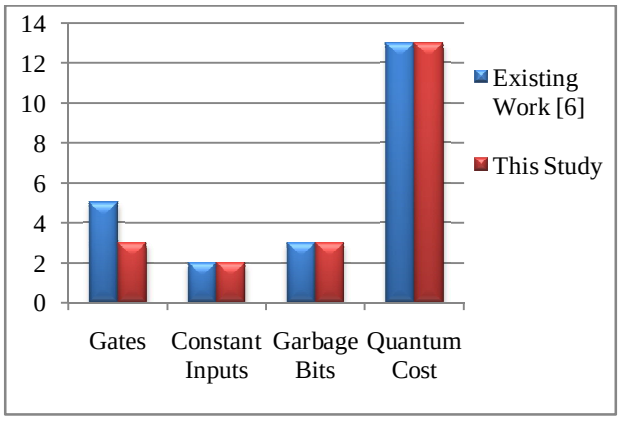

Figure 11: Graphical representation of comparison of two design works of Reversible T-FlipFlop

	No. Of gates	**No. of Constant Inputs**	**No. of Garbage Bits**	**Quantum Cost**
Existing Work [6]	23	8	12	55
This Study	15	8	12	55

Table 4: Comparative Experimental Results Of Different Reversible 4-Bit Asynchronous Up/Down Counter

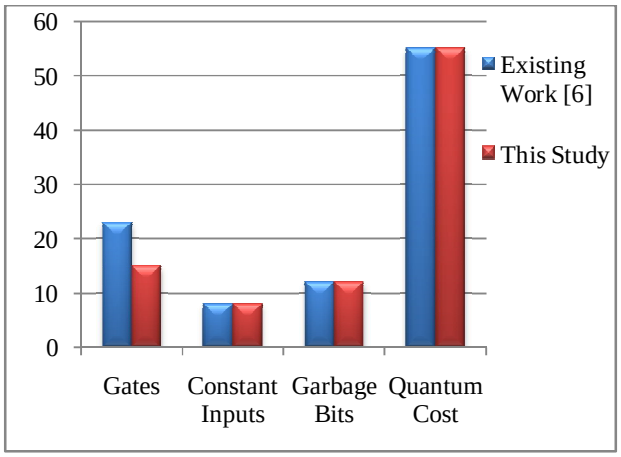

Figure 12: Graphical representation of comparison of two design works of Reversible 4-Bit Asynchronous Up/Down Counter

6.Conclusion

This paper proposes designs of basic reversible sequential elements such as latches, flip-flops and four bit reversible asynchronous up/down counter. We have shown average

power dissipation in each gate in simulation part which indicates negligible energy dissipation which in turn improves performance of circuit. Basic reversible gate presented in this paper can be used in regular circuits realizing Boolean functions. The proposed asynchronous counter designs have the applications in building reversible ALU, reversible processor etc. In this paper, we present a method of asynchronous counter design directly from reversible gates. This work forms an important move in building large and complex reversible sequential circuits.

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