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Analysis of 15 Level Inverter Using Hybrid PWM Strategy

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Abstract:
This paper represents a new topology 15 level asymmetric multilevel inverter with HYBRID PWM strategy. Multilevel inverter is triggered using hybrid PWM strategy. It includes Phase Disposition (PD) strategy, Alternate Phase Opposition Disposition (APOD) strategy and Carrier Overlapping (CO) strategy. The performance measures like Total Harmonic Distortion (THD), V_{RMS} (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK.

Key words: *APOD, CO, PD, PWM*

1. Introduction

Multilevel inverters are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high power applications. Multilevel inverters have lower harmonic spectra and lower device voltage stresses; so they are particularly suitable for high voltage and high power applications. Zambra et al [1] discussed comparison of neutral-point-clamped, symmetrical, and hybrid asymmetrical multilevel inverters. Taghizadeh and Tarafdar Hagh [2] proposed harmonic elimination of cascade multilevel inverters with nonequal DC sources using particle swarm optimization. Sivakumar [3] introduced a hybrid multilevel inverter topology for an open-end winding induction-motor drive using two-level inverters in series with a capacitor-fed H-bridge cell. Ewanchuk et al [4] introduced a five / nine-level twelve-switch neutral-point-clamped inverter for high-speed electric drives. Zhang and Sun [5] analysed an efficient control strategy for a five-level inverter comprising flying-capacitor asymmetric H-bridge. Pereda and Dixon [6] developed high-frequency link a solution for using only one DC source in asymmetric cascaded multilevel inverters .Ghazanfari et al [7] proposed simple voltage balancing approach for CHB multilevel inverter considering low harmonic content based on a hybrid optimal modulation strategy. Wang et al [8] developed an improved pulse width modulation method for chopper-cell-based modular multilevel converters. Faith et al [9] introduced THD minimization applied directly on the line-to-line voltage of multilevel inverters. Rathore et al [10] proposed generalized optimal pulse width modulation of multilevel inverters for low-switching-frequency control of medium-voltage high-power industrial AC drives. This paper presents a single phase binary DC source 15 level inverter topology for investigation with various HYBRID PWM switching strategies. Simulations were performed using MATLAB-SIMULINK.

2. Proposed Asymmetrical Multilevel Inverter

Asymmetric multi-level inverter looks like a conventional cascaded H-bridge multilevel inverter except input DC sources. The properties of asymmetric multi-level inverters are however quite different from those of symmetrical multilevel inverter. Especially the number of output-voltage levels can be dramatically increased. Instead of increasing the number of modules, one can also choose to reduce the number of cells. The advantages of asymmetric topology are:

- Reduced number of DC sources
- Low output switching frequency
- Low switching losses
- High conversion efficiency
- Flexibility to enhance output levels
- Reduction in circuit complexity and cost

The proposed new asymmetric cascaded multilevel inverter is shown in Figure 1. This inverter consists of a three conversion cell and a H bridge. Conversion cell consist of separate voltage sources (V1, V2, V3) connected in cascade and two active switching elements that can make the output voltage in only positive polarity with several levels. H-bridge consists of four active switching elements that can make the output voltage in positive or in negative polarity depending on the switching condition. Table 1 show the switching sequence of proposed inverter. By using Vdc,2Vdcand 4Vdc, it can synthesize 15 output levels;-7Vdc,-6Vdc,-5Vdc, -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc,5Vdc,6Vdc,7Vdc. Expected output voltage level is given by

$Vn=2^{n+1}-1$, where n=1, 2, 4…….

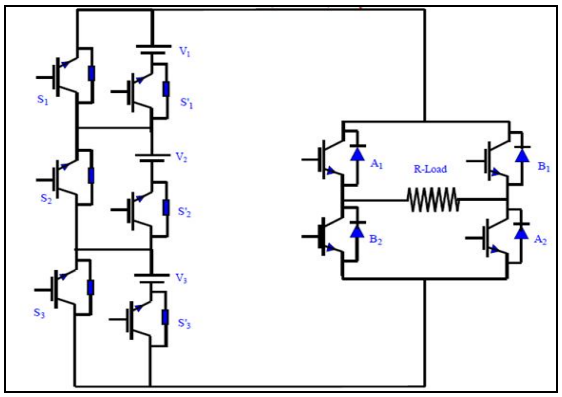

Figure 1: Proposed Multilevel Inverter

S_1	S_2	S_3	S_1'	S_2'	S_3'	A_1	A_2	B_1	B_2	Level
1	1	1	0	0	0	1	1	0	0	7
0	1	1	1	0	0	1	1	0	0	6
1	0	1	0	1	0	1	1	0	0	5
0	0	1	1	1	0	1	1	0	0	4
1	1	0	0	0	1	1	1	0	0	3
0	1	0	1	0	1	1	1	0	0	2
1	0	0	0	1	1	1	1	0	0	1
0	0	0	1	1	1	0	0	1	1	0
1	1	1	0	0	0	0	0	1	1	-7
0	1	1	1	0	0	0	0	1	1	-6
1	0	1	0	1	0	0	0	1	1	-5
0	0	1	1	1	0	0	0	1	1	-4
1	1	0	0	0	1	0	0	1	1	-3
0	1	0	1	0	1	0	0	1	1	-2
1	0	0	0	1	1	0	0	1	1	-1

Table 1: Switching Table for Proposed Inverter

3. Multi Carrier Based PWM Methods

In this proposed work Hybrid PWM strategy used to generate firing pulses for a 15 level inverter. For an m-level inverter using Unipolar multi-carrier Strategies, (m-1)/2 carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the device switches off. There are many alternative strategies are possible, some of them are tried in this paper and they are:

a. Unipolar Phase disposition PWM strategy (UPDPWM).

b. Unipolar Alternate phase opposition disposition PWM strategy (UAPODPWM).

c**.** Unipolar Carrier overlapping PWM strategy (UCOPWM).

The formulae to find the Amplitude of modulation indices are as follows:

For PDPWM and APODPWM

$$m_a = 2A_m/(m-1)A_c)$$

For COPWM:

$$m_a = A_m/(2*A_c)$$

3.1. Unipolar Phase disposition PWM strategy.

In case of UPDPWM strategy, all the carrier waveforms are in phase. The carrier arrangement of hybrid PWM reference is illustrated in figures 2.

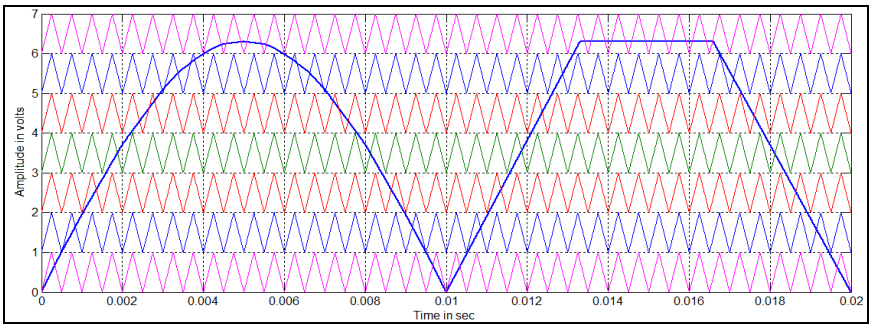

Figure 2: Carrier arrangements for UPDPWM strategy with hybrid PWM strategy (m_a = 0.9 and m_f = 40)

3.2. Unipolar Alternate phase opposition disposition PWM strategy

In case of UAPODPWM, every carrier waveform is in out of phase with its neighboring carrier by 180°. The carrier arrangements of hybrid PWM reference are illustrated in figures 3.

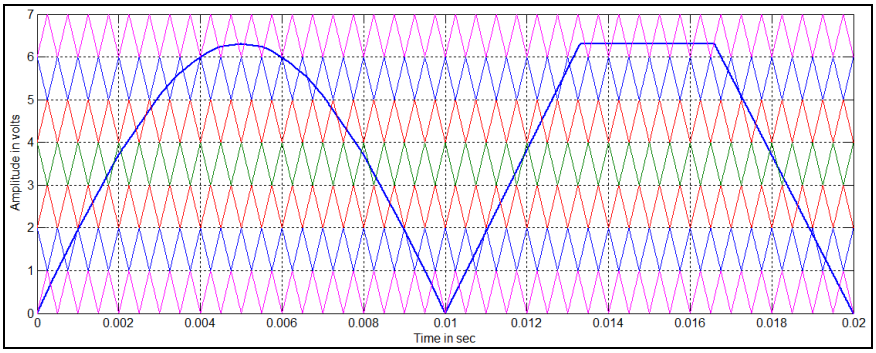

Figure 3: Carrier arrangements for UAPODPWM strategy with hybrid PWM strategy (m_a = 0.9 and m_f = 40)

3.3. Unipolar Carrier overlapping PWM strategy

In carrier overlapping technique, (m-1)/2 carriers are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is Ac/2. The carrier arrangements of hybrid PWM reference are illustrated in figures 4.

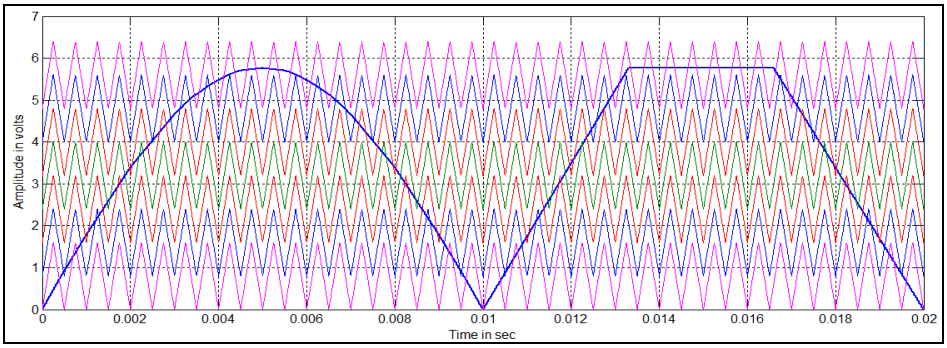

Figure 4: Carrier arrangements for UCOPWM strategy with hybrid PWM strategy (m_a = 0.9 and m_f = 40)

4. Simulation Result

The single phase binary DC source 15 level inverter is modeled in SIMULINK using power system block set. Switching signals for binary multilevel inverter using USPWM strategies are simulated.Fig.5 (a) and (b) respectively shows the 15 level output voltage generated by UPDPWM strategies with hybrid strategy and its FFT plot. Fig .6 (a) and (b) respectively shows the 15 level output voltage generated by UAPODPWM strategies with hybrid strategy and its FFT plot .7 (a) and (b) respectively shows the 15 level output voltage generated by UCOPWM strategies with hybrid strategy and its FFT plot. Simulations were performed for different values of m_a ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table II. Table III represents the V_{RMS} of the inverter output voltage. Table IV represents the crest factor of the output voltage. Table V and VI represents the form factor and distortion factor of the output voltage. For ma= 0.9, it is observed from the figures [5b 6b 7b] harmonic energy is dominant in:5b) 5^{th},6^{th},39^{th} order in UPDPWM strategy with hybrid PWM reference and triangular carrier. 6b) 21^{st},23^{rd} order in UAPODPWM strategy with hybrid PWM reference and triangular carrier.7b) 3^{rd},4^{th},5^{th},6^{th},37^{th} ,38^{th}, order in UCOPWM strategy with hybrid PWM reference and triangular carrier The following parameter values are used for simulation: V_{dc} =21.5V, R (load) = 100 ohms, f_c=2000 Hz and f_m=50Hz.

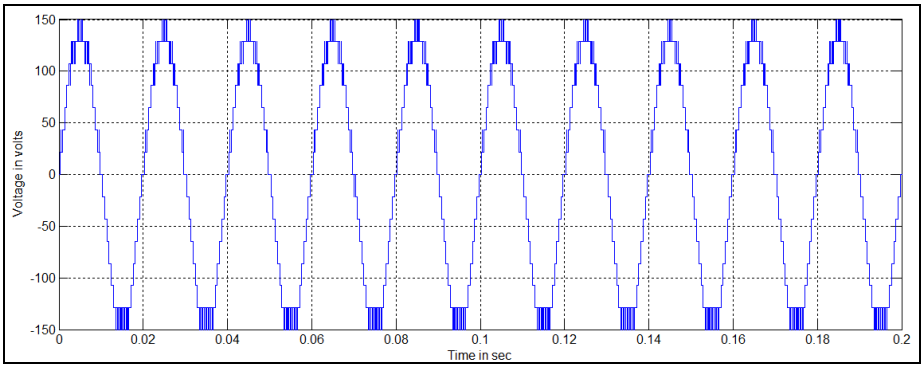

Figure 5(a): Output voltage generated by UPDPWM strategy with hybrid PWM strategy

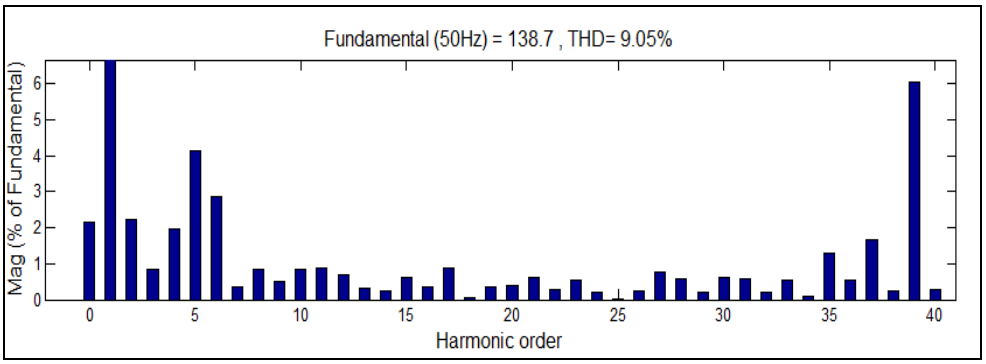

Figure 5(b): FFT plot for output voltage of UPDPWM strategy with hybrid PWM strategy

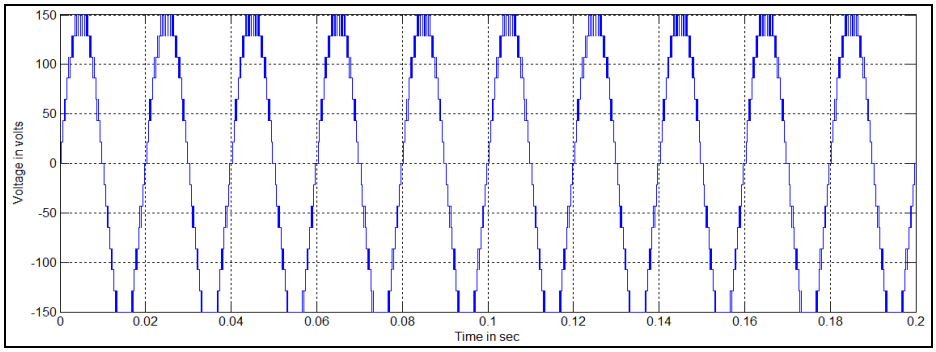

Figure 6 (a): Output voltage generated by UAPODPWM strategy with hybrid PWM strategy

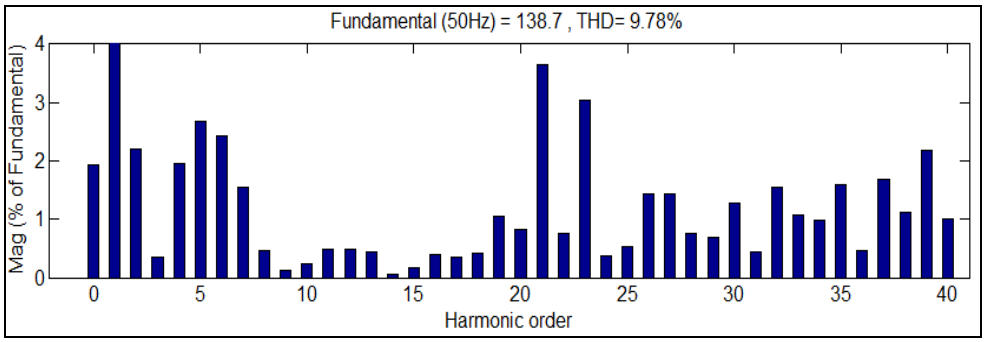

Figure 6 (b): FFT plot for output voltage of UAPODPWM strategy with hybrid PWM strategy

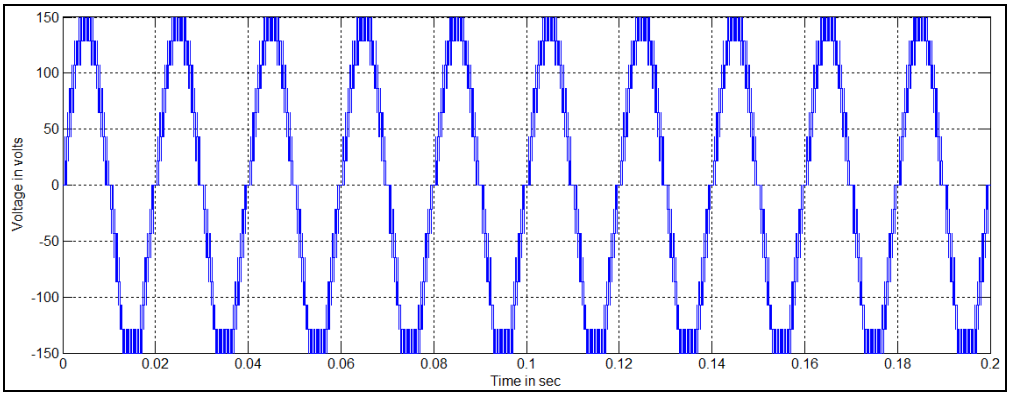

Figure 7(a): Output voltage generated by UCOPWM strategy with hybrid PWM strategy

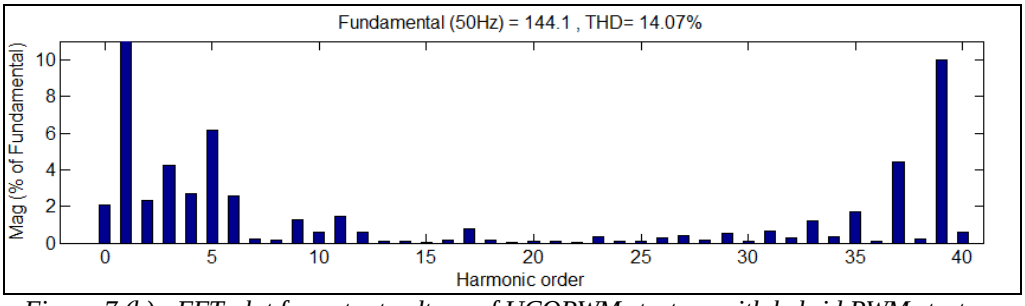

Figure 7 (b): FFT plot for output voltage of UCOPWM strategy with hybrid PWM strategy

ma	UPDPWM	UAPODPWM	UCOPWM
1	9.09	8.22	11.21
0.95	9.15	9.05	12.71
0.9	9.05	8.22	14.07

Table 2: %THD for Different Modulation Indices

ma	UPDPWM	UAPODPWM	UCOPWM
1	108.6	109.1	110.9
0.95	102.8	103.6	106.6
0.9	98.08	109.1	101.9

Table 3: V_{RMS} for Different Modulation Indices

m_a	UPDPWM	UAPODPWM	UCOPWM
1	1.414365	1.414299	1.413886
0.95	1.414397	1.414093	1.414634
0.9	1.414152	1.414299	1.414132

Table 4: CF for Different Modulation Indices

m_a	UPDPWM	UAPODPWM	UCOPWM
1	52.641784	48.85039	73.7857762
0.95	61.741742	49.807692	60.602615
0.9	45.47056	48.85804	48.75598

Table 5: Form Factor for Different Modulation Indices

m_a	UPDPWM	UAPODPWM	UCOPWM
1	0.004810873	0.004247	0.003539
0.95	0.004613946	0.004255	0.004121
0.9	0.004409454	0.004247	0.005562

Table 6: Distortion Factor for Different Modulation Indices

5. Conclusion

In this paper, HYBRID strategy for binary DC source 15 level inverter has been presented. Binary DC source multilevel inverter gives higher output voltage with reduced switch count and low harmonics. Performance factors like % THD, VRMS, CF, FF and DF have been evaluated presented and analyzed. It is found that the UAPODPWM strategy with hybrid PWM strategy provides relatively lower %THD, UCOPWM strategy with hybrid PWM strategy is found to perform relatively higher fundamental RMS output voltage. CF is almost same for all the strategies. FF is almost same for all the strategies. DF relatively low in UCOPWM strategy with hybrid PWM strategy.

6. References

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