Grid Connected Boost-Full-Bridge Photovoltaic Microinverter System Using Phase Opposition Disposition Technique and Maximum Power Point Tracking

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Abstract:
This paper presents a novel grid-connected boost-full-bridge photovoltaic (PV) micro-inverter system and its control implementations. The concept of micro-inverter is a future trend for grid connected Photovoltaic micro-inverter. Increasing demand on the renewable energy sources has made the grid connected inverter systems to be more important than ever before. Maximum Power Point Tracking (MPPT) technique is implemented which is used by the grid connected inverters to get the maximum power from one or more photovoltaic device, typically solar panels. The Z source network is used to get the steady state. Interleaving of the Boost DC-DC converter is carried out to get more boosts up the voltage and better efficiency. A new multilevel inverter topology constituting of an H-bridge structure with four switches connected to the DC link. Based on Phase Opposition Disposition technique a new PWM method requires only one carrier signal is suggested.

Key words: Boost-Full-Bridge, Grid-connected photovoltaic (PV) system, Incremental Conductance (IncCond), Maximum Power Point Tracking (MPPT), Photovoltaic micro-inverter, Phase Opposition Disposition technique (POD)

1. Introduction

Hybrid renewable energy systems are becoming popular in remote area power generation applications. Due to advances in renewable energy technologies and subsequent rise in processing of petroleum products it has become more and more popular. Photovoltaic array coupled with a wind turbine would create more output from the wind turbine during winter. During summer the solar panels will produce the peak output. Hybrid energy systems yield greater economic and environmental returns than wind.

A photovoltaic microinverter converts direct current (DC) from solar panel to alternating current (AC). The main advantage of the proposed multilevel inverter is a small amount of shading, debris or snow lines on any one solar panel, complete failure in the panel does not disproportionately reduce the output of the entire array. Each microinverter harvests optimum power by performing Maximum Power Point Tracking. Several MLI topologies have been suggested. so far and they can be mainly classified as three types as shown in Figure 1.
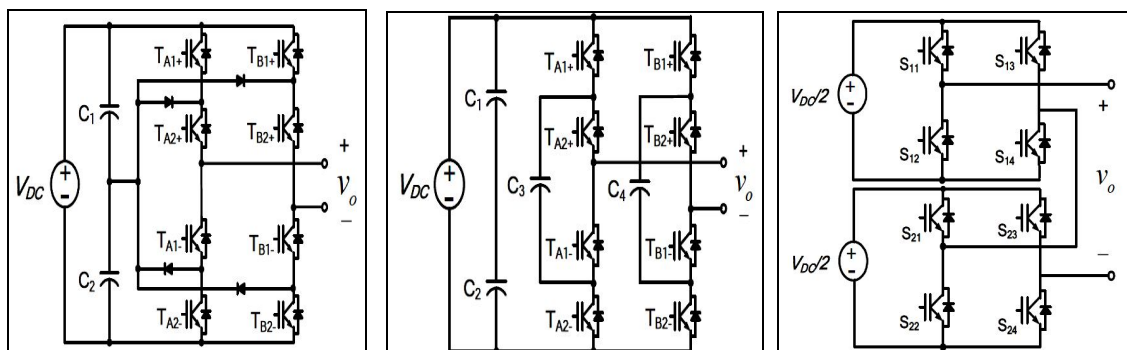

Figure 1: Topologies Of Multi Level Inverter (A) Neutral Point Clamped (NPC) (B) Flying Capacitor (C) Cascade Type

In this paper a circuit based on a H-bridge topology with four switches connected to the dc-link is proposed as an MLI topology. Also, it is simple, because the proposed PWM method uses one carrier signal for generating PWM signals. In addition a switching sequence considering the voltage balance of dc-link was proposed. Finally, the proposed topology of the multi-level inverter is verified through the simulation and the experiment.

2. Maximum Power Point Tracking
Maximum Power Point Tracking is a technique that grid connected inverters, solar battery chargers and similar devices use to get the maximum possible power from one or more photovoltaic device, typically solar panels. It is one of the key functions that every grid-connected PV inverter should have. There is a large amount of publications that deals with MPPT, and trackers in the majority of the commercial PV inverters are able to extract around 99% of the available power from the PV plant over a wide irradiance and temperature range, at least in steady state.

2.1. Incremental Conductance Method
Incremental conductance (IncCond) maximum power point tracking (MPPT) is proposed in this paper. Simulation and hardware implementation of incremental conductance used in solar array power systems with direct control method are presented. This system is capable of tracking maximum power more accurately and rapidly without steady state oscillation and also its dynamic performance is satisfactory. The IncCond algorithm is used to track MPPs because it performs precise control under rapidly changing atmospheric conditions. The IncCond method is the one which overrides over the drawback of the neutral network that comes with the reliance on the characteristics of the PV array that changes with time, implying that the neutral network has to be periodically trained to guarantee accurate MPPs. IncCond method tracks the true MPPs independent of PV array characteristics. IncCond method with boost converter is described as the best MPPT method. The efficiency of this method results up to 95%.

2.2. Direct Control Methods
There are two independent control loops in MPPT. First control loop contains the MPPT algorithm, and the second one is usually a proportional (P) or P-integral (PI) controller. The IncCond method uses instantaneous and IncCond to generate an error signal, which is zero at the MPP; however, it is not zero at most of the operating points. The main purpose of the second control loop is to make the error from MPPs near to zero. In this paper, the IncCond method with direct control is selected. The flow chart of a direct control method is as shown in Figure 2. The PI control loop is eliminated, and he duty cycle is adjusted directly in the algorithm. The control loop is simplified, and the computational time for tuning controller gains is eliminated. To compensate the lack of the PI controller in the proposed system, a small marginal error of 0.002 was allowed.
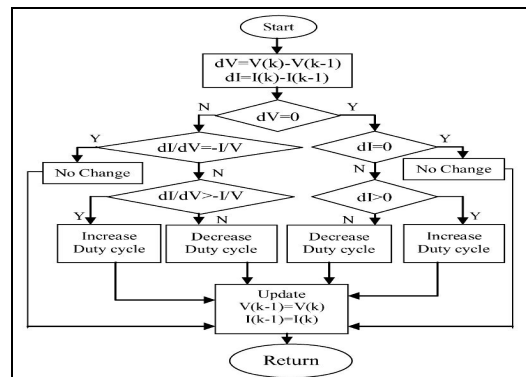

Figure 2: Direct Method in Incremental Conductance

3. Z Source Network
For the traditional V-source inverter, the dc capacitor is the sole for energy storage and filtering element to suppress voltage ripple and serve temporary storage. For traditional I-source inverter, the dc inductor is the sole energy storage/filtering element to suppress current ripple and serve temporary storage. The Z-source network is a combination of two inductors and two capacitors. This combined circuit, the Z-source network is the energy storage/filtering element for the Z-source inverter. The Z-source network provides a second-order filter and is more effective to suppress voltage and current ripples than capacitor or inductor used alone in the traditional inverters. Therefore, the inductor and capacitor requirement should be smaller than the traditional inverters. When the two inductors (L_1 and L_2) are small and approach zero, the Z-source network reduces to two capacitors (C_1 and C_2) in parallel and becomes a traditional V-source. Therefore, a traditional V-source inverters capacitor requirements and physical size is the worst case requirement for the Z-source network. Considering additional filtering and energy storage provided by the inductors, the Z-source network should require less capacitance and smaller size compared with the traditional V-source inverter. Similarly, when the two capacitors (C_1 and C_2) are small and approach zero, the Z-source network reduces to two inductors (L_1 and L_2) in series and becomes a traditional I-source. Therefore, a traditional I-source inverter's inductor requirements and physical size is the worst case requirement

for the Z-source network. Considering additional filtering and energy storage by the capacitors, the Z-source network should require less inductance and smaller size compared with the traditional I-source inverter.

4. Proposed Multi-Level Inverter

4.1. Topology of Multi-Level Inverter
The proposed multi-level inverter topology based on an H-bridge inverter with four switches connected to the dc link is as shown in Figure 3. As shown in figure the proposed MLI is composed of two dc-link capacitors (C_1, C_2) and four switching devices (T_A^+, T_A^-, T_B^+, T_B^-) comprising a H-bridge and four active switches (T_P^+, T_P^-, T_N^+, T_N^-) located between the dc-link and H-bridge. The voltage across the switching devices in the dc-link (T_P^+, T_P^-, T_N^+, T_N^-) is $V_{DC}/2$ and operated at a switching frequency. Whereas, the voltage across the switching devices in the H-bridge (T_A^+, T_A^-, T_B^+, T_B^-) is V_{DC} and the switches (T_A^+, T_A^-, T_B^+, T_B^-) are switched at a frequency of the fundamental component of the output voltage.
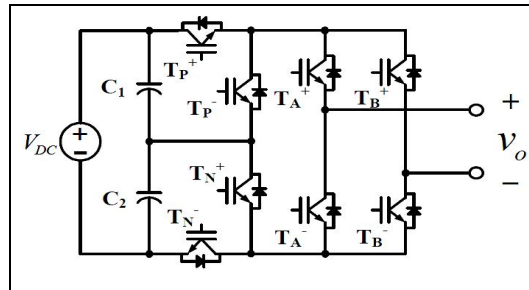

Figure 3: Proposed Single Phase Multi-Level Inverter Topology

Thus, the dc-link switches (T_P^+, T_P^-, T_N^+, T_N^-) and the H-bridge switches (T_A^+, T_A^-, T_B^+, T_B^-) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table 1 shows the output voltage according to the switching states.

Output voltage (V_o)	Switching condition					
	T_P^+,	T_P^-	T_N^+	T_N^-	T_A^+, T_B^-	T_A^-, T_B^+
V_{DC}	ON	OFF	OFF	ON	ON	OFF
$V_{DC}/2$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$-V_{DC}/2$	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

Table 1: Output Voltage According To Switching States

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_c \leq V_{ref} < 2V_c$	$V_{DC}/2$ or V_{DC}
Mode 2	$0 \leq V_{ref} < V_c$	0 or V_{DC}
Mode 3	$-V_c \leq V_{ref} < 0$	$-V_{DC}/2$ or 0
Mode 4	$-2V_c \leq V_{ref} < -V_c$	$-V_{DC}$ or $-V_{DC}/2$

Table 2: Operating Mode of the Proposed Mli

4.2. Operating Modes and Proposed PWM Strategy

The output voltage of the proposed MLI is as shown in Figure 3. It has five levels (V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, $-V_{DC}$) according to the switching states of the inverter. There are four operation modes depending on the instantaneous value of the reference voltage, V_{ref} and the maximum value of the carrier signal, V_c as shown in Figure 4. Table II shows the possible inverter output voltage level according to the operating mode. In case of the N-level NPC type multi-level inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range $+V_{DC}$ to $-V_{DC}$. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Three dispositions of the carrier signal are considered to generate the PWM signal.

- Phase Disposition (PD); where all carriers are in phase
- Alternative Phase Opposition Disposition (APOD); where each carrier is phase shifted by 180 degrees from its adjacent carrier.
- Phase Opposition Disposition (POD); Where the carriers above zero voltage are 180 degrees out of phase with those below zero voltage.

Figure 4. Shows the reference signal and the carrier signal arrangements for PD modulation, POD modulation, and APOD modulation. A new PWM strategy based on POD modulation which requires only a single carrier signal ($V_{carrier}$) is proposed and the detailed PWM strategy is depicted. If the reference signal is positive, then the switch pair (T_A^+, T_B^-) are turned on, and if it is negative, then the switch pair (T_A^-, T_B^+) are turned on. Thus the switches composing the H-bridge inverter turned on and turned off once during the period of the reference signal. The voltage across the switch at blocking state is V_{DC}. The switches (T_P^-, T_N^+) are operated complementary to the switches (T_P^+, T_N^-).

The generation of the PWM signal for dc-link switches (T_P^+, T_N^-) can be explained as follows.

- Mode 1: a signal subtracted from the reference signal by Vc is compared with the carrier signal. If $V_{ref} - V_c > V_{carrier}$, then all switches T_P^+ or T_N^- is turned on. If $V_{ref} - V_c < V_{carrier}$, then the switch T_P^+ or T_N^- is turned off alternately.
- Mode 2: The reference signal is directly compared with a carrier signal. If $V_{ref} > V_{carrier}$, then the switch T_P^+ or T_N^- is turned on alternatively. If $V_{ref} < V_{carrier}$, then all switches T_P^+ or T_N^- are turned off.
- Mode 3: $-V_{ref}$ is directly compared with a carrier signal. If $-V_{ref} > V_{carrier}$, then the switch T_P^+ or T_N^- is turned on alternatively. If $-V_{ref} < V_{carrier}$, then all switches T_P^+ or T_N^- are turned off.
- Mode 4: A signal subtracted from $-V_{ref}$ by Vc is compared with the carrier signal. If $-V_{ref} - V_c > V_{carrier}$, then all switches T_P^+ or T_N^- are turned on. If $-V_{ref} - V_c < V_{carrier}$, then the switch T_P^+ or T_N^- is turned off alternately.

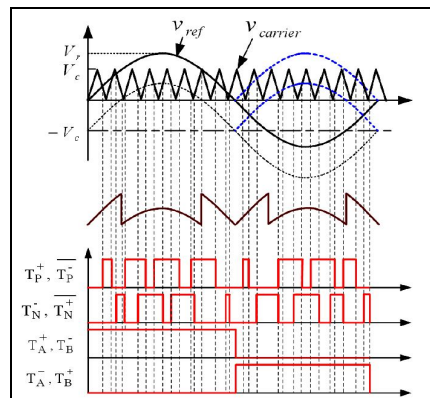Only one carrier signal is used to generate eight PWM signals in the proposed PWM method. Thus, it is quite simple.

Figure 4: PWM Strategy Based On POD with Single Carrier Signal

5. Full Bridge Boost Converter

A Boost converter (Step-up converter) is a DC-to-DC power converter with an output voltage greater than its input voltage. It is a class of switched mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element a capacitor, inductor, or the two in combination. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

Pulse-width modulated (PWM) full-bridge converters are used in applications where the output voltage is considerably higher than the input voltage. Zero-voltage-switching (ZVS) is typically implemented in these converters. The objective of this thesis is to propose, analyze, design, implement and experimentally confirm the operation of a new Zero-Voltage- Switching PWM DC-DC full-bridge boost converter that does not have any of the drawbacks that other converters of this type have, such as a complicated auxiliary circuit, increased current stresses in the main power switches and load dependent ZVS operation.
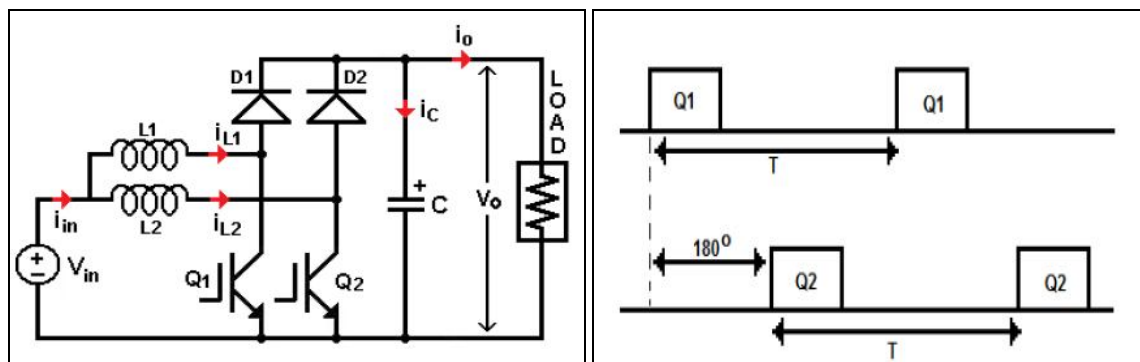
Figure 5: Interleaved Boost DC-DC converter (a) Schematic diagram (b) Timing diagram of control signal

5.1. Interleaved Boost converter

Interleaved Boost dc-dc converter is proposed for current sharing on high power application. The schematic of the interleaved boost dc-dc converter is as shown in Figure 5(a).A basic boost converter converts a DC voltage to a higher DC voltage. Interleaving adds additional benefits such as reduced ripple currents in both the input and output circuits. Higher efficiency is realized by splitting the output current into two paths, substantially reducing I^2R losses and inductor AC losses. The major challenge of designing a boost converter for high power application is how to handle the high current at the input and high voltage at the output. An interleaved boost dc-dc converter is a suitable candidate for current sharing and stepping up the voltage on high power application. In interleaved boost converter topology, one important operating parameter is called the duty cycle D. For the boost converter, the ideal duty cycle is the ratio of voltage output and input difference with output voltage. The input current and output voltage ripple of interleaved boost dc-dc converter can be minimized by virtue of interleaving operation. Moreover, the converter input current can be shared among the phases, which is desired for heat dissipation. Therefore, the converter reliability and efficiency can be improved significantly. The interleaved boost dc-dc converter consists of two parallel connected boost converter units, which are controlled by a phase-shifted switching function. To illustrate the interleaving operation, Figure 5(b) shows the timing diagram of control signals to the switches. Since this converter has two parallel units, the duty cycle for each unit is equal to (Vout-Vin)/Vout, and it is same for each unit due to parallel configuration. A phase shift should be implemented between the timing signals of the first and the second switch. Since there are two units parallel in this converter, the phase shift value is 180 degrees.

5.2. Modes of Operation

The mode of operation can be analyzed based on one channel. Since both power channels share current and because both inductors are identical, each power channel behaves identically. Based on the amount of energy that is delivered to the load during each switching period, the boost converter can be classified into continuous or discontinuous conduction mode. If all the energy stored in the inductor is delivered to the load during each switching cycle, the mode of operation is classified as discontinuous conduction mode (DCM). In this mode the inductor current ramps down to zero during the switch off-time. If only part of the energy is delivered to the load, then the converter is said to be operating in continuous conduction mode (CCM). Figure 6 shows the inductor current waveform. In order to simplify the calculation, it is assumed that the inductance value of both inductors is L_1 and L_2, where $L_1=L_2-L$, and the duty cycle of Q_1 and Q_2 denoted as D_1 and D_2, with $D_1=D_2=D$.

- State a:
  At time to, Q_1 is closed and Q_2 is opened. The current of the inductor L_1 starts to rise, while L_2 continues to discharge. The rate of change of i_{L1} is $di_{L1}/dt=V_i/L$, while the rate of change of i_{L2} is $di_{L2}/dt=(V_i-V_o)/L$

- State b:
  At time t_1, Q_1 and Q_2 are opened. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{L1} and i_{L2} are $di_{L1}/dt=di_{L2}/dt=(V_i-V_o)/L$.

- State c:
  At time t_2, Q_2 is closed while Q_1 still opened. The current of the inductor L_2 starts to rise. While L_1 continues to discharge. The rate of change of i_{L2} is $di_{L2}/dt=V_i/L$, while the rate of change of i_{L1} is $di_{L1}/dt=(V_i-V_o)/L$.

- State d:
  At time t_3, Q_2 is opened and Q_1 still opened. The situation is same as state b. The inductors L_1 and L_2 discharge through the load. The rate of change of i_{L1} and i_{L2} are $di_{L1}/dt=di_{L2}/dt=(V_i-V_o)/L$.
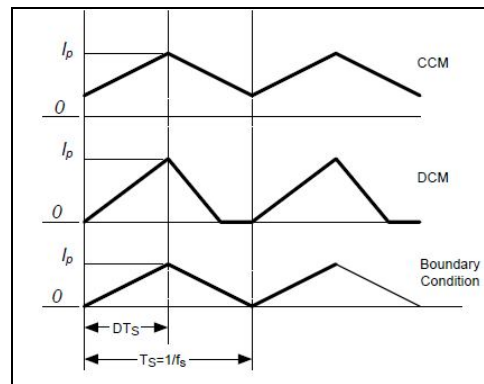
Figure 6: Inductor Current (I_L) Waveform

5.3. Continuous Versus Discontinuous Mode

Both modes of operation have advantages and disadvantages. The main disadvantages in using CCM is the inherent stability problems caused by the right-half-plane zero in the transfer function . However, the switch and output diode peak currents are larger when the converter is operating in the DCM mode. Larger peak currents necessitate using larger current and power dissipation rated switches and diodes. Also, the larger peak currents cause greater EMI/RFI problems. Most modern designs use CCM because higher power densities are possible. For these reasons, this design is based on continuous conduction mode.

5.4. Selection of Boost stage components

The interleaved boost converter design involves the selection of the inductors, the input and output capacitors, the power switches and the output diodes. Both the inductors and diodes should be identical in both channels of an interleaved design. In order to select these components, it is necessary to know the duty cycle range and peak currents. Since the output power is channeled through two Power paths, a good starting point is to design the power path components using half the output power. Basically, the design starts with a single boost converter operating at half the power. However, a trade-off exists that will depend on the goals of the design.
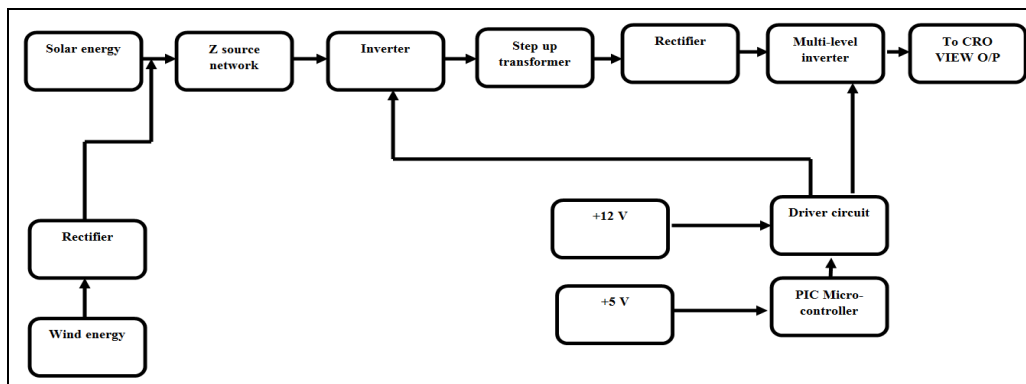
6. Block Diagram Description

Figure 7: Block Diagram of the Proposed System

The Schematic block diagram of the proposed system is as shown in the Figure 7. Solar energy and wind energy are the main input source of this system. Solar energy gives Direct current and wind gives alternating current. The maximum power is tracked using Maximum Power Point Tracking. Solar and the wing energy are combined together. Wind energy gives alternating current which is converted into DC using a rectifier. The dc from solar and the wind combine together, and the average dc supply is given to the Z source network, which is used to overcome the disadvantage of voltage Source Inverter (VSI) and Current Source Inverter (CSI). It constitutes of two inductors and two capacitors. The main purpose of using   Z source network is that it can perform both Buck and boost operation. The Boosted output from the Z-source network is given to the inverter which converts the DC into AC. Step up transformer is used to step up the voltage applied to it. It is then given to the rectifier which converts AC into DC and then gives the output to the multilevel inverter which uses the POD technique and hence the harmonics gets reduced. The output of the above process can be viewed through the Cathode Ray Oscilloscope (CRO).

7. Simulation

The simulation is mainly carried out under three categories.
- With interleaving and proposed cascaded H-bridge MLI using POD technique as shown in Figure 8.
- With interleaving and normal MLI as shown in Figure 9.

- Without interleaving and proposed cascaded H-bridge MLI using POD technique as shown in Figure 10.

7.1. With interleaving and proposed cascaded H-bridge MLI using POD technique
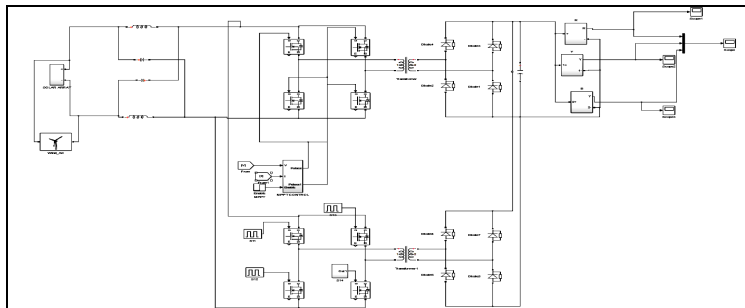

Figure 8: Simulink Model with Interleaving and POD Technique

The Simulink model of the proposed system is as shown in Figure 8. The solar and the wind input are combined together and given to the Z source network, which acts as the boost up the voltage and then passes through the interleaved circuit which splits up the voltage and gives higher efficiency. The DC output is given to the MLI which, along with POD technique reduces the harmonic distortions.

7.2. With Interleaving and Normal MLI
The Simulink model of the system with interleaving and the normal multilevel inverter is as shown in Figure 9. Normal 5 level inverter is used.
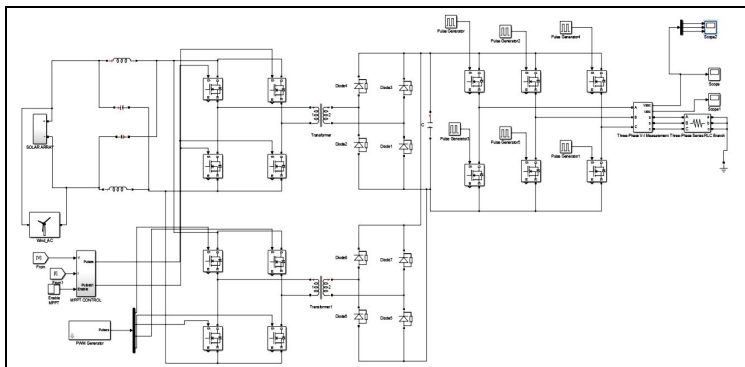

Figure 9: Simulink Model with Interleaving and Normal MLI

7.3. Without Interleaving and Proposed MLI
The simulink model Of the system without interleaving and the proposed MLI is as shown in Figure 10. MLI with phase opposition Disposition technique is used.
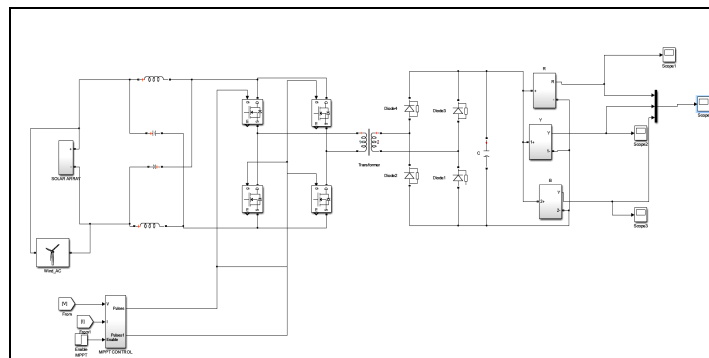

Figure 10: Simulink Model without Interleaving and POD Technique

8. Results
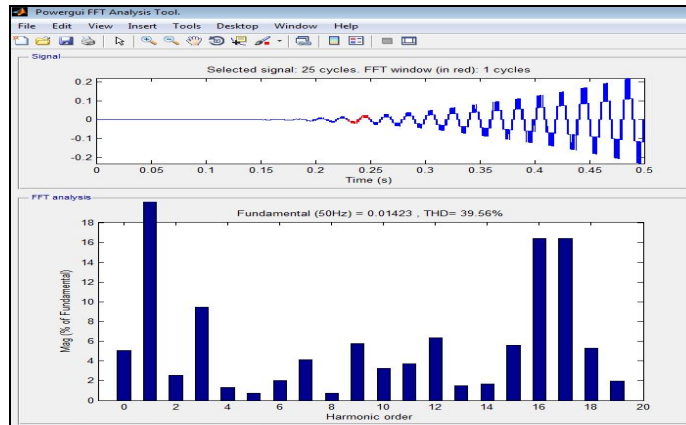
8.1. With Interleaving and POD Technique

Figure 11: O/P - With Interleaving and With POD Technique
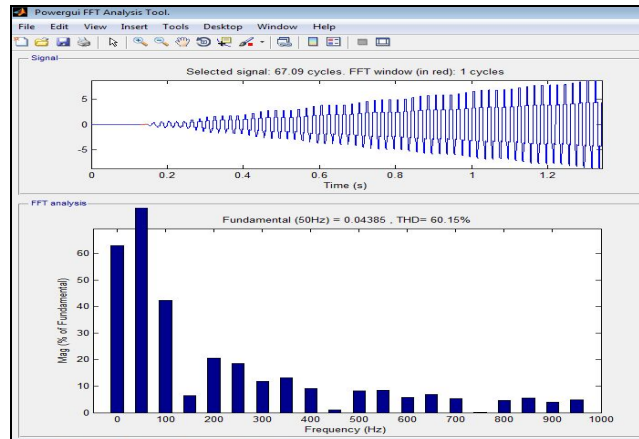
8.2. With Interleaving and Normal MLI

Figure 12: O/P - With Interleaving and Normal MLI

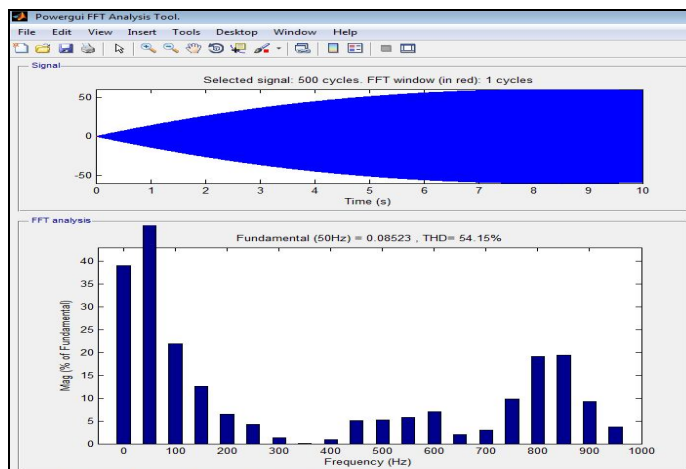*8.3. Without interleaving and POD technique*

Figure 13: Without Interleaving and POD Technique

9. Conclusion

This project presents a novel grid-connected Boost full-bridge Photovoltaic (PV) micro inverter system and its control implementations. The operating principles and dynamics of the Boost-full-bridge dc-dc converter were analyzed and a customized MPPT control was developed correspondingly. This project also proposes a new multi-level inverter topology based on an H-bridge inverter with four switches connected to the DC link. The proposed MLI has many advantages. It is more reliable and cost competitive than the conventional two level and multi-level inverters, switching losses are more negligible. Only one carrier signal is required to generate the PWM signals for four switching devices. The proposed topology can be easily extended to 9-level or higher level with minimized active device component count. The proposed system was simulated and constructed, and the functionality of the suggested control concept was proven. From the results acquired during the simulations and hardware experiments, it was confirmed that, with a well-designed system including a proper converter and selecting an efficient and proven algorithm, the implementation of MPPT is simple and can be easily constructed to achieve an acceptable efficiency level of the PV modules. The results also indicate that the proposed control system is capable of tracking the PV array maximum power and thus improves the efficiency of the PV system and reduces low power loss and system cost.

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