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DC–DC Non-isolated Boost Converter Based on the Five-State Switching Cell and Voltage Multiplier Cells

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Abstract:
This paper introduces a dc–dc boost converter based on the five-state switching cell and voltage multiplier cells. A brief literature review is presented to demonstrate some advantages and inherent limitations of several topologies that are typically used in voltage step up applications. The behavior of the converter is analyzed. The converter can be applied to uninterruptible power supplies and is also adequate to operate as a high gain boost stage cascaded with inverters in renewable energy systems. Furthermore, it can be applied to systems that demand dc voltage step up such as electrical fork-lift, renewable energy conversion systems, and many other applications.

Key words: *Boost converters, dc–dc converters, high voltage gain, voltage multiplier cells (VMCs)*

1. Introduction

Depending on the application nature, several types of static power converters are demanded for the adequate conversion and conditioning of the energy provided by primary sources such as photovoltaic arrays, wind turbines, and fuel cells. Typical solutions include the use of low-frequency or high-frequency power transformers to adjust the voltage gain properly.

The conventional boost converter can be advantageous for step-up applications that do not demand very high voltage gains mainly due to the resulting low conduction loss and design simplicity. Theoretically, the boost converter, static gain tends to be infinite when duty cycle also tends to unity. However, in practical terms, such gain is limited by the I^2R losses in the boost inductor and semiconductor devices due to their intrinsic resistances, also leading to the necessity of accurate and high-cost drive circuitry for the active switch.

Due to the importance of the conventional boost converter in obtaining distinct and improved topologies for voltage step-up applications, some techniques have been developed and modified with the aim of improving the characteristics of the original structure. Basically, two strategies are adopted for this purpose: voltage step-up with and without using extreme values of duty cycle. Some arrangements existent in the literature will be discussed as follows.

An early work concerned with non-isolated converters with large conversion ratios was proposed in, where multiple stages are connected in parallel to obtain high voltage step-up converters. However, the use of multiple controlled switches, diodes, and inductors may lead to high component count, making the proposed approach not adequate to achieve very large ratios that are typically obtained with the use of transformers.

Voltage multiplier cells (VMCs) are adopted to provide high voltage gain and reduced voltage stress across the semiconductor elements. Interleaving also allows the operation of the multiplier stages with reduction of the current stress through the devices. In addition, size of input inductors and capacitors is drastically reduced. The voltage stress across the main switches is limited to half of the output voltage for a single multiplier stage. However, high component count is necessary, with the addition of a snubber circuit due to the sum of the reverse recovery currents through the multiplier diodes and consequent increase of conduction losses.

2. Proposed Topology

The canonical switching cell is an approach that allows obtaining and classifying the classical dc–dc converters, from which some families of converters can be derived.

With the aim of achieving higher power density, switching frequency is usually increased, with consequent reduction of size and volume of reactive elements. Switching losses are consequently increased, while the volume of heat sinks also is. This practice therefore compromises the very reduction of physical dimensions in static power converters.

It is also possible to increase the efficiency by the use of the 3SSC, which is derived from the dc–dc push-pull converter. It is formed by two controlled switches S_1 and S_2, two diodes D_1 and D_2, one autotransformer T, and one inductor L.

Typically, a high-frequency transformer is used in static power converters to achieve a high voltage conversion ratio, either in step-up or step-down applications. This practice eliminates the need to operate with extreme duty cycle values, even though the additional loss due and increased size and weight associated

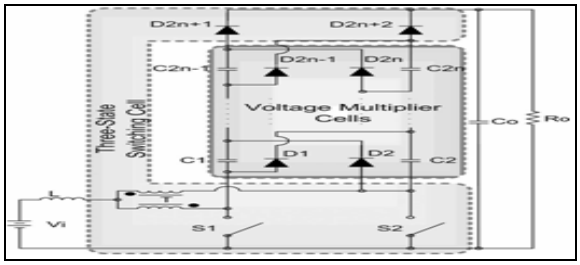

Figure 1 Proposed boost converter based on the association of the five-state switching cell and voltage multiplier cells

With the transformer are the resulting disadvantages. For instance, let us consider the circuit of the interleaved flyback-boost converter mentioned in. Even though the static gain becomes $N \cdot [1/1 - D)]$, where N is the turns ratio and D is the duty cycle, and the current rating of the main switches is reduced by the use of interleaving cells, the proposed approach does not contribute to the very reduction of conduction losses. In structures, using the 3SSC, this is an intrinsic and remarkable advantage.

In order to better understand the operating principle of the structures, the following assumptions are made:

- The input voltage is lower than the output voltage;
- Steady-state operation is considered;
- Semiconductors and magnetics are ideal;
- switching frequency is constant;
- The turn's ratio of the autotransformer is unity;
- The drive signals applied to the switches are 180° displaced.

3. Operating Principle

The proposed approach is based on the use of VMCs to further increase the step-up ability of the boost converter. The introduced concept can be ex-tended to the use of two multiplier cells, as the resulting topology is presented in Figure. The equivalent circuits that correspond to the converter operation and the relevant theoretical waveforms are presented in Figures. 3 and 4, respectively.

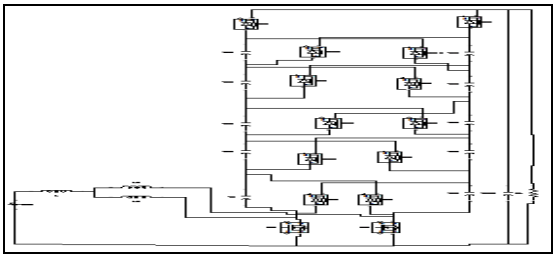

Figure 2: Proposed converter of five voltage multiplier cells (mc=5)

- MODE 1

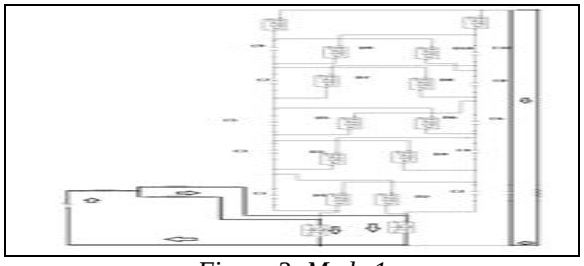

Figure 3: Mode 1

Switches S1 and S2 are turned ON, while all diodes are reverse biased. Energy is stored in inductor L and there is no energy transfer to the load. The output capacitor provides energy to the load.

- MODE 2

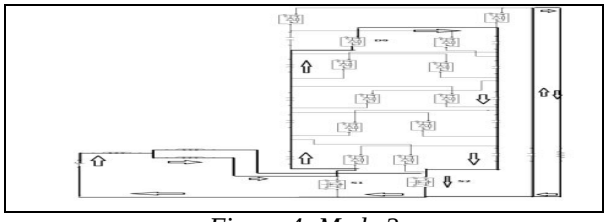

Figure 4: Mode 2

Switch S1 is turned OFF, while S2 is still turned ON and diodeD9 is forward biased. There is no energy transfer to the load as well. Inductor L stores energy, capacitors C1 a C3,C5 and C7 are discharged, and capacitors C2 , C4 , and C6,C8,C10 are charged.

- MODE 3

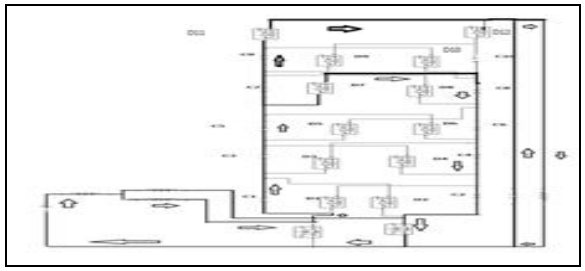

Figure 5: Mode 3

Switch S1 is turned OFF, while S2 is still turned ON and diodeD7 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D11* .Inductor L stores energy, capacitors C1, C3 C5, C7, C9 are discharged, and capacitors C2, C4, and C6, C8 are charged.

- MODE 4

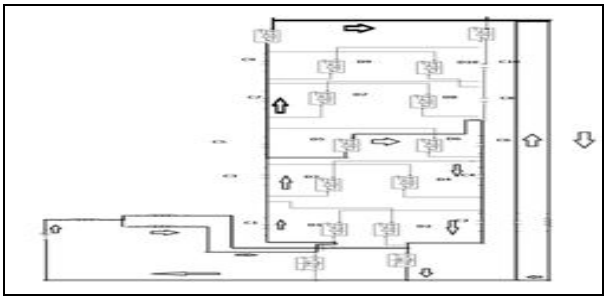

Figure 6: Mode 4

Switch S1 is turned OFF, while S2 is still turned ON and diodeD5 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D11.* Inductor L stores energy, capacitors C1, C3, C5, C7, C9 are discharged, and capacitors C2, C4, C6 are charged.

- MODE 5

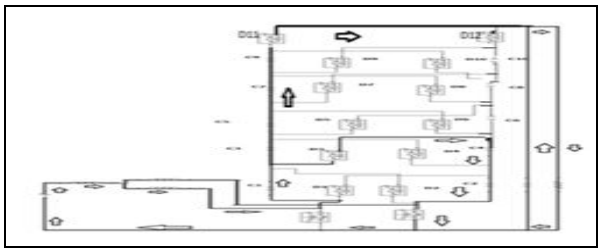

Figure 7: Mode 5

Switch S1 is turned OFF, while S2 is still turned ON and diodeD3 is forward biased while all the remaining ones are reverse biased. Energy is transferred to the output stage through *D11*. Inductor L stores energy, capacitor C1, C3, C5, C7, C9 are discharged, and capacitors C2, C4 are charged.

- MODE 6

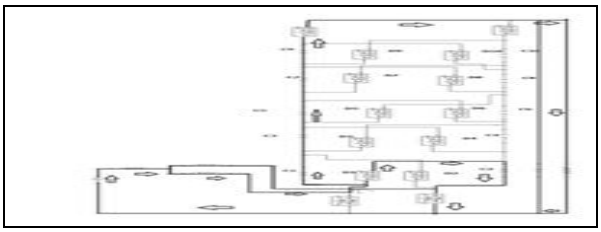

Figure 8: Mode 6

Switch S2 remains turned ON, diode D3 is reverse biased, and diode D1 is forward biased while all the remaining ones are reverse biased. Energy is transferred to the load through D11. The inductor is discharged, and so are capacitors C1, C3, and C5, C7, C9 while C2 is charged.

- MODE 7

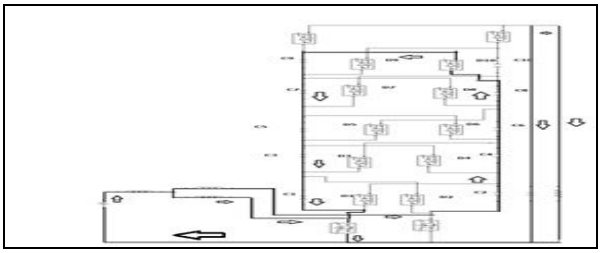

Figure 9: Mode 7

Switch S2 is turned OFF and switch S1 is still turned ON. Diode D10 is forward biased while all the remaining ones are reverse biased. The inductor is charged by the input source, although capacitors C2, C4, C6, C8 are discharged and the capacitors C1, C3, C5, C7, C9 are charged.

- MODE 8

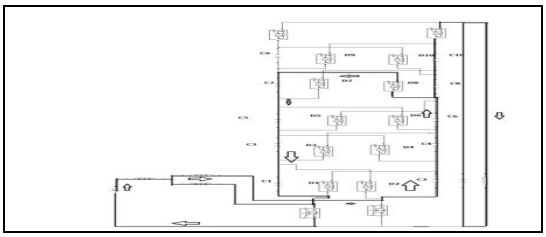

Figure 10: Mode 8

Switches S1 turned ON, DiodeD8 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy, and capacitors C1, C3, C5, C7 are charged. Capacitors C2 is discharged, and so are C4, C6, C8, C10.

- MODE 9

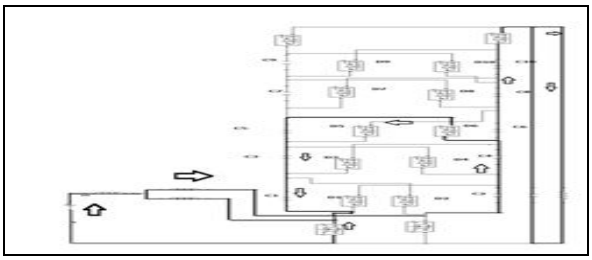

Figure 11: Mode 9

Switches S1turned ON, Diode D6 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy, and capacitors C1and C3, C5, are charged. Capacitor C2 is discharged, and so are C4 and C6, C8, C10.

- MODE 10

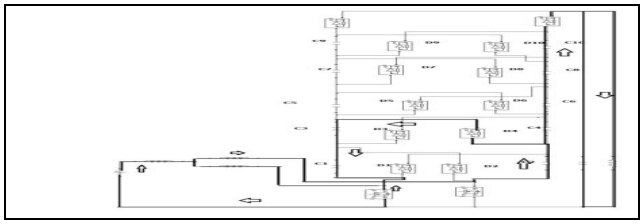

Figure 12: Mode 10

Switches S1turned ON, Diode D4 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy and capacitors C1and C3 are charged. Capacitor C2 is discharged, and so are C4 and C6, C8, C10.

- MODE 11

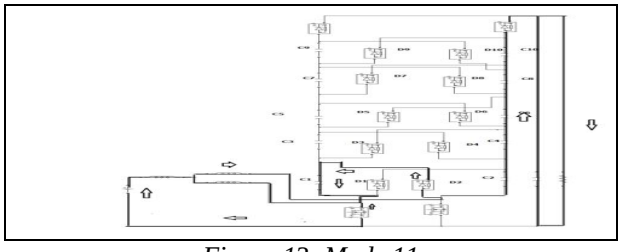

Figure 13: Mode 11

Switches S1turned ON, Diode D2 is forward biased, while all the remaining ones are reverse biased. Energy is transferred to the output stage through D12. The inductor stores energy and capacitors C1 is charged. Capacitor C2 is discharged, and so are C4 and C6, C8, C10.

Static Gain and Energy Storage Elements:

The static gain of the converter can be obtained from the inductor volt second balance. The voltage area multiplied by the time interval that corresponds to the inductor charge is equal to that regarding the discharge. The following expressions can then be derived:

$$V_{D5,D6} = (D-1)\cdot \Delta V_C + \frac{V_0 \cdot D}{5} + \left(\frac{2\cdot C_4^2}{C_2} + 12\cdot C_4\right)\cdot \frac{\Delta V_C^2}{T \cdot I_L} \quad (1)$$

$$V_i = D\cdot T_S - \frac{T_s}{2} = -\left(V_i - \frac{V_0}{4}\right)\cdot (1 - D\cdot T_S) \quad (2)$$

$$\frac{V_0}{V_i} = \frac{2}{1 - D} \quad (3)$$

Where *VI is* the input voltage. Expression (3) can then be generalized for any number of VMCs *mc* as

$$G_V = \frac{V_0}{V_i} = \frac{mc = 1}{1 - D} \quad (4)$$

Expression (4) is plotted and shown in Fig. 5. The dotted line plotted in Fig. 5 corresponds to 1/1 − 2 ⋅ *D*, representing the boundary from which the static gain changes. One can see that it really occurs for *D* < 0.5 at a different point for each number of employed multiplier cells because the multiplier capacitors are not fully charged due to the reduced charge time.

The average values of the output current *Io* and output

Voltage *VO* as a function of the duty cycle, input current *Ii*, input voltage *Vl*, and number of multiplier cells *mc* are defined by, respectively,

$$V_0 = \frac{V_i (mc + 1)}{1 - D} \quad (5)$$

$$I_0 = \frac{I_i (1 - D)}{mc + 1} \quad (6)$$

Assuming that the current through inductor *L* increases linearly during the first operating stage, what is valid for the generic configuration in Fig. 1, the following expression results,

$$L\frac{\Delta iL}{\Delta t} = \frac{V_0 (1 - D)}{mc + 1} \quad (7)$$

Where Δ*iL* is the ripple current through the inductor and Δ*t* is the time interval that corresponds to the overlapping between the drive signals applied to the main switches, determined by (8)

$$\Delta t = \frac{\Delta iL}{(2D-1)T_S / 2} = (2D-1)T_S / 2 \quad (8)$$

Substituting (8) in (7) gives

$$L \frac{\Delta iL}{(2D-1)T_S/2} = \frac{V_0(1-D)}{mc+1} \quad (9)$$

By rearranging (9), expression (10) can be obtained, which corresponds to the normalized ripple current β as a function of the duty cycle

$$\beta = \frac{2L\Delta iL}{T_S V_0} = \frac{(1-D)(2-D)}{mc+1} \quad (10)$$

Expression (10) is plotted in Fig. 6, where it can be seen that the maximum ripple current is obtained when D = 0.75, and the respective inductance is calculated from

$$L = \frac{V_0}{16 f_S (mc+1)\Delta I_L} \quad (11)$$

The multiplier capacitors *Cn* and the output capacitor *Co* can be obtained from the following expressions:

$$C_1 = C_2 = 1/4 \frac{I_i(1-D)}{f_S \Delta V_C} \quad (12)$$

$$C_{2j+1} = C_{2j+2} = \frac{1}{3n} \frac{I_i(1-D)}{f_S \Delta V_{Cn}} \quad (13)$$

j=0, 1, 2, . . . for n=1, 2, . . . , respectively, if mc=2

$$C_{2j+1} = C_{2j+2} = \frac{3-n+1}{8} \frac{I_i(1-D)}{f_S \Delta V_{Cn}} \quad (14)$$

j=0, 1, 2, . . . for n=1, 2, 3, . . . , respectively, if mc=3

$$C_0 = \frac{I_0}{2} \frac{I_i(1-D)}{f_S \Delta V_C} \quad (15)$$

The average currents through the diodes are given by

$$I_{D1(avg)} \ldots . D_{D6(avg)} = \frac{1}{6}(1-D) I_L \quad (16)$$

The maximum voltages across the switches and diodes are given by

$$V_{s1} = V_{s2} = \frac{V_0}{3}(1-D) - \frac{\Delta V_C^2}{I_L T_S}\left(4\frac{C_4^2}{C_2} - 14 C_4\right) \quad (17)$$

$$V_{D1} = V_{D2} = (1-D)\Delta V_C + \frac{V_0}{3} - \left(4\frac{C_4^2}{C_2} - 8C_4\right)\frac{\Delta V_C^2}{I_L T_S} \quad (18)$$

$$V_{D3} = V_{D4} = \frac{V_0}{3} - \left(4\frac{C_{+4}^2}{C_2} - 8C_4\right)\frac{\Delta V_C^2}{I_L T_S} \quad (19)$$

Where ΔVc *is* the ripple voltage across the multiplier capacitors, *Ts* is the switching period, and *VO* is the output voltage.

4. Experimental Results

An experimental prototype for the structure with five multiplier cells has been designed accordingly and implemented in this paper. While the components used in the prototype are at recent market specifications. The converter modeling and design guidelines regarding the control system are presented and will not be discussed here again. The converter startup is given, where the output voltage reaches 510 V as desired, and the input voltage increases from null to 52 V. According to the simulation of the proposed circuit the results are given below, The output voltage for the proposed circuit system is given as approximately Vo=510V.

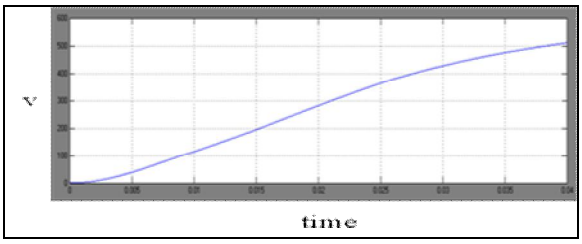

Figure 14: Simulation of proposed system V0=510V

The current output values of the proposed system can be obtained from the below graph. The output current reaches Io=0.9A.

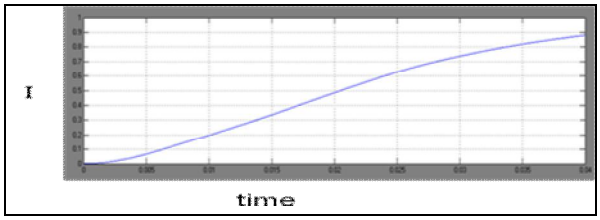

Figure 15: Simulation of proposed system Io=0.9A

5. Conclusion

This paper has proposed a new generalized non-isolated boost converter with high voltage gain. The topology is adequate for several applications such as photovoltaic systems, SMPS and UPSs, hybrid vehicles where high voltage gain between the input and output voltages are demanded also in efficiency enriching applications.

6. References

1. R. Kadri, J.-P. Gaubert, and G. Champenois, "An improved maximum power point tracking for photovoltaic grid-connected inverter based on voltage-oriented control," IEEE Trans. Ind. Electron., vol. 58, no. 1, 66–75, Jan. 2011.
2. W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Trans. Ind. Electron., vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
3. C. G. C. Branco, C. M. T. Cruz, R. P. Torrico-Bascope, and F. L. M. Antunes, "A non-isolated single-phase UPS topology with 110-V/220-V input-output voltage ratings," IEEE Trans. Ind. Electron., vol. 55, no. 8, 2974–2983, Aug. 2008.
4. S. V. Araujo, R. P. Torrico-Bascope, and G. V. Torrico-Bascope, "Highly efficient high step-up converter for fuel-cell power processing based on three-state commutation cell," IEEE Trans. Ind. Electron., vol. 57, no. 6, 1987–1997, Jun. 2010.
5. Z. Amjadi and S. S. Williamson, "Power-electronics-based solutions for plug-in hybrid electric vehicle energy storage and management systems," IEEE Trans. Ind. Electron., vol. 57, no. 2, pp. 608–616, Feb. 2010.

6. L. G. Junior, M. A. G. Brito, L. P. Sampaio, and C. A. Canesin, "Integrated inverter topologies for low power photovoltaic systems," in Proc. Int. Conf. Ind. Appl., 2010, pp. 1–5.
7. S. V. Araujo, R. P. Torrico-Bascope, G. V. Torrico-Bascope, and L. Menezes, "Step-up converter with high voltage gain employing three-state switching cell and voltage multiplier," in Proc. Power Electron. Spec. Conf., 2008, pp. 2271–2277.
8. R. A. da Camara, C. M. T. Cruz, and R. P. Torrico-Bascope, "Boost based on three-state switching cell for UPS applications," in Proc. Brazilian Power Electron. Conf., 2009, pp. 313–318.
9. R. D. Middlebrook, "Transformerless DC-to-DC converters with large conversion ratios," IEEE Trans. Power Electron., vol. 3, no. 4, pp. 484– 488, Oct. 1988.
10. L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking," in Proc. Appl. Power Electron. Conf. Expo., 2000, pp. 1163–1169.
11. X. G. Feng, J. J. Liu, and F. C. Lee, "Impedance specifications for stable dc distributed power systems," IEEE Trans. Power Electron., vol. 17, no. 2, 157–162, Mar. 2002.
12. Y. R. Novaes, A. Rufer, and I. Barbi, "A new quadratic, three-level, DC/DC converter suitable for fuel cell applications," in Proc. Power Convers. Conf., Nagoya, Japan, 2007, pp. 601–607.
13. K. W. Ma and Y. S. Lee, "An integrated flyback converter for dc unin-terruptible power supply," IEEE Trans. Power Electron., vol. 11, no. 2, 318–327, Mar. 1996.
14. C. T. Choi, C. K. Li, and S. K. Kok, "Modeling of an active clamp discon-tinuous conduction mode flyback converter under variation of operating condition," in Proc. IEEE Int. Conf. Power Electron. Drive Syst., 1999, 730–733.
15. K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," Proc. Inst. Elect. Eng.—Elect. Power Appl., vol. 151, no. 2, pp. 182–190, Mar. 2004.
16. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated converters," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–887, Mar. 2008