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Deciding Optimal Location for Placing FACTS Devices [UPFC, IPQC, DPFC] Using Bang-Bang Control Technique

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Abstract:
There are many problems arising in the electricity networks. In that, voltage fluctuation and power loss reduction becomes a major drawback in the electrical power supply system. Hence it is necessary to enhance the system power flow by placing suitable facts devices. Hence, the placement of FACTS devices in suitable location can lead to control in-line flow and maintain bus voltages in desired level and reduce the losses. The facts devices like Upfc, Ipqc, Dpfc are compared with each other, and the higher efficiency converter is identified. Finally, the location for better efficiency is traced out. The unique control capability of the UPFC is given by the back-to-back connection between the shunt and series converters, which allows the active power to freely exchange. UPFC has a DC link, whereas DPFC does not have any DC link. It is connected directly to the transmission line so the hysteresis loss is controlled. Optimal location and better efficiency of UPFC, IPQC and DPFC are found out and the devices are placed at the exact location. This project presents one of the Bang-Bang Controller to seek the optimal location of FACTS devices in a power system Proposed algorithm is tested on IEEE 14 bus power system for optimal location of multi-type FACTS devices and the results are presented.

Key words*: Bang-Bang control technique, Distributed Power Flow Controller (DPFC), FACTS (Flexible AC Transmission System), Improved Power Quality Controller (IPQC), optimal location, Unified Power Flow Controller (UPFC)*

1. Introduction

Electric power distribution network is playing an essential role in power system planning. This type of power systems has a major function to serve distributed customer loads along a feeder line; therefore under competitive environment of electricity market service the electric energy transfer must not be interrupted and at the same time they must provide reliable, stable and high quality of electric power. FACTS cover several systems based on power electronics for AC power transmission and distribution. FACTS are the family of devices which can be used in series, in shunt and in some cases both as series and shunt. Series capacitor (SC), Thyristor controlled series capacitor (TCSC) and STATCOM have important applications in transmission and distribution. SVC and SC are the devices which have been utilized for a long time. Real and reactive power is not stable in the devices which were used earlier and had less efficiency. Advanced FACTS devices like UPFC (Unified Power Flow Controller, DPFC (Distributed Power Flow Controller, IPQC (Improved Power Quality Controller) are implemented in this paper. Shunt series connections are present in DPFC and UPFC. IPQC has only the series connection. There are many benefits of the FACTS devices which can be attained in AC systems. Minimized transmission losses, Minimized environmental impact, improved power quality, improved power system stability and availability, improved power transmission capability are the benefits of the FACTS devices. These devices are more reliable and have high efficiency and have direct control over real and reactive power flow.

2. Devices Description

Advanced FACTS devices like UPFC, IPQC and DPFC are used. It provides fast dynamic reactive power support and voltage control and hence reduces the financial cost.

2.1. Unified Power Flow Controller

UPFC is most comprehensive flexible ac transmission system. The schematic diagram of UPFC is as shown in Figure 1. It consists of a series and a shunt converter connected by a common dc link capacitor and can simultaneously perform the function of transmission line real/reactive power flow control in addition to UPFC bus voltage/shunt reactive power control.

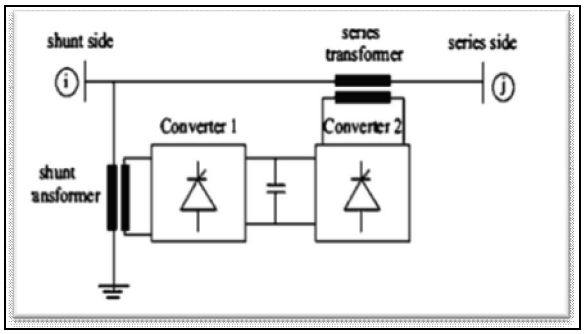

Figure 1: Schematic Diagram Of UPFC

The shunt converter of the UPFC controls the UPFC bus voltage/shunt reactive power and the dc link capacitor voltage. The series converter of the UPFC controls the transmission line real/reactive power flows by injecting a series voltage of adjustable magnitude and phase angle. The interaction between the series injected voltage and the transmission line current leads to real and reactive power exchange between the series converter and the power system. This arrangement of UPFC ideally works as a ideal ac to dc power converter. The real power can freely flow in either direction between ac terminals of the two converters. Each converter can independently generate or absorb reactive power at its own AC output terminal. The main functional is provided by the shunt converter by injecting an ac voltage considered as a synchronous ac voltage source with controllable phase angle and magnitude in series with the line.

2.2. Improved Power Quality Controller

IPQC is a three phase integrated active rectifier and shunt power quality compensator. The schematic diagram of IPQC is as shown in Figure 2. The measurement of only three currents is required, and the control algorithm can be implemented using a low cost controller.

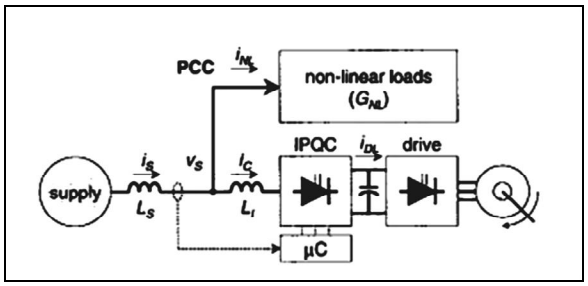

Figure 3: Schematic Diagram of IPQC

IPQC improves the harmonic content of the supply current, displacement power factor, supply current balance, and can serve as a four-quadrant active rectifier for motor drives and other dc-link loads.

The IPQC performs the following functions:

- Improvement of the supply current (i_s) harmonic content in the presence of multiple nonlinear loads.
- Improvement of the displacement power factor in the presence of multiple loads with a leading or lagging power factor.
- Improvement of the supply current balance
- Four quadrant active rectifier operation.

2.3. Distributed Power Flow Controller

The DPFC is derived from the Unified Power Flow Controller (UPFC). The schematic diagram of DPFC is as shown in Figure 3. The DPFC can be considered as a UPFC with an eliminated common dc link.

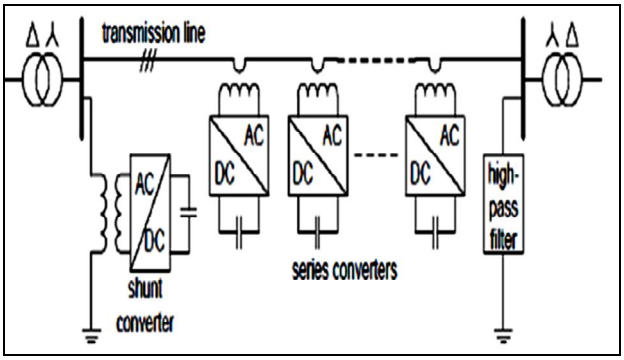

Figure 3: Schematic Diagram of DPFC

The active power exchange between the shunt and series converters, which is through the common dc link in the UPFC, is now through the transmission lines in the third-harmonic frequency. The DPFC employs the distributed FACTS (D-FACTS) concept, which is to use multiple small size single phase converters instead of the one large size three phase series converter in the UPFC. The large number of series converters provides redundancy, thereby increasing the system reliability. Two approaches are applied to the UPFC to increase the reliability and to reduce the cost; they are as follows. First, eliminating the common dc link of the UPFC and second distributing the series converter. By combining these two approaches, the new FACTS device DPFC is achieved. The DPFC consists of one shunt and several series connected converters. The shunt converter is similar as a STATCOM, while the series converter employs the D-FACTS concept, which is to use multiple single-phase converters instead of one large rated converter. Each converter within the DPFC is independent and has its own dc capacitor to provide the required dc voltage.

3. Bang-Bang Control Technique

Bang-Bang controller (ON-OFF controller), also known as Hysteresis controller are the switches which acts as a feedback controller between the two states. It is the most common residential thermostat. It is a variable structure controller, which is used in heavy side function in discrete form. The representation of the grid interfacing inverter control is as shown in the Figure 2. Neutral current of the load is compensated using the fourth leg of the inverter. The main aim of the proposed approach is to regulate the power at PCC during the following conditions:

- $P_{RES} = 0$
- P_{RES} < total load power (P_L)
- P_{RES} > total load power (P_L)

While performing the power management operation.

$$I_{dc2} = P_{inv} / V_{dc} = P_G + P_{loss}/V_{dc} \quad (1)$$

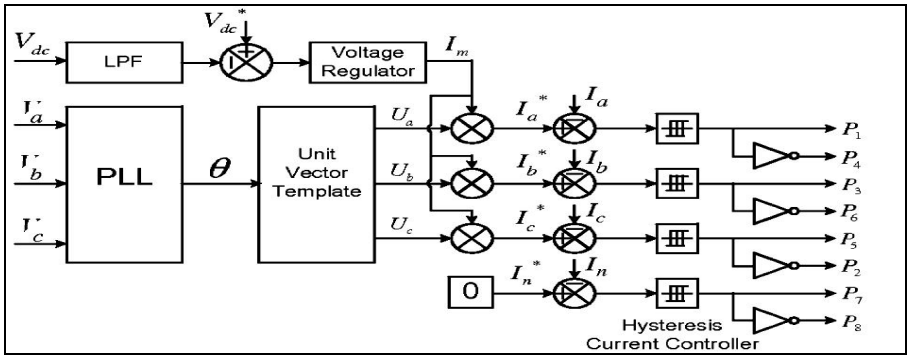

Figure 4: Block Diagram Representation Of Grid-Interfacing Inverter Control

If PCC is non- linear or unbalanced or the combination of both when connected to the load, then the approach compensates the harmonics, unbalance, and neutral current. The duty ratio of inverter switches is varied in a power cycle, such that the combination of load and inverter injected power appears as balanced resistive load to the grid. The multiplication of the action current component (I_m) with unity grid voltage vector templates (Us, U_b and U_c) generates the reference grid currents (I_a^*, I_b^* and I_c^*). The reference grid neutral current (I_n^*) is set to zero, being the instantaneous sum of balanced grid currents. The grid synchronizing angle obtained from phase locked loop (PLL) is used to generate unity vector template as

$$U_a = \mathrm{Sin}(\theta) \quad (2)$$

$$U_b = \mathrm{Sin}(\theta - 2\mu/3) \quad (3)$$

$$U_c = \mathrm{Sin}(\theta + 2\mu/3) \quad (4)$$

The actual dc-link voltage (V_{dc}) is sensed and passed through a first-order low pass filter (LPF) to eliminate the presence of switching ripples, on the dc-link voltage and in the generated reference current signals. The difference of this filtered dc-link voltage and reference dc-link (V_{dc}^{*}) is given to a discrete PI regulator to maintain a constant dc-link voltage under varying generations and load conditions. The dc-link voltage error $V_{dc\,err}(n)$ at nth sampling instant is given as:

$$V_{dcerr(n)}=V_{dc}^{*}{}_{(n)}-V_{dc(n)} \quad (5)$$

The output of the discrete-PI regulator at nth sampling instant is expressed as

$$I_{m(n)}=I_{m(n-1)}+K_p V_{dc}(V_{dcerr(n)}-V_{dcerr(n-1)})+K_{IVdc} V_{dcerr(n)} \quad (6)$$

Where K_{PVDC} = 10 and K_{IVdc} = 0.05 are proportional and integral gains of the dc-voltage regulator. The instantaneous values of reference three phase grid currents are computed as

$$I_a^{*}=I_m.U_a \quad (7)$$

$$I_b^{*}=I_m . U_b \quad (8)$$

$$I_c^{*}=I_m . U_c \quad (9)$$

The neutral current, present if any, due to the loads connected to the neutral conductor should be compensated by the fourth leg of grid-interfacing inverter and thus should not be drawn from the grid. In other words, the reference current for the grid neutral current is considered as zero and can be expressed as

$$I_n^{*}=0 \quad (10)$$

The reference grid currents (I_a^{*}, I_b^{*}, I_c^{*}, and I_n^{*}) are compared with actual grid currents (I_a, I_b, I_c and I_n) to compute the current errors as

$$I_{aerr} = I_a^{*}- I_a \quad (11)$$

$$I_{berr}=I_b^{*}-I_b \quad (12)$$

$$I_{cerr}=I_c^{*}-I_c \quad (13)$$

$$I_{nerr}=I_n^{*}-I_n \quad (14)$$

These current errors are given to the hysteresis current controller. The hysteresis controller then generates the switching pulses (P_1 to P_8) for the gate drives of the grid-interfacing inverter. The average model of 4-leg inverter can be obtained by the following state space equations.

$$dI_{Inva}/dt=(V_{Inva}-V_a)/L_{sh} \quad (15)$$

$$dI_{Invb}/dt=(V_{Invb}-V_b)/L_{sh} \quad (16)$$

$$dI_{Invc}/dt=(V_{Invc}-V_c)/L_{sh} \quad (17)$$

$$dI_{Invn}/dt=(V_{Invn}-V_n)/L_{sh} \quad (18)$$

$$dV_{dc}/dt=(I_{Invad}+I_{Invbd}+I_{Invcd}+I_{Invnd})/C_{dc} \quad (19)$$

Where I_{Inva}, I_{Invb}, I_{Invc} and I_{Invn} are the three-phase ac switching voltages generated on the output terminal of the inverter. These inverter output voltages can be modeled in terms of instantaneous dc bus voltage and switching pulses of the inverter as

$$I_{Invad} = I_{Inva}(P_1-P_4) \quad (20)$$

$$I_{Invbd} = I_{Invb}(P_3-P_6) \quad (21)$$

$$I_{Invcd} = I_{Invc}(P_5-P_2) \quad (22)$$

$$I_{Invad} = I_{Inva}(P_7-P_8) \quad (23)$$

The switching pattern of each IGBT inside inverter can be formulated on the basis of error between actual and reference current of the inverter.

4. Block Diagram Description

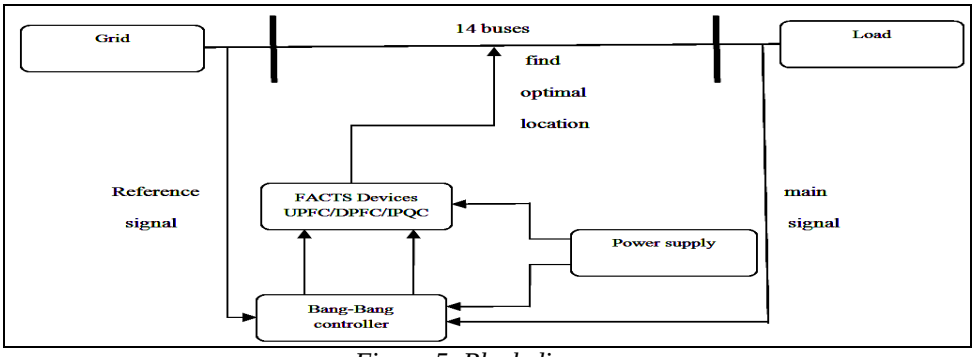

Figure 5: Block diagram

In a normal transmission line from grid to the load side the location of the fault can be found out by optimal location of the FACTS devices. 14 bus systems is connected in between the grid and the load. The output from the grid is taken as the reference signal and the signal from the load side are given as the input to the Bang-Bang control technique. The signals which are given as the input are compared with each other and if there is a difference between the two signals then the pulse will be generated and given to the FACTS

devices to trigger the pulses. FACTS device will act immediately and the optimal location can be found out in a 14 bus system and the devices can be placed in the proper location. Separate power supply is given for bang-Bang control technique and FACTS devices.

5. Simulation

MATLAB version 8.002 (2012-(b)) is used. Advanced FACTS devices are used in the IEEE 14 bus system to find the optimal location of the FACTS devices. Bang-Bang control technique is used for the hysteresis control of the devices, i.e. UPFC, IPQC and DPFC. Optimal location of the devices is found out easily and the devices are placed at the suitable location. Bang-Bang control technique is used because of its simplicity of implementation. Also, besides the fast response current loop, the method does not need any knowledge of the load parameters.

5.1. With Distributed Power Flow Controller

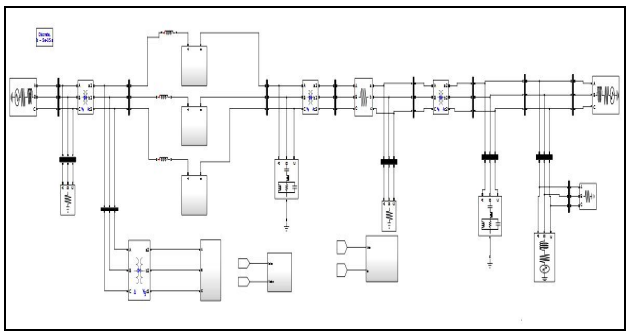

Figure 6: With Distributed Power Flow Controller

DPFC is placed in between the IEEE 14 bus system and the simulation for with and without DPFC. The MATLAB model of with DPFC is as shown in fig 6.

5.2. With Improved Power Quality Controller

IPQC is placed in between the IEEE 14 bus system. The simulation is performed with and without IPQC. The MATLAB model of with IPQC as shown in figure 7. The optimal location of IPQC is found out and they are placed in a proper location and the better efficiency of the device is found out.

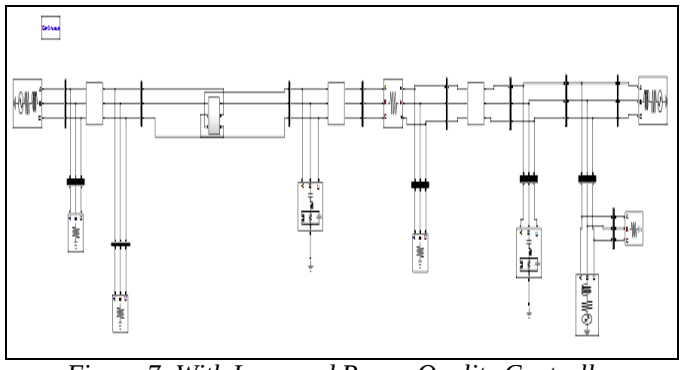

Figure 7: With Improved Power Quality Controller

5.3. With Unified Power Flow Controller

UPFC is tested in IEEE 14 bus system. The optimal location of the UPFC is found out and it is placed in a proper location. The efficiency of the devices is found out. The Simulink model of UPFC is as shown in the fig 8.

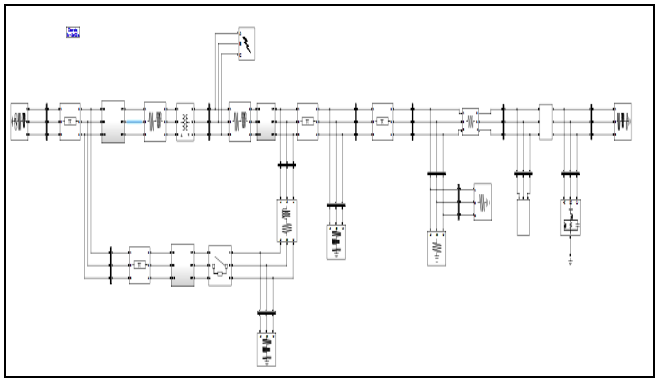

Figure 8: With Unified Power Flow Controller

6. Simulation Results

The simulation results of the FACTS devices (UPFC, DPFC and IPQC are tested in IEEE 14 bus system and the better efficiency is found out and the devices are placed at the suitable location. The simulation is carried out in MATLAB software for IEEE 14 bus system the graphical output of the devices are as shown below:

6.1. Distributed Power Flow Controller (DPFC)

6.1.1. Real And Reactive Power With And Without DPFC

Simulation for the Distributed Power Flow Controller was performed in IEEE 14 bus system. When Distributed Power Flow Controller is used the real power increases and the reactive power is maintained throughout. The output waveform of the real and the reactive power with and without DPFC are as shown in Figure 9.

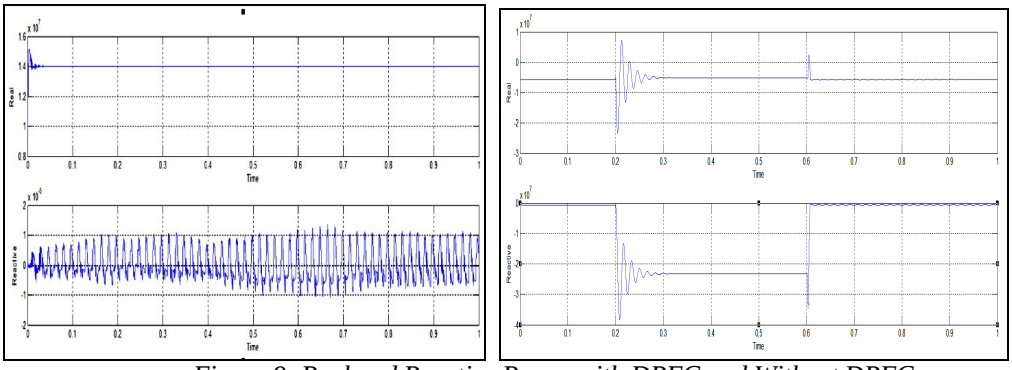

Figure 9: Real and Reactive Power with DPFC and Without DPFC

6.1.2. Voltage And Current With and Without DPFC

Simulation for the Distributed Power Flow Controller was performed in IEEE 14 bus system. The voltage and the current waveforms are observed and it is noted that the fault occurs from 0 secs and ends at 0.04 secs. The output waveform for voltage and the current with and without DPFC are as shown in the Fig 10.

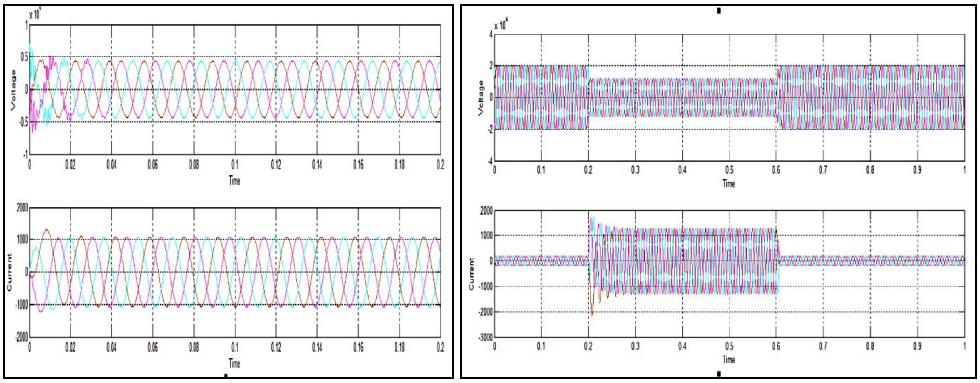

Figure 10: Voltage and Current with DPFC and Without DPFC

6.2. Improved Power Quality Controller (IPQC)

6.2.1. Real and Reactive Power With and Without IPQC

Simulation for the IEEE 14 bus system with Improved Power Quality Controller and the real and reactive power waveforms are as shown below. It can be noted that the reactive power increases and hence the fault will be rectified only after a long duration. Hence the efficiency is less compared to the IEEE system with Improved Power Quality Controller.

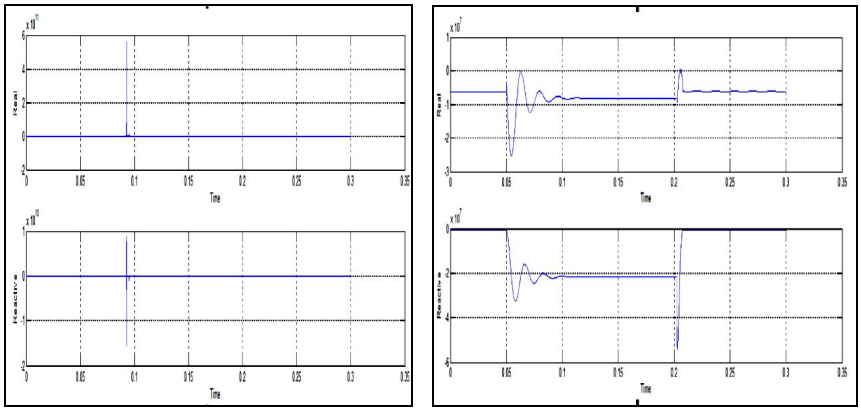

Figure 11: Real and Reactive Power With and Without IPQC

6.2.2. Voltage and Current With and Without IPQC

Simulation for the IEEE 14 bus system was performed with Improved Power Quality Controller. The voltage and the current waveforms are observed and it is noted that the fault occurs from 0.090 secs and ends at 0.095 secs that occurs in the system remains for a long duration of time. The voltage and the current waveform are as shown in the Figure 12.

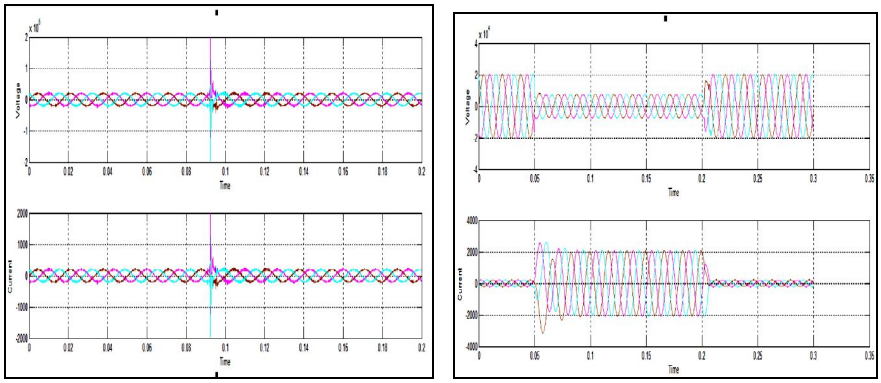

Figure 12: Voltage and Current With and Without IPQC

6.3. Unified Power Flow Controller (UPFC)

6.3.1. Real and Reactive Power With and Without UPFC

Simulation for the IEEE 14 bus system with Unified Power Flow Controller and the real and reactive power waveforms are as shown below. It can be noted that the reactive power increases and hence the fault will be rectified only after a long duration. Hence the efficiency is less compared to the IEEE system with Unified Power Flow Controller.

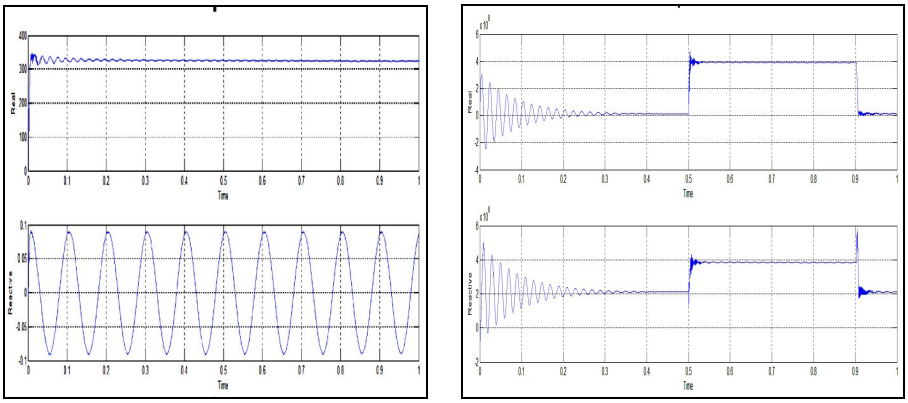

Figure 13: Real and Reactive Power With and Without UPFC

6.3.2. Voltage and Current With and Without UPFC

Simulation for the IEEE 14 bus system was performed with Unified Power Flow Controller. The voltage and the current waveforms are observed and it is noted that the fault occurs from 0 secs and ends at 0.05 secs that occurs in the system remains for a long duration of time. The voltage and the current waveform are as shown in the Figure 14.

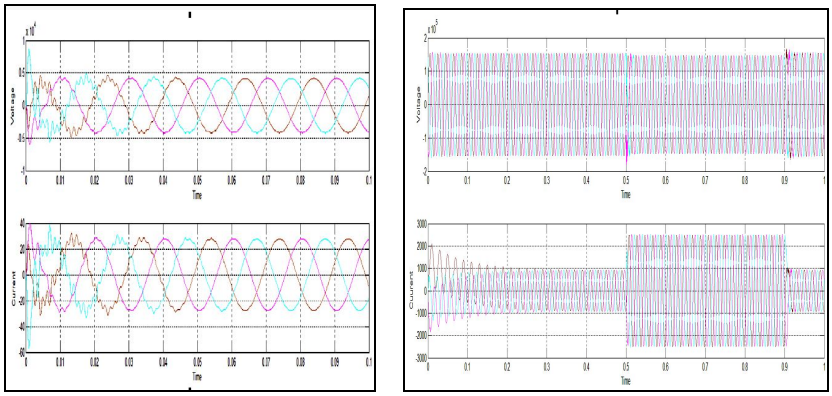

Figure 14: Voltage and Current With and Without UPFC

7. Tabulation

FACTS devices, i.e. Unified Power Flow Controller, Improved Power Quality Controller and Distributed Power Flow Controller are implemented along the IEEE 14 bus system. The FACTS devices are utilized in 14 bus systems to measure voltage, current, real and reactive power for each and every bus. Optimal location of the FACTS devices is decided based on all these values.

Bus	DPFC				UPFC				IPQC			
	V	I	Real	Reactive	V	I	Real	Reactive	V	I	Real	Reactive
1	1.85×10^{4}	410	9×10^{6}	6.6×10^{6}	1.5×10^{5}	1600	1.5×10^{7}	3.5×10^{8}	2×10^{4}	240	7×10^{6}	1×10^{5}
2	4360	100	5×10^{5}	2×10^{5}	1.15×10^{4}	180	2.8×10^{6}	1.5×10^{6}	5000	40	2.5×10^{5}	1.5×10^{5}
3	4400	100	5×10^{5}	1.7×10^{5}	2800	28	1.15×10^{5}	5.75×10^{-4}	1×10^{4}	100	2×10^{5}	1×10^{5}
4	1100	300	3.2×10^{5}	3.6×10^{5}	1.27×10^{5}	750	0.5×10^{7}	1.4×10^{8}	1×10^{5}	100	0.5×10^{7}	1×10^{6}
5	3×10^{5}	600	2.77×10^{7}	3.5×10^{5}	2000	20	6.5×10^{4}	3×10^{-4}	6000	600	2×10^{6}	0.5×10^{7}
6	3×10^{4}	300	1.4×10^{7}	0.5×10^{-5}	2×10^{4}	4.6×10^{5}	2×10^{4}	4.6×10^{5}	4×10^{4}	600	2.5×10^{7}	0.5×10^{7}
7	7800	2400	2.85×10^{7}	2×10^{6}	1.5	150	325	0.1	4×10^{4}	400	1.5×10^{7}	4×10^{-9}
8	7800	4.0	200	4.5×10^{7}	1.5	100	325	1×10^{-11}	1×10^{4}	250	3×10^{7}	2×10^{6}
9	7800	2440	2.9×10^{7}	1.9×10^{6}	1.5	150	325	2×10^{-12}	1×10^{4}	4	0.5×10^{4}	5×10^{4}
10	7800	820	2.62×10^{6}	9.28×10^{6}	4000	0.04	248	0.1	1×10^{4}	2300	2.9×10^{7}	2×10^{6}
11	7800	78	9.2×10^{5}	1×10^{-7}	4000	3.4	2×10^{4}	6743	8000	80	10×10^{5}	5×10^{5}

12	4000	1000	3.7×10^{6}	6×10^{6}	1000	10	1.5×10^{4}	3.6×10^{5}	1×10^{4}	80	2×10^{5}	4×10^{-3}
13	1.85×10^{4}	185	5×10^{6}	0.25×10^{-6}	1000	0.5	8×10^{-4}	766	2.5×10^{4}	250	6×10^{6}	1×10^{-9}
14	7800	2400	2.6×10^{7}	1.175×10^{7}	4000	28	1.7×10^{5}	150	8000	2300	2.6×10^{7}	13×10^{6}

Table 1: Readings of FACTS Devices along 14 Bus Systems

FAULT TIME IN WITH FACTS DEVICE		
DEVICE	**STARTING**	**ENDING**
DPFC	0	0.04
UPFC	0	0.05
IPQC	0.090	0.095

Table 2: Fault Time In With FACTS Device

Fault time in FACTS device are found out and the starting and ending time of the fault are as mentioned in table 3. It can be noted that the fault that the fault starts from and ends at .04 for DPFC where as in UPFC it is from 0 to 0.05 which is comparatively higher than UPFC hence DPFC gives better efficiency than UPFC. IPQC has its starting time from 0.090 and ends at 0.095. IPQC has lower duration of fault but occurs after a long time compared to the other devices. Hence its efficiency is lower than UPFC and DPFC. The higher efficiency is give by DPFC

FAULT TIME WITHOUT FACTS DEVICES		
DEVICE	**STARTING**	**ENDING**
DPFC	0.2	0.6
UPFC	0.5	0.9
IPQC	0.05	0.2

Table 3: Fault Time In Without FACTS Device

BUS NO.	**DPFC**	**UPFC**	**IPQC**
1	11th bus	9th bus	13th bus
2	13th bus	8th bus	7th bus
3	6th bus	3rd bus	12th bus
4	3rd bus	5th bus	9th bus
5	2nd bus	7th, 10th bus	1st, 3rd bus
6	5th bus	7th, 10th bus	1st, 3rd bus
7	4th bus	14th bus	2nd bus
8	9th bus	13th bus	11th bus
9	7th bus	11th bus	4th bus
10	12th bus	12th bus	8th, 10th bus
11	1st bus	6th bus	8th, 10th bus
12	10th bus	2nd bus	13th bus
13	14th bus	4th bus	5th, 6th bus
14	8th bus	1st bus	5th, 6th bus

Table 4: Placement of FACTS Devices

The placement of the devices along the IEEE 14 bus system is as shown in the table 5. The placement of the devices depends upon the following factors, i.e. voltage, current, real and reactive power and also depends upon the time period in which the fault gets rectified.

8. Conclusion

In this paper appropriate model development of flexible ac transmission systems (FACTS) shunt-series controllers for multiobjective optimization is shown and also a multiobjective optimization methodology to find the optimal location of FACTS shunt-series controllers is presented. In large power systems, the selection of proper location for FACTS devices is the first and important step in designing FACTS controllers. Based on the FACTS locations, the design and coordination of their controllers can be carried out. This project presents one of the Bang-Bang Controller to seek the optimal location of FACTS devices in a power system using MATLAB/Simulink. The proposed algorithm is tested on IEEE 14 bus power system for optimal location of multi-type FACTS devices and results are presented.

The optimal location of IPFC, DPFC and UPFC are found out and the comparison is made among these three FACTS devices. The higher efficiency among these devices are found out. It is observed that DPFC has better efficiency when compared with UPFC and IPQC. It is also noted that UPFC has better efficiency than IPQC. The simulation results on IEEE test networks with up to 14 buses show that the FACTS placement toolbox is effective and flexible enough for analyzing a large number of scenarios with mixed types of FACTS to be optimally sited at multiple locations simultaneously.

9. References

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