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# Low Power Pulse Triggered Flip-Flop for Memory Applications

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***Abstract:***
*The choice of flip-flop technologies is an essential importance in design of VLSI integrated circuits for high speed and high performance CMOS circuits. The main objective of this project is to design a Low-Power Pulse-Triggered flip-flop. Flip-flops are the major storage elements in all SOC's of digital design. They accommodate most of the power that has been applied to the chip. Flip-flop is one of the most power consumption components. It is important to reduce the power dissipation in both clock distribution networks and flip-flops. Here a kind of conventional pulse-triggered flip-flop called Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop is designed. The comparison of low power pulse triggered flip-flops between DET, SVL logics is carried out and the best power -performance is obtained which is implemented as a memory application. The simulation results are obtained with Tanner simulation tool.*

***Key words:*** *Flip-flop, SCCER, DET, SVL*

## 1. Introduction

Flip-Flops and latches are the basic elements for storing information. One latch or Flip-Flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their input change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even. There are basically four main types of latches and flip-flops: SR, D, JK, and T. The major differences in these flip-flop [13] types are the number of inputs they have and how they change state. For each type, there are also different variations that enhance their operations. Figure 1(a), (b) illustrates the difference between positive edge triggered flip flop and an active high latch. As it can be seen in this figure, possible changes of input can be seen at the output of the latch while it is transparent

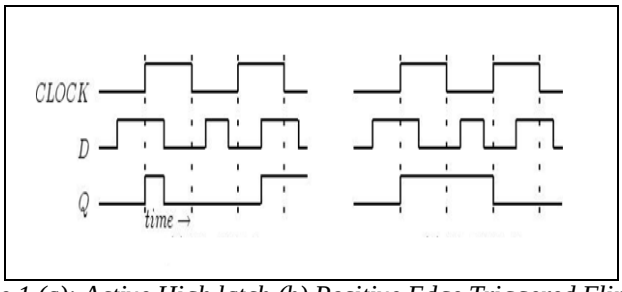


*Figure 1 (a): Active High latch (b) Positive Edge Triggered Flip-Flop*

The performance of a flip-flop is measured by three important timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They reflect in the system level performance of the Flip-Flops [5]. Setup time and hold time define the relationship between the clock and input data as shown in the Figure 1(c).Setup time and hold time describe the timing requirements on the D input of a Flip-Flop with respect to the Clk input. Setup and hold time define a window of time which the D input must be valid and stable

in order to assure valid data on the Q output. Setup Time (Tsu) Setup time is the time that the D input must be valid before the Flip-Flop samples. Hold Time (Th**)** – Hold time is the time that D input must be maintained valid after the Flip-Flop samples.
Propagation Delay (Tpd) – Propagation delay is the time that takes to the sampled D input to propagate to the Q output.

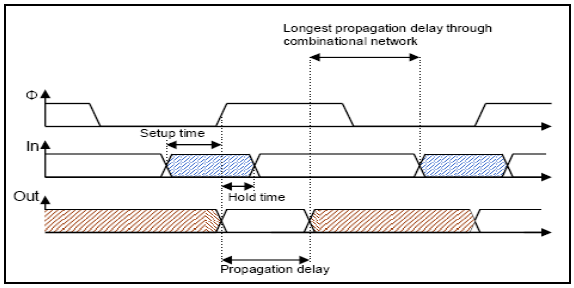


*Figure 1(c): Timing Diagram*

**2. Existing Flip-Flop Design**

*2.1. Single Ended Conditional Capturing Energy Recovery*
Single Ended Conditional Capturing Energy Recovery Flip-Flop is one kind of Energy Recovery Flip-Flop. Where Energy Recovery is a technique developed for low power digital circuits, the energy recovery circuit achieves low energy dissipation by restricting current to flow across device with low voltage drop and by recycling the energy stored on their capacitors by using an AC type supply voltage. This SCCER Flip-Flop uses the Conditional Discharge Technique.

2.1.1. Operation of SCCER
SCCER is the refined Low power pulse triggered flip-flop the circuit diagram of SCCER is shown in the below figure 2.This SCCER Flip-Flop uses the Conditional Discharge Technique. In this technique, the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH and thus the name conditional discharge technique. In this scheme, an NMOS transistor controlled by QB is inserted in the discharge path of the stage with high switching activity. When the input undergoes a Low-to-High transition the output Q changes to high and QB to low. This transition at the output switches off the discharge path of the first stage to prevent it from discharging.
In this design, a weak pull up transistor P1 is employed in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge path contains NMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

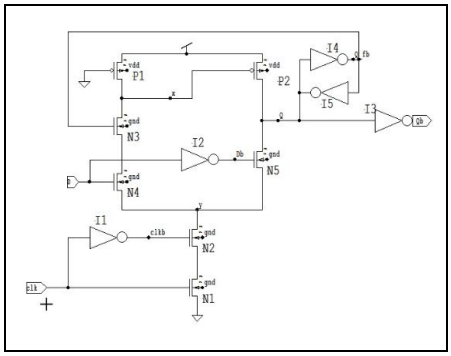


*Figure. 2: Circuit diagram of SCCER*

When the clock pulse is 1 and the data is 0 the output is 0. Here the transition occurs only if the clock pulse is 1 and data is 1, only then the input to output transition occurrence takes place. The keeper logic (back-to-back inverters I7 and I8 is replace by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X.The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1.A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

*3.1. SCCER with Self Controllable Voltage Level Circuit Logic (SVL)*
The SVL circuit can reduce stand by leakage power of CMOS logic circuits with minimal overheads in terms of chip area and speed. In the operating Mode, it provides high-Speed Operation for load circuits. In the Stand-by Mode it provides, minimum Stand-by power, data retentions and high noise immunity.

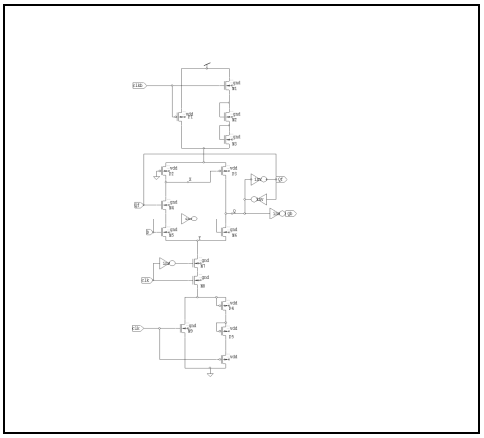

*Figure 3: Circuit Diagram for SCCER with SVL logic*

The SVL logic is added to the upper part and the lower part of the modified SCCER circuit.The modified SCCER circuit is decreased in transistor count when compared to figure 4.

*3.2. Double Edge Triggering On Sccer*

It is using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. For example, the clock branch shared implicit pulsed flip-flop (CBS-ip DEFF) [8] & [13], is a double edge triggered flip-flop. Double clock edge triggering method reduces the power by decreasing frequency in equation.

Most of the flip flops are designed to operate in single clock edge i.e. either in positive edge or negative edge. In double edge triggering [8] the flip flop is made to operate in both clock edges. With this method the opposite clock edge will not be wasted and speed of operation is increased. In double edge triggering flip flop in that figure 8.1 the number of clocked transistor is high than single edge triggering flip flop. This method is preferable to the circuits which consist of reduced number of clocked transistors [14]. In dual edge triggering the flip flop is triggered in both edges of clock pulses. So the half of the clock operating frequency is enough and it will reduce the power consumption.

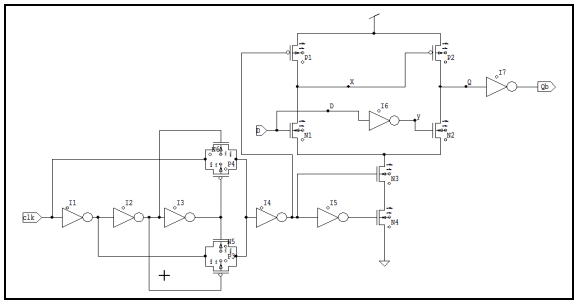

*Figure 4: Dual-Edge Triggered with SCCER*

Instead, applying the clock signal to the flip flop the dual pulse is applied using dual pulse generator scheme [15] shown in figure 4. The flip flop will evaluate the output in both edge of the clock.When *clk=1* the upper TG is ON and lower TG if OFF the output *pulse=0*. When the *clk* transit from 1_0 suddenly the *pulse=1*. That is the output of the inverter I3 is '1' after three inverter delay. Similarly, When *clk=0* the lower TG is responsible to produce the *pulse* at negative edge of the clock. The pulse generator is interfacing with the DETSCCER flip flop we get the first proposed flip flop called *double edge triggered SCCER (DET-SCCER)* as shown in figure 4. The pulse generator circuit is the external circuit it may drive one or more flip flop. Whenever the pulse is high the *q* output follows the *d* input. The pulse is applied to the input of the inverter I2 instead of clock. The working principle is same as the SCCER.

**4. Implementation in Memory Cell Design**

The Circuit diagram of 10T SRAM cell is shown in the figure 5.Here the inputs are WWL, WBL, RWL and RWL_N and the outputs are WBL_N and RBL. Where WWL means write word line, WBL is the word bit line, RWL is the read word line and RWL_N is the inversion of read word line, WBL_N is the inversion of write bit line and RBL is read bit line. When an input of WWL and RWL is given as 1 and WBL and RWL_N is given as 0 the output obtained for WBL_N as 0 and RBL as 1 correspondingly.

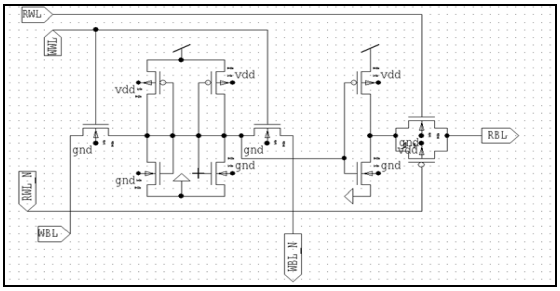


*Figure 5: Circuit Diagram for 10T SRAM cell*

The Circuit diagram of 10T SRAM cell is shown in the figure 6.Here the inputs are WWL, WBL, RWL and RWL_N and the outputs are WBL_N and RBL. Where WWL means write word line, WBL is the word bit line, RWL is the read word line and RWL_N is the inversion of read word line, WBL_N is the inversion of write bit line and RBL is read bit line. When an input of WWL and RWL is given as 1 and WBL and RWL_N is given as 0 the output obtained for WBL_N as 0 and RBL as 1 correspondingly.

*4.1. Read Circuit in the Memory Block*

As shown in Fig.6 DFFs are serially connected to implement a shift-register and the 8 word lines are activated by the shift-register row-by-row. The read bit lines (RBL) then provide the configuration data to the shadow SRAMs. Conventional FPGAs use one SRAM cell to control a reconfigurable switch. However, reconfiguration requires access of the local 10T SRAM block, which leads to a delay overhead. To hide this delay, we use the shadow SRAM scheme which shows Read circuit in the memory block.

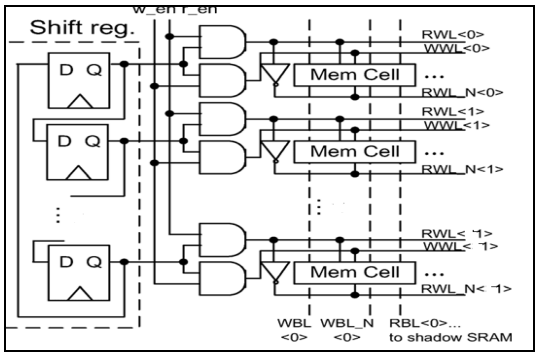


*Figure 6: Block diagram for read circuit cycle*

The circuits operates in simple sense .Here the inputs are the D , clk, w_en and r_en and the outputs are RWL,WWL,RWL_N and WBL respectively. When D, clk, w_en and r_en is given as 1 the outputs obtained is for RWL and WWL is 1 and for RWL_N and WBL it's 0.

- **Write operation**: storing new information into memory.
- **Read operation**: transferring the stored information out of the memory.

*4.2. Write Operation*

When the input to the B is given and r/w is given zero i.e(r/w=0) the first AND gate is enabled and the data in the line B is written into the memory cell. All the three inputs of first AND gate is 1 and the gate is enabled and the data is being written into the memory.

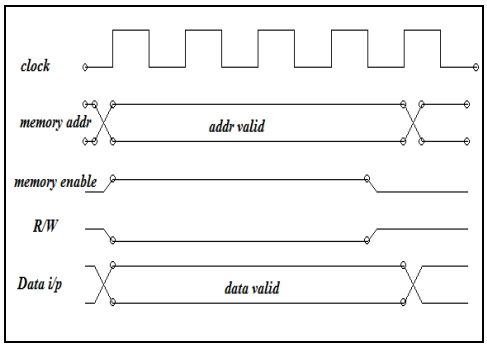


*Figure 7: Timing Diagram of Write Port Cycle*

**5. Benchmark Mark Circuits**

Benchmark circuit is the standard circuit s which is available already in order to check the functionality of the circuit and to test the working of the given circuit .In bench mark circuits we have two different types of circuits,

- Sequential Benchmark circuit.
- Combinational Benchmark circuit.

*5.1. Sequential Benchmark Circuit*

The sequential benchmark circuit is applicable to check the synchronous based circuit i.e. flip-flops etc. Here in sequential circuit, the output depends not only on the present input but also on the past output. Memory unit is required.

*5.2. Combinational Benchmark Circuit*

The combinational based circuits output is based on the present state input and it does not require any memory unit.Our motive is to test the SCCER flip-flop with the Self voltage controlled logic circuit (SVL), since it is based on flip-flop it comes under the a sequential based benchmark circuit. Here i have taken as an example a S27 benchmark circuit. The circuit is shown in the below figure, consists of three D flip-flop where the SCCER based SVL logic is put under test using the benchmark circuit. It consists of 4 inputs and the output is inverted and OUT is obtained and Figure 8 is shown in the block diagram of the S27 circuit.

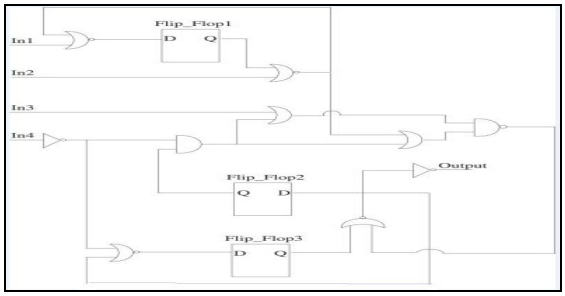


*Figure 8: Block Diagram of the S27 Benchmark Circuit*

The block diagram of an SCCER with SVL logic circuit can be build with the help of AND, OR, NOR, NAND logic gates where, NAND and NOR is said to be universal gates**.**

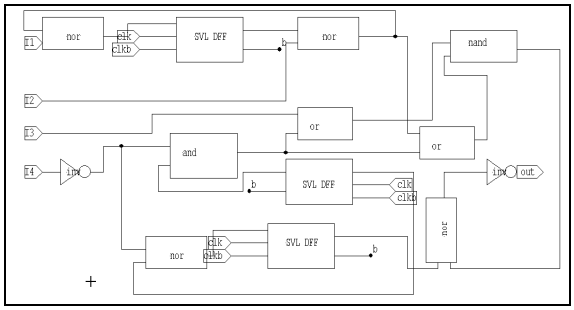


*Figure 9: Block Diagram of the SCCER Implementation*

Figure 9 is shown in the block diagram of SCCER implemented on bench mark circuit. The power consumption is obtained when compared to the SCCER circuit and hence it proves that the obtained output is tested and the correct output is thereby produced by using the S27 benchmark circuit.

**6. Simulation Results**

*6.1. Simulation Result for SCCER*

The waveform of SCCER is shown in the figure 10.

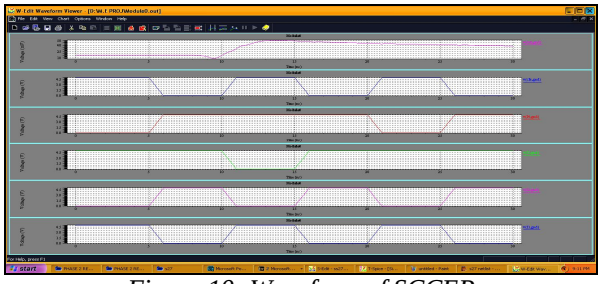

*Figure 10: Waveform of SCCER*

*6.2. Simulation Result for SCCER with SVL Logic*

The waveform of SCCER with Self Voltage controllable logic (SVL) is shown in the figure 11.

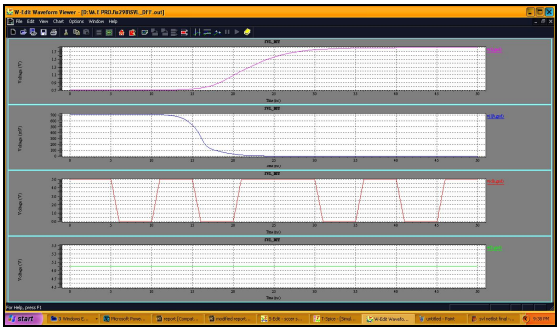

*Figure 11: Waveform of SCCER with SVL logic*

*6.3. Simulation Result for SCCER with Detlogic*

The waveform of SCCER with Dual Edge Triggered logic (DET) is shown in the figure 12.

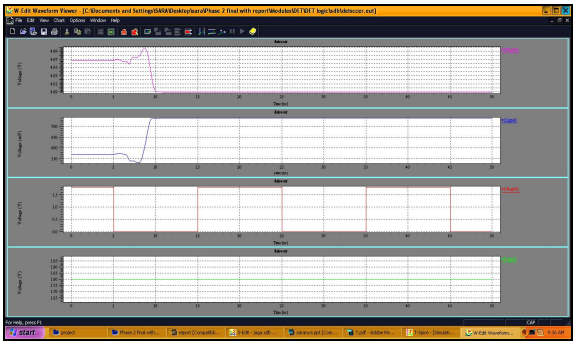

*Figure 12: Waveform of SCCER with DET logic*

*6.4. Simulation Result for Waveform of 10t SRAM Cell*

The waveform of 10T SRAM Cell is shown in the figure 13.

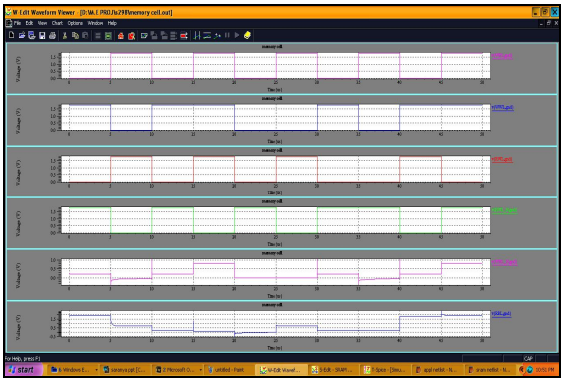

*Figure 13: Waveform of 10T SRAM cell*

*6.5. Simulation Result for Waveform of 8 Bit Memory Cell*

The Waveform of 8 bit memory cell design is shown in figure 14.Here, the inputs are the D, clk, w_en and r_en and the outputs are RWL,WWL,RWL_N and WBL respectively.

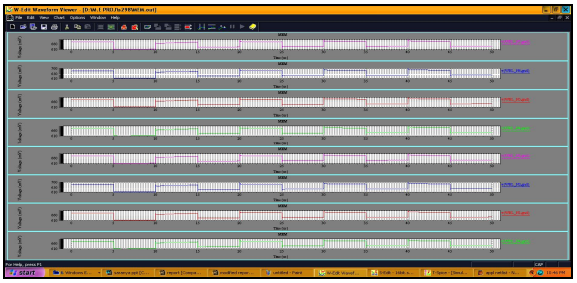

*Figure 14: Waveform of 8 Bit Memory Cell*

*6.6. Simulation Result for SCCER Implemented In Benchmark Circuit*

The power consumption is obtained when compared to the SCCER circuit and hence it proves theat the obtained output is tested and the correct output is thereby produced by using the S27 benchmark circuit shown in the figure 15.

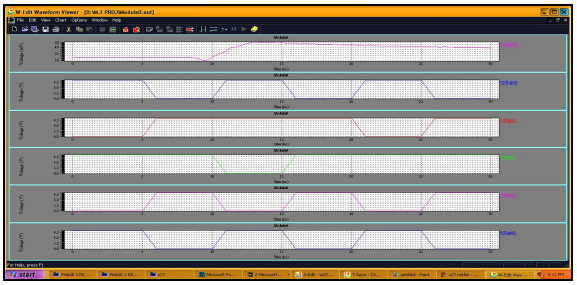

*Figure 15: Waveform of SCCER in benchmark circuit*

**7. Power Comparison Table for Different Flip-Flops**

The power comparison for different flip-flops is discussed and tabulated as shown in the table 1.

| FLIP-FLOP | AVERAGE POWER (m.watts) | MAXIMUM POWER (m.watts) | MINIMUM POWER (m.watts) |
|---|---|---|---|
| SCCER | 0.691 | 0.423 | 0.0067 |
| SCCER WITH SVL LOGIC | 0.726 | 0.6485 | 0.01447 |
| SCCER WITH DET LOGIC | 0.544 | 0.1402 | 0.0015 |

*Figure 1: Power Comparison Table*

*7.1. Power Comparison Chart for Different Flip-Flops*

The power comparison chart for different flip-flops is shown in the figure 16

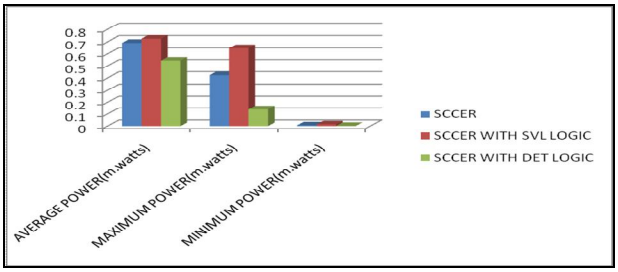


*Figure16: Power Comparison Chart*

**8. Conclusion**

In this paper, the various Flip flop design like SCCER and Proposed flip-flop design with SVL and DET Logic's were discussed .These flip-flop were been designed in Tanner tool and the results and waveforms are also obtained. The comparison table is also added to verify the designed methods. Even though, when the circuit is in idle condition the circuit consumes some power which is said to be leakage power. Here, we devise a novel low-power pulse-triggered FF design and the circuit is tested with the help of S27

benchmark circuit. This SCCER with SVL logic circuit is implemented and designed for a memory cell design with the help of SRAM cell. Simulation results indicate that the proposed design excels in performance indexes such as power and area.

**9. Acknowledgement**
We Thank to Dr. S. V. Saravanan, Principal, Christ The King Engineering College, Coimbatore for their Contribution in this work.

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