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A 10 Bit Low Power Current Steering Digital to Analog Converter Using 45 nm CMOS and GDI Logic

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Abstract:
In this paper, The Design and Implementation low power Current Steering Digital to Analog Converter in 45 nm technology using CMOS and GDI Logic using TANNER TOOL, V15 is presented. This architecture gives the most optimized results in terms of speed, resolution and power. The designed 10-bit DAC operates with two supply voltages, 1 V and 3.3 V. The simulation result shows the transient analysis waveforms of current Steering DAC. The average power dissipation 1.40 mW using GDI Logic and 2.63 mW using CMOS Logic. The tool used for simulation is Tanner S-Edit and T-Spice. Comparisons show that using GDI logic it consists low power as compare to the CMOS logic.

Key words: *CMOS , Current-Source, TANNER TOOL*

1. Introduction

GDI Logic in CMOS technologies has been used for low power applications; also submicron processes have allowed CMOS to achieve low power. In a wireless system the quality of the communication link is main criteria, for long distance transmission it is necessary to convert analog signal into digital signal at input side, same as convert digital signal into analog signal at output side. In this paper current steering DAC using 45nm technology are presented. CMOS technology dissipates less power compare to other design. CMOS architecture can be easily scaled down for the major three factors: 1) Area 2) Speed 3) Power [7].

1.1. GDI Technology

Energy performance requirements are forcing designers of next-generation systems to explore approaches to lease possible power consumption. Power consumption is majorly affected by power supply voltage. Scaling of power supply voltage is major factor to reduce power Consumption. The technique to achieve ultra-low power is to operate the circuit with supply voltage less than threshold voltage. The region where supply voltage is less than threshold voltage is called sub threshold region. Ultra-low power consumption can be achieved by operating digital circuits at sub threshold region. Here proposed sub threshold circuit is based on GDI (Gate Diffusion Input) technique. GDI technique allows reducing power consumption, delay, area of the digital circuit while maintaining low complexity of logic design as compared to other CMOS (Complementary Metal Oxide Semiconductor) circuits. [4]

Scaling of power supply voltage is major factor to reduce the power consumption. Sub threshold operation has gained a lot of attention due to ultralow-power consumption applications requiring low to medium performance. It has also been shown that by optimizing the device structure, power consumption of digital sub threshold logic can be further minimized while improving its performance.

To accomplish this task circuit with lower frequency should be operated in the weak inversion region or sub threshold region. Sub threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub threshold operation.

The architectural technique described in this paper suggests a design to minimize area and capacitance by using Gate Diffusion Input (GDI) multiplexer. As feature size of the CMOS (Complementary Metal Oxide Semiconductor) technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip.

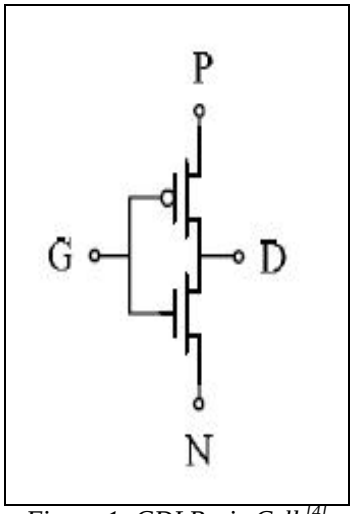


Figure 1: GDI Basic Cell [4]

N	P	G	D	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table 1: Some logic functions that can be implemented with a single GDI cell [4]

The GDI method is based on the simple cell shown in Fig 1. A basic GDI cell contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N and D may be used as either input or output ports, depending on the circuit structure. Simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and PTL design techniques. Multiple-input gates can be implemented by combining several GDI cells. The buffering constraints, due to possible VTH drop, are described in detail in, as well as technological compatibility with CMOS and SOI. [4]

2. DAC Architecture

The Segmented Current- Steering architecture is shown in Figure 2. The architecture is a combination of two parts, the MSB is going through the thermometer coded architecture and the LSB is going through the Binary Weighted architecture. The input n-digital codes are sent into buffer to get enough amplitude and synchronized with the clock. Then the (N-B) bits MSBs are decoded by thermometer decoder to reduce the glitch and achieve well matching of current sources. The B Bits LSB is given to the LSB Delay. The signal after decoding will be controlled by latch to put into current switch array or not, which decides the output current direction.

The binary weighted architecture is very simple, but less accurate. The thermometer coded architecture is very accurate, but the circuit complexity is very high, and is comparatively slow.

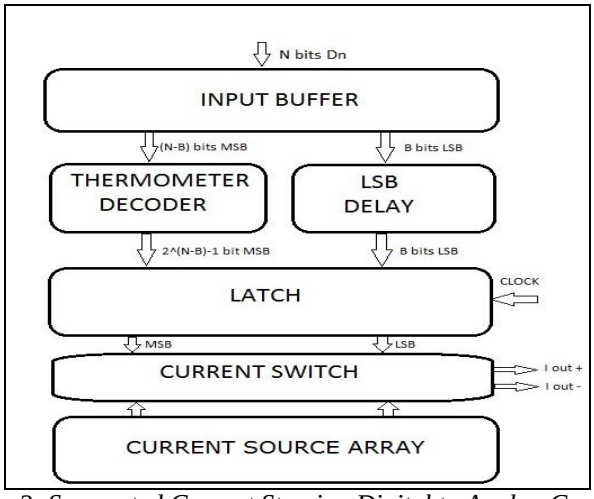


Figure 2: Segmented Current Steering Digital to Analog Converter

The segmented architecture is the combination of binary weighted architecture and thermometer coded architecture. Thus, it combines the good things and removes bad things. Here, the 10-bit digital input is divided into two parts, 7-bit LSB and 3-bit MSB. The 7-bit LSB is implemented using binary weighted architecture, while 3-bit MSB is implemented using thermometer coded architecture.
The 7-bit LSB are implemented using binary weighted architecture, thus requires only seven current sources. The 3-bit MSB is implemented using thermometer coded architecture, which requires 7 current sources. So, total 14 current sources are needed to implement 10-bit DAC, which is quite low as compared to fully thermometer coded architecture. The binary weighted current source is also similar, but to compensate the delay of row-column decoder in thermometer coded current sources, the dummy combination logic is provided, which ensures that the digital input in both binary weighted and thermometer coded current source reaches at the switches at the same instant.
The main building blocks in this prototype are the unit current cells, Latches and the thermometer decoder design.

3. Cascode Current Source with Thick Oxide Layer Cascoded Switches and Latches

The current cell configuration used here is a thick oxide layer transistor for the switch Cascode [05]. The low voltage headroom problem in 45-nm technology can be solved using a thick oxide layer transistor for the switch cascade [5]. This thick oxide layer transistor can operate with a higher supply voltage up to 3.3 V. Hence the voltage headroom is increased significantly. Care should be taken to prevent the voltage at the drain of the switching transistors from increasing beyond the maximum supply voltage in 45-nm technology i.e. beyond 1 V. Methods used to keep the voltage at the drain of the switching transistor below 1 V are explained below. The drain voltage of the switching transistor can be held constant by using a voltage regulator. The voltage regulator (Zener diode) is connected in parallel such that the voltage at the drain remains below 1 V, but its unknown leakage current flows through the output of the DAC. The output current of the current steering DAC should be proportional to the input code. [5]

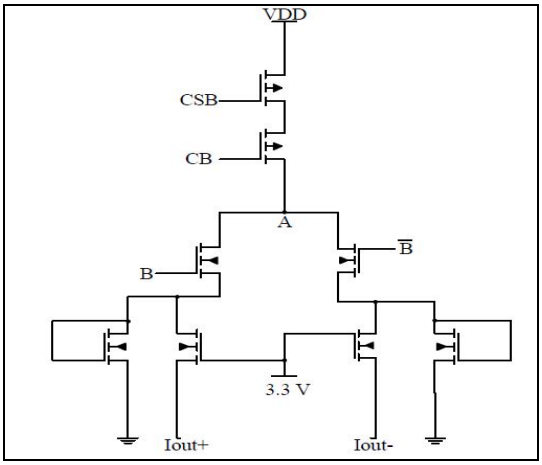


Figure 3: Cascode Current Source with Thick Oxide Layer Cascoded Switches [5]

3.1. CMOS D-Flip Flop Implementation

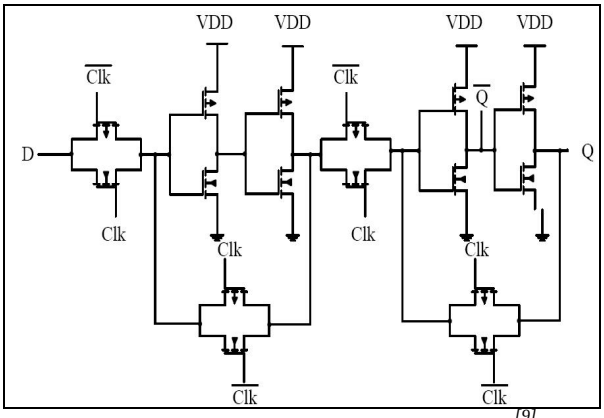


Figure 4: CMOS master slave D flip-flop [9]

There are so many latch configurations. The latches used here are Master Slave configuration D latches implemented in CMOS as shown in figure 4. This is the negative edge triggered configuration. The master slave configuration ensures the elimination of race-around condition.

3.2. GDI D-Flip Flop Implementation

A novel implementation of a GDI DFF is shown in Fig. 5. It is based on the Master-Slave connection of two GDI D-Latches. Each latch consists of four basic GDI cells, resulting in a simple eight-transistor structure. The components of the circuit can be divided into two main categories: [4]

- *Body gates* – responsible for the state of the circuit. These gates are controlled by the Clk signal and create two alternative paths: one for transparent state of the latch (when the Clk is low and the signals are propagating through PMOS transistors), and another for the holding state of the latch (when the Clk is high and internal values are maintained due to conduction of the NMOS transistors).
- *Inverters* (marked by ×) – responsible for maintaining the complementary values of the internal signals and the circuit outputs. An additional important role of inverters is buffering of the internal signals for swing restoration and improved driving abilities of the outputs.

This partition to categories can be helpful for understanding of circuit operation and optimization. As can be seen, in body gates the transmission of the signal is performed through the diffusion nodes of the GDI cells. It might cause a swing drop of VTH in the output signals. This problem is solved by the internal inverters in their buffer role. Performance optimization of the proposed circuit can be performed by adjusting the transistor sizes (as sweep parameter in simulation) to obtain a minimal power delay product. This procedure is iterative and contains a sequence of separate size adjustments:

- First, the same scaling factor is obtained for all transistors of the circuit (body gates and inverters).
- Secondly, iterative size optimizations are applied separately to inverters and body gates (mostly by opposite shifting of the scaling factors around the "operation point" found in (a)), while targeting the minimal power-delay product.
- For high load requirements, an additional optimization can be separately performed on the inverter of the Slave latch.

The relatively compact structure of the proposed DFF, containing 18 transistors (with the inverter for complementary value of D), makes it an efficient alternative for obtaining the combination of low area and high performance.[4]

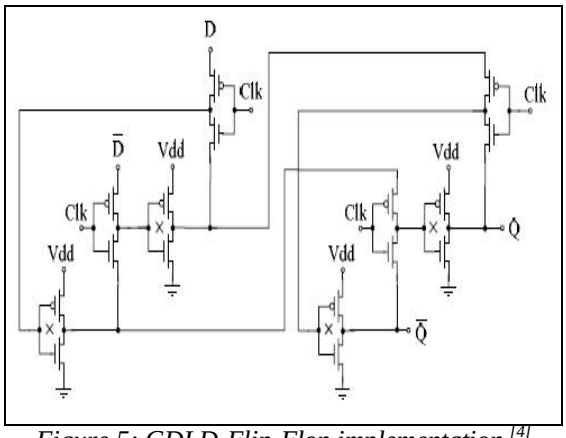


Figure 5: GDI D-Flip-Flop implementation [4]

4. Binary-to-Thermometer Decoder

The Binary to thermometer decoder is used to convert N bit binary input into $2^N - 1$ Thermometer coded output lines.

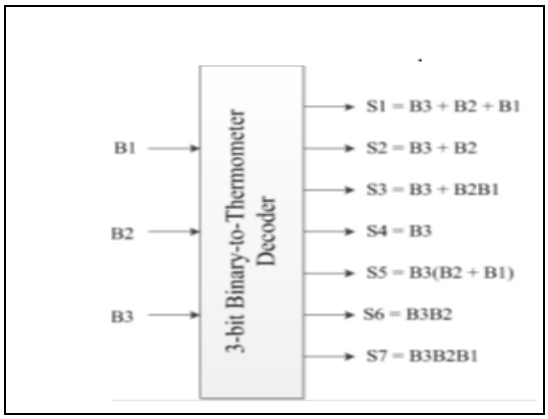


Figure 6: 3-bit Binary to Thermometer Decoder

In this implementation, 3 bits are converted into the 7 bit thermometer code. The 3 bit binary to 7 bit thermometer bit decoder are shown in figure. It requires two input and three input AND gate and OR gate for Implementation. This logic gates are Implemented using GDI Logic. [07] [08]

Figure 7 and 8 shows reconstructed sine wave output of 10-bit DAC using CMOS and GDI Logic. The sine wave accuracy becomes higher as the resolution increases. Figure 9 and 10 shows the FFT spectrum of sine wave output. the measured SFDR is 40 dB using CMOS and the measured SFDR is 42 dB using GDI Logic.

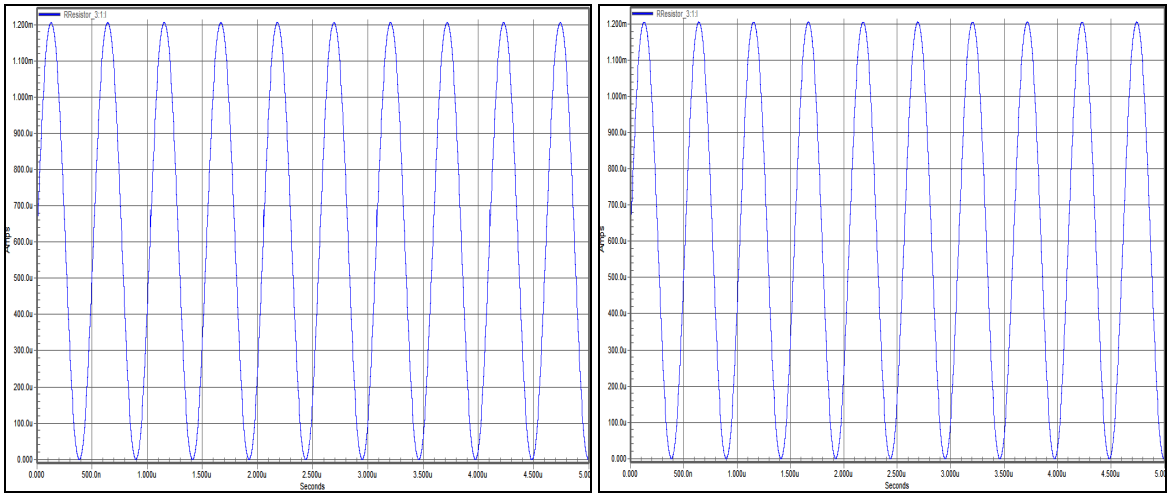
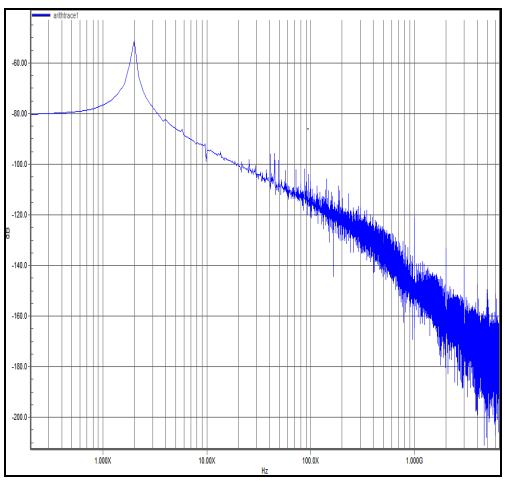


Figure 7: Reconstructed Sine Wave Output of 10-bit Segmented DAC (CMOS)
Figure 8: Reconstructed Sine Wave Output of 10-bit Segmented DAC (GDI)

Figure 11 and 12 shows the DNL and INL plots of 10-bit DAC. As shown, the measured DNL and INL are + 0.41 LSB and + 0.6 LSB using CMOS and the measured DNL and INL are + 0.3 LSB and + 0.4 LSB using GDI Logic, respectively



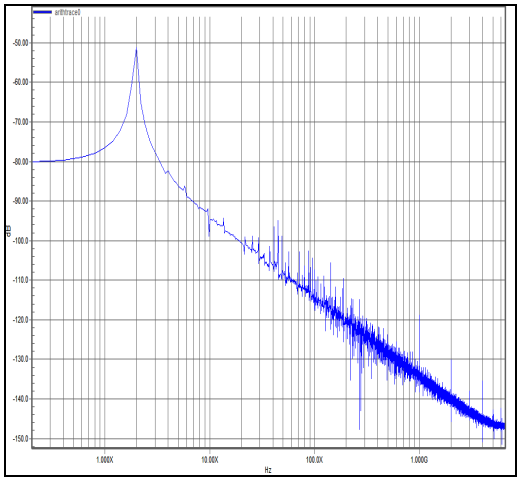
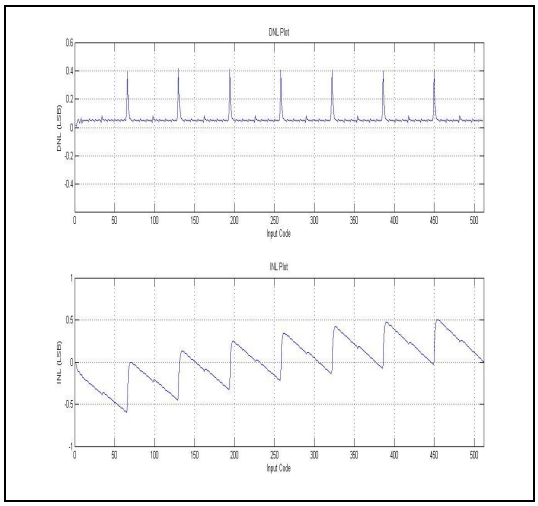


Figure 9: Frequency Spectrum of Sine Wave Output of 10-bit DAC (CMOS)
Figure 10: Frequency Spectrum of Sine Wave Output of 10-bit DAC (GDI)



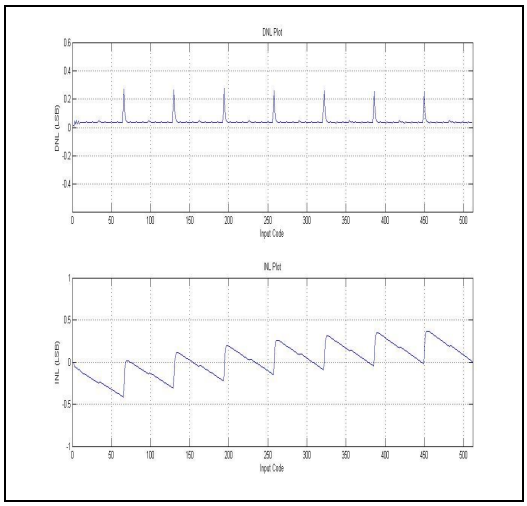


Figure 11: DNL and INL Plots of 10-bit DAC (GDI)
Figure 12: DNL and INL Plots of 10-bit DAC (GDI)

The measured response time of the DAC is 240 ps and the settling time is 69.9 ps using CMOS logic and the measured response time of the DAC is 201.9 ps and the settling time is 60.8 ps using GDI logic. The Signal to Noise Ratio using CMOS and GDI is 70 dB and 65 dB respectively at sampling frequency of 1 GHz.

5. Conclusion

This implemented DAC provides desired level of accuracy with Very low power consumption. After justifying the advantages of segmented current steering architecture, the 10-bit DAC is designed in that configuration using 45-nm CMOS and GDI technology. The DNL and INL are achieved accurate in GDI technology then the CMOS technology. The designed DAC provides high-speed and high-resolution performance with low power consumption. The accuracy of DAC is acceptable for most of the applications. The designed DAC can be used in any applications requiring high speed and high resolution operations, such as digital audio, digital video, HD Television, wireless communication, etc. Table II shows the Comparisons of different performance parameters, Comparisons show that using GDI logic it consumes low power as compared to the CMOS logic.

Parameters	This Implementation (GDI)	This Implementation (CMOS)	[01]	[02]
Resolution	10-bit	10-bit	10-bit	10-bit
Technology	45-nm GDI	45-nm CMOS	90-nm CMOS	130-nm CMOS
Supply Voltage	1 V & 3.3V	1 V & 3.3V	1.2 V & 2.5 V	1.2 V & 3.3 V
Output Current Swing	0 – 1.21 mA	0 – 1.21 mA	10 mA	---
DNL	+ 0.3 LSB	+ 0.41 LSB	+ 0.3 LSB	0.47 LSB
INL	+ 0.4 LSB	+ 0.6 LSB	+ 0.8 LSB	0.46 LSB
SFDR	42 dB at f_s = 1 GHz	40 dB at f_s = 1 GHz	40.09 dB at f_s = 1.25 GHz	72.8 dB At 1 MHz
SNR	65 dB at f_s = 1 GHz	70 dB at f_s = 1 GHz	---	---
Average Power Dissipation	1.40 mW at f_s = 1 GHz	2.63 mW at f_s = 1 GHz	56.65 mW at f_s = 1.25 MHz	4.46 mW
Response Time	201.9 ps	240 ps	-	-
Settling Time	60.8 ps	69.9 ps	--	-
Max. Sampling Frequency	1 GHz	1 GHz	1.25 GHz	200 MHz

Table 2: Summary and Comparison of Simulation Results of 10-Bit DAC Designs

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