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A Survey on Different Architectures Used in Online Self Testing for Real Time System

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Abstract:
On-line self-testing is the solution for detecting permanent and intermittent faults for real-time embedded multiprocessors. This paper basically describes the scheduling and allocation policies of 3 types of On-line Self Testing architectures.

Key words*: components: MPSoC, On-line self-testing, DSM technology*

1. Introduction

Real-time systems are very important parts of our life now a day to day. In the last few decades, we have been studying the time aspect of computations. But in recent years, it has increased exponentially among the researchers and research school. There has been an eye catching growth in the count of real-time systems, being used in domestic and industry production. So we can say that real-time system is a system which not only depends upon the correctness of the result of the system, but also on the time at which the result is produced. The example of the real-time system can be given as the chemical and nuclear plant control, space mission, flight control systems, military systems, telecommunications; multimedia systems and so on all make use of real-time technologies.
Testing is a fundamental step in any development process. It consists in applying a set of experiments to a system (system under test − SUT), with multiple aims, from checking correct functionality to measuring performance. In this paper, we are interested in so-called Black-box conformance testing, where the aim is to check conformance of the SUT to a given specification. The SUT is a “black box” in the sense that we do not have a model of it, thus, can only rely on its observable input/output behavior.

1.1. Online Self Testing

Online self-testing is the most cost-effective technique which is used to ensure correct operation for microprocessor-based systems in the field and also improves their dependability in the presence of failures caused by components aging.

1.2. DSM Technologies

Deep submicron technology means, the use of transistors of smaller size with faster switching rates [2]. As we know from Moore's law the size of transistors are doubled by every year in a system, the technology has to fit those inc in transistors in small area with better performance and low-power [4].

2. Different Architectures used in Online Self Testing in Real Time Systems

2.1. The Architecture Of The DIVA Processing In Memory Chip

The DIVA system architecture was specially designed to support a smooth migration path for application software by integrating PIMs into conventional systems as seamlessly as possible. DIVA PIMs resemble, at their interfaces, commercial DRAMs, enabling PIM memory to be accessed by host software either as smart memory coprocessors or as conventional memory [2]. A separate memory to memory interconnect enables communication between memories without involving the host processor.

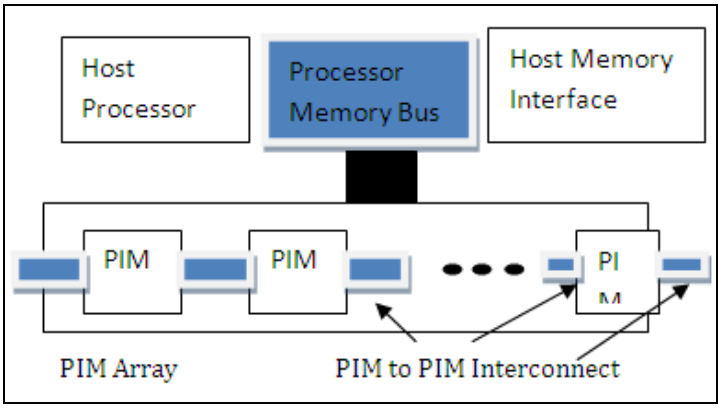

Figure 1: DIVA Architecture

A parcel is closely related to an active message as it is a relatively lightweight communication mechanism containing a reference to a function to be invoked when the parcel is received. Parcels are transmitted through a separate PIM to PIM interconnect to enable communication without interfering with host memory traffic. This interconnect must support the dense packing requirement of memory devices and allow the addition or removal of devices from system.
Each DIVA PIM chip is a VLSI memory device augmented with general purpose computing and communication hardware [3]. Although a PIM may consist of multiple nodes, each of which are primarily comprised of few megabyte of memory and a node processor.

2.2. Chip Multiprocessor Architecture (CMP Architecture)
Chip multiprocessors are also called as multi-core microprocessors or CMPs for short, these are now the only way to build high-performance microprocessors, for a number of reasons [6] limiting acceptance of CMPs in some types of systems.

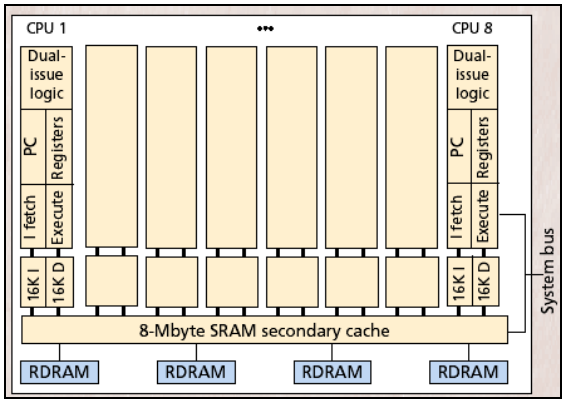

Figure 2: The above figure shows the CMP Architecture [6]

2.3. SCMP Architecture: An Asymmetric Multiprocessor System-On-Chip
This asymmetric multiprocessor can support dynamic migration and preemption of tasks, thanks to a concurrent control of tasks, while offering a specific data sharing solution.
In response to an ever increasing demand for computational efficiency, the performance of embedded system architectures have improved constantly over the years. This has been made possible through fewer gates per pipeline stage, deeper pipelines, better circuit designs, faster transistors with new manufacturing processes, and enhanced instruction level or data-level parallelism (ILP or DLP)[7].
An increase in the level of parallelism requires the integration of larger cache memories and more sophisticated branch prediction systems. It therefore has a negative impact on the transistors' efficiency, since the part of these that performs computations is being gradually reduced. Switching time and transistor size are also reaching their minimum limits.
The SCMP architecture has a CMP structure and uses migration and fast preemption mechanisms to eliminate idle execution slots. This means bigger switching penalties; it ensures greater flexibility and reactivity for real-time systems.

3. Programming Model
The programming model for the SCMP architecture is specifically adapted to dynamic applications and global scheduling methods. The proposed programming model is based on the explicit separation of the control and the computation parts. Computation tasks and the control task are extracted from the application, so as each task is a standalone program. The control task handles the computation task scheduling and other control functionalities, like synchronizations and shared resource management for instance. Each embedded

application can be divided into a set of independent threads, from which explicit execution dependencies are extracted. Each thread can in turn be divided into a finite set of tasks. The greater the number of independent and parallel tasks is extracted, the more the application can be accelerated at runtime.

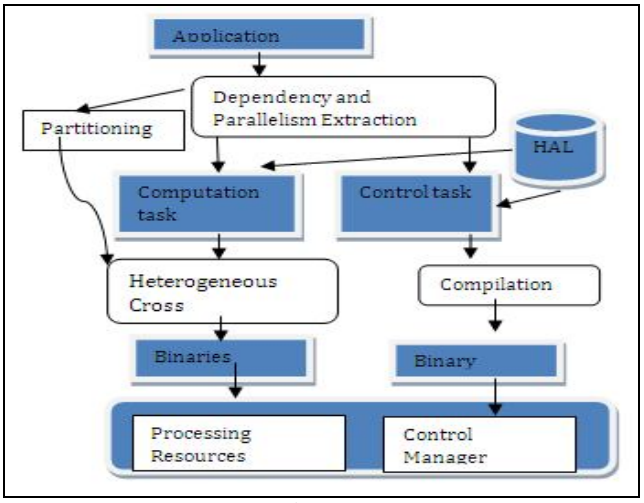

Figure 3

4. SCMP Processing

As shown in Figure 9, the SCMP architecture is made of multiple PEs and I/O controllers. This architecture is designed to provide real-time guarantees, while optimizing resource utilization and energy consumption. The next section describes execution of applications in SCMP architecture.

When the OSoC receives an execution order of an application, its Petri Net representation is built into the Task Execution and Synchronization Management Unit (TSMU) of the OSoC. Then, the execution and configuration demands are sent to the Selection unit according to application status. They contain all of active tasks that can be executed and of coming active tasks that can be pre-fetched.

Scheduling of all active tasks must then incorporate the tasks for the newly loaded application. If a non-configured task is ready and waiting for its execution, or a free resource is available, the PE and Memory Allocation Unit sends a configuration primitive to the Configuration Unit.

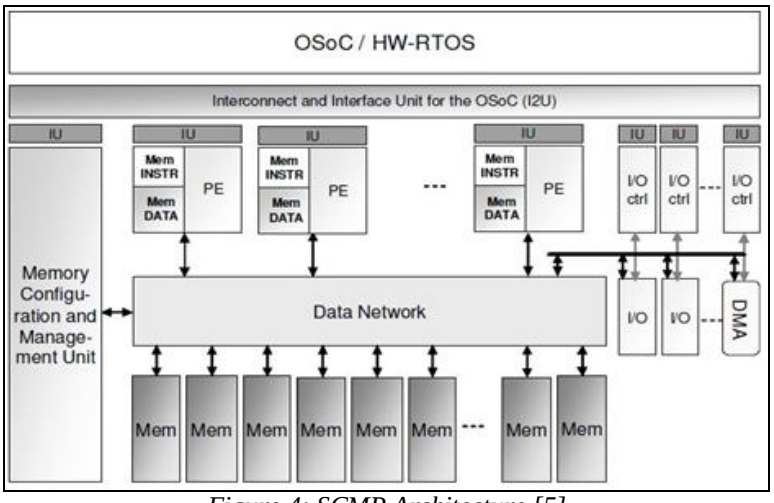

Figure 4: SCMP Architecture [5]

Name Of The Paper	Year of Publication	Author	Limits
The Architecture of the DIVA Processing In Memory Chip	2002	Jeff Draper, Jacqueline Chame, Mary Hall, Craig Steele, Tim Barrett, Jeff LaCoss, John Granacki, Jaewook Shin, Chun Chen, Chang Woo Kang, Ihn Kim, Gokhan Daglikoca	This paper has described a detailed description of DIVA PIM Architecture. This paper having some issues for exploiting memory bandwidth, particularly the memory interface and controller, instruction set features for fine grained parallel operation, and mechanism for address translation.
Chip Multiprocessor Architecture: Techniques to Improve Throughput and Latency	2007	KunleOlukotun, LanceHammond, James Laudon	This work provides a solid foundation for future exploration in the area of defect-tolerant design. We plan to investigate the use of spare components, based on wearout profiles to provide more sparing for the most vulnerable components. Further, a CMP switch is only a first step toward the overreaching goal of designing a defect-tolerant CMP system.
SCMP Architecture: An Asymmetric Multiprocessor System on-Chip for Dynamic Applications	2010	NicolasVentroux, Raphael David	The new architecture, which has been called SCMP, consists of a hardware real-time operating system accelerator (HW-RTOS), and multiple computing, memory, and input/output resources. The overhead due to control and execution management is limited by our highly efficient task and data sharing management scheme, despite of using a centralized control. Future works will focus on the development of tools to ease the programmation of the SCMP architecture.

Table 1: Table of Comparison

5. Conclusion

We have done a survey, how on-line self-testing can be controlled in a real-time embedded multiprocessor for dynamic but non safety critical applications using different architectures. We analyzed the impact of three on-line self-testing architectures in terms of performance penalty and fault detection probability. As long as the architecture load remains under a certain threshold, the performance penalty is low and an aggressive self test policy, as proposed in can be applied to such architecture. Otherwise, on-line self-testing should consider the scheduling decision for mitigating the overhead in detriment to fault detection probability. It was shown that a policy that periodically applies a test to each processor in a way that accounts for the idle states of processors, the test history and the task priority offers a good trade-off between the performance and fault detection probability. However, the principle and methodology can be generalized to other multiprocessor architectures.

6. References

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