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Asynchronizer Based Wireless Sensor System

V. Umasankar
Assistant professor, Department of ECE, Shreenivasa Engineering College, Dharmapuri, India
K. Suganthi
Post Graduate Student, M.E. VLSI Design, Shreenivasa Engineering College, Dharmapuri, India

Abstract:
In this article we propose the design of a GALS wrapper used in Network on Chip (NoC) based on standard cells. The GALS packaging embrace two announcement docks, 4-phase grasp circuits, records buffer and pointer synchronizer. The detailed aim of GALS wrapper is given and the circuits are verified with Verlog-HDL and executed in FPGA. The verified results shows that the wrapper provides fast and consistent communication for the subsystems working with different clocks of NoC.

1. Introduction

The growing difficulty of System on Chip together with the wiring troubles of highly developed IC technologies make Network on Chip capable stand-in for buses and devoted interconnect. The main components of a NoC are switches, which move information from one place to another, and network interface (NI), which execute the interface between IP cores and switches.
The major functions of an NI are data packetization and depacketization, end to-end flow control with scheduling for buffer excess and protocol consistency sandwiched between unified modules. The core idea of this proposal is to devise a synchronizer for wireless sensor networks that can converse with each other efficiently and the data switch will be efficient. Using VHDL language the synchronizer design is developed and experienced with sender and receiver type representation setup to prove the developed synchronizer will resourceful than existed design.

2. Network on Chip

NoC architecture is comprises of routers, Network Interfaces (NI) and links. Links bond the routers collectively and also the routers to the NIs. Network interfaces are located between a router and an IP core and is used as an arbitrator between IP cores and the interconnect network. Routers are in charge for steering data units of transmission from source to destination.

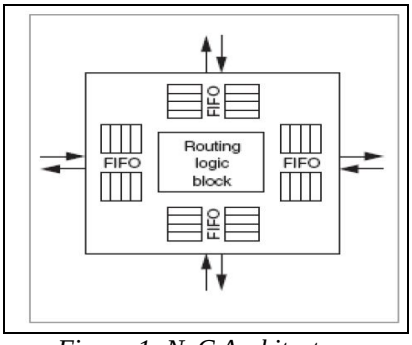

Figure 1: NoC Architecture

In circuit designs, clock skew is an event in synchronous circuit in which the clock signal arrives at diverse apparatus at dissimilar times. This can be caused by numerous different effects, such as wire-interconnect span, temperature variations. As the clock pace of a circuit increases, timing becomes more serious and fewer discrepancy can be tolerated if the circuit is to operate accurately. To overcome the clock skew, EMI and power consumption caused by global clock distribution, NoC supports Globally Asynchronous Locally Synchronous (GALS) style of implementing physically large chips. Each core could be implemented as a separate clock

domain and different cores could communicate among themselves using asynchronous communication through switches. Therefore we should add GALS wrapper to NI, and then it is possible for each core to use its own clock.

3. Network Topology

Network topology is used to connect the routers. It is a significant problem in NoC, in view of the fact that it has considerable effect on effectiveness of on-chip resource usage. The NoC topologies also affect the power of physical criteria. In normal topologies similar to mesh there is a superior power on electrical constraint and clatter sources but it may endure from under-utilization of links and localized jamming. However in asymmetrical topology there are fewer control on corporal issues, instead it is extra efficient in resource usage.

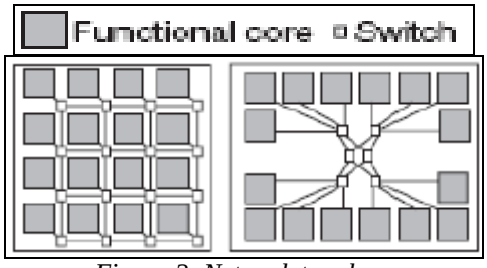

Figure 2: Network topology

4. Operation of NoC system with the application of GALS

Based on the fundamental perception of GALS system Locally Synchronous module (LS) transmit or receive the information asynchronously all the way throughout GALS. This system consists of grasp network; sense Sign, Synchronizer and Data Buffer. At transmit port, wrapper finishes the job in three procedures: (1) LS module applies the data into the buffer if the wrapper is idle. (2) Sense signal sense the condition of buffer and trigger grasp path. (3) Grasp network direct ask for and Acknowledge sign and transmit data from the buffer to the receive port.

4.1. Operation of GALS

To implement the handshake circuit it is necessary to use standard cells which are composed of Transmit port and receive port.

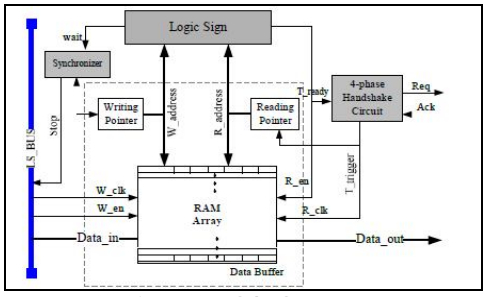

Figure 4: GALS system

T_ready and R_ready are the activating signal for data output and input. T_trigger and R_trigger provide the rising edge of T_request and R_ack. T_clear and R_clear are used to create the stumpy phase of T_request and R_ack.

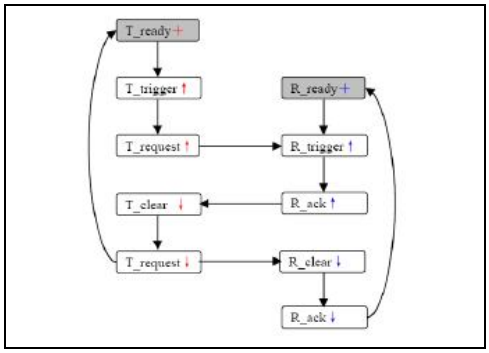

Figure 5: Signal Transition

For T-port, T_ready will be developed suddenly when the data buffer shows it is full. If the R_ack is at low phase, data buffer will be rising. Then T_request+ will be transmitted to the R-port, where which combines with the demanding signal for reading data from buffer. R_ack+ direct to T_request- which resets R_ack+ to R_ack-. Likewise the synthesis of R port can also be done.

4.2. Features of Handshake circuit

Handshake circuits easily match with LS modules, and also reliable and robust. Easy to an average data communication speed.

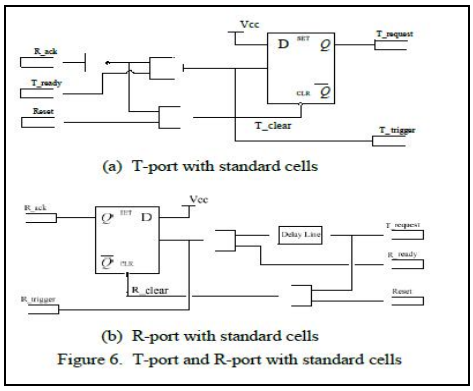

Figure 6

4.3. Simulation and Verification

The transmit port of GALS wrapper is linked by means of pre-module through buffer, and the receive port is linked with follow-module. The modeling of a circuit is done in VHDL then the timing sequence is simulated and verified in an Spartan 3e FPGA by using Xilinx 14.1.

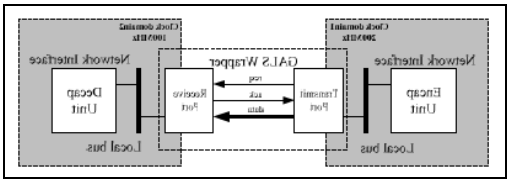

Figure 7: structure of point to point communication

From	To	Time consumes(ps)
T ready	T trigger	283
T trigger	T request	1212
T request	R trigger	310
R trigger	R ack	1303
T clear	T request	304

Figure 1

5. Conclusion

The conclusion of this theory is that GALS network is designed with the application of NoC to reduce the time consumption in transmitting the data. This can be accomplished and tested, verified with the use of VHDL and EDA tools.

6. References

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