# Approximate Adder Design Using CPL Logic for Image Compression

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*Abstract:*
*Low power is an imperative requirement for portable multimedia devices for employing various signal processing algorithms and architectures. In most multimedia applications, human beings can gather useful information from slightly erroneous outputs. Therefore it is not necessary to produce exactly the correct numerical outputs. Taking this fact into account, complexity reduction was done in the adder design, as adder design has become the most focused area in the VLSI design process to reduce the power consumption and to enhance the speed and overall performance of the system. In the previous work, the number of transistors was reduced in the conventional mirror adder based on certain approximations also the area comparison was done for the conventional mirror adder and its four approximations. In this paper a much more advanced Complementary Pass Transistors Logic (CPL) adders are used in the design for considering the approximations and the obtained area and power savings is compared with the previous work. The simulated results show area savings of 31.3% and power savings of 36%.*

*Key words: CPL adder, approximate adders, image compression*

**Conventional CPL Adder and Its Approximation Designs**

## 1. Introduction
Complementary Pass Transistor Logic (CPL) is becoming increasingly important in the design of specific classes of digital integrated circuits which employ the XOR and MUX operations. The complexity of CMOS can be reduced by adopting CPL circuits. Here all inputs are applied in complementary form which means every input signal and its inverse have to be applied. The simulations show that the delay and total power dissipations in CPL design are better than conventional CMOS logic design. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level. CPL circuits come in the category of fast operating circuits. This adder exhibits low propagation delay and Power Delay Product (PDP). PDP is defined as the extend of energy utilised by the system in performing a determined task. Inorder to quantify how effective or efficient a design technology, in terms of delay and power, the product of propagation delay and power dissipation can be used. PDP also influences the overall performance of the system.

### 1.1. Conventional CPL Adder
The figure 1 shows the circuit diagram for conventional CPL adder. The CPL circuits have the specialty that here there are inverters that drive the inputs to the outputs. Here there are three inputs A, B, Cin. Circuit configurations are arranged such that Cin is the selection line and the outputs Sum and Cout are taken from the MUX as seen in figure 1. The cases for the operation are shown below;

When Cin= 0;
Sum= A XOR B, Cout= A AND B
When Cin=1;
Sum= $\overline{\text{A XOR B}}$, Cout= A OR B
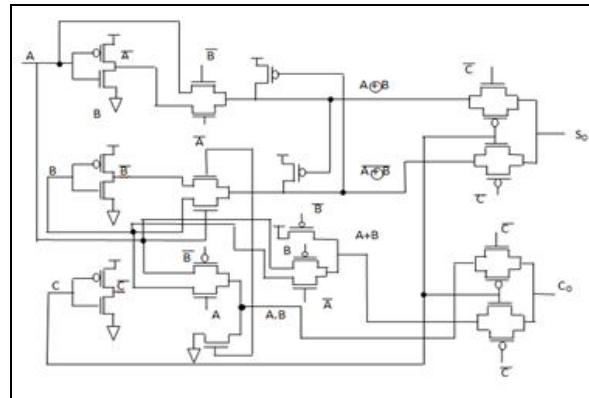


*Figure 1: Conventional CPL adder [2]*

| INPUTS | | | ACCURATE O/P | |
|---|---|---|---|---|
| **A** | **B** | **Cin** | **Sum** | **Cout** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

*Table 1: Truth Table for Conventional CPL adder*

*1.2. Approximate Adder-1*
In the first approximate adder design, two transistors have been removed and the circuitdiagram is given in figure 2 and the truth table 2 shows that even if two transistors were removed it did not bring any influence in the Sum and Cout.
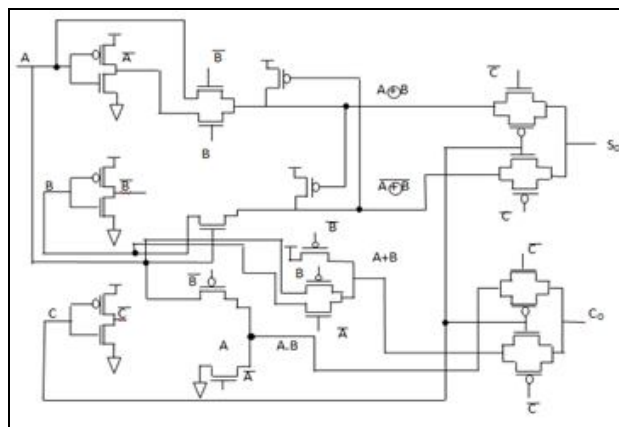


*Figure 2: Approximate Adder-1*

| | Inputs | | Accurate o/p | | Approximate o/p | |
|---|---|---|---|---|---|---|
| A | B | Cin | Sum | Cout | Sum1 | Cout1 |
| 0 | 0 | 0 | 0 | 0 | 0✓ | 0✓ |
| 0 | 0 | 1 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 0 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 1 | 0 | 1 | 0✓ | 1✓ |
| 1 | 0 | 0 | 1 | 0 | 1✓ | 0✓ |
| 1 | 0 | 1 | 0 | 1 | 0✓ | 1✓ |
| 1 | 1 | 0 | 0 | 1 | 0✓ | 1✓ |
| 1 | 1 | 1 | 1 | 1 | 1✓ | 1✓ |

*Table 2: Truth Table for Approximate Adder-1*

### 1.3. Approximate Adder-2

Figure 3 shows the approximate adder 2 design where again two transistors are removed andthe truth table 3 shows that there are two errors in sum part that's when A=B=Cin=0 and A=0, B=Cin=1.
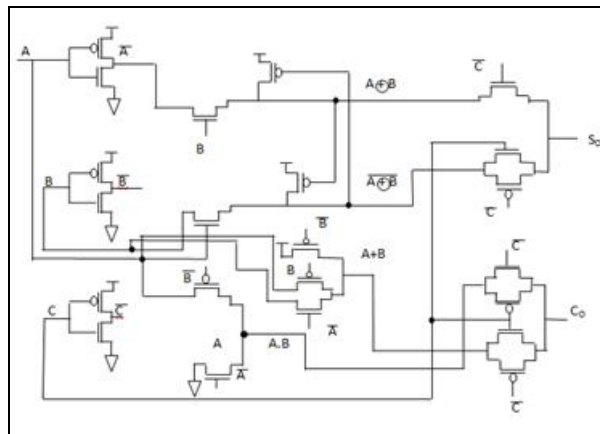


*Figure 3: Approximate Adder-2*

| | Inputs | | Accurate o/p | | Approximate o/p | |
|---|---|---|---|---|---|---|
| A | B | Cin | Sum | Cout | Sum2 | Cout2 |
| 0 | 0 | 0 | 0 | 0 | 1× | 0✓ |
| 0 | 0 | 1 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 0 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 1 | 0 | 1 | 1× | 1✓ |
| 1 | 0 | 0 | 1 | 0 | 1✓ | 0✓ |
| 1 | 0 | 1 | 0 | 1 | 0✓ | 1✓ |
| 1 | 1 | 0 | 0 | 1 | 0✓ | 1✓ |
| 1 | 1 | 1 | 1 | 1 | 1✓ | 1✓ |

*Table 3: Truth Table for Approximate Adder-2*

### 1.4. Approximate Adder-3

Figure 4 shows circuit diagram for approximation 3 with only 17 transistors and table 4 shows the truth table. That means when compared to conventional CPL adder about 9transistors are removed. The errors are found in the sum part when A=0, B=Cin=1 and in Cout part when A=B=1, Cin=0.
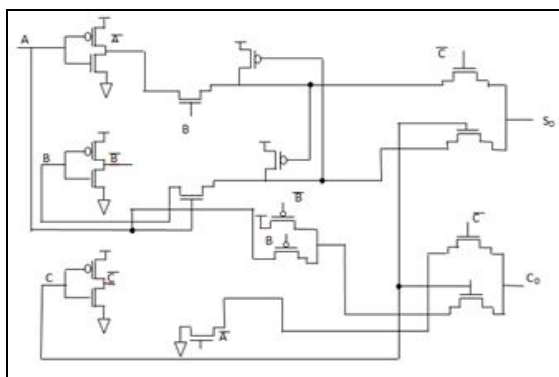
*Figure 4:  Approximate Adder-3*

| Inputs | | | Accurate o/p | | Approximate o/p | |
|---|---|---|---|---|---|---|
| A | B | Cin | Sum | Cout | Sum3 | Cout3 |
| 0 | 0 | 0 | 0 | 0 | 0✓ | 0✓ |
| 0 | 0 | 1 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 0 | 1 | 0 | 1✓ | 0✓ |
| 0 | 1 | 1 | 0 | 1 | 1× | 1✓ |
| 1 | 0 | 0 | 1 | 0 | 1✓ | 0✓ |
| 1 | 0 | 1 | 0 | 1 | 0✓ | 1✓ |
| 1 | 1 | 0 | 0 | 1 | 0✓ | 0× |
| 1 | 1 | 1 | 1 | 1 | 1✓ | 1✓ |

*Table 4: Truth Table for Approximate Adder-3*

*1.5. Approximateadder-4*
Figure 5 gives the circuit diagram for approximation 4 with total transistors of 16 and thecorresponding truth table is shown in table 5. Here there are two errors in sum and one error in Cout. In sum part error is found when A=B=Cin=0 and A=B=Cin=1 and in the Cout part it's found when A=B=1, Cin=0.
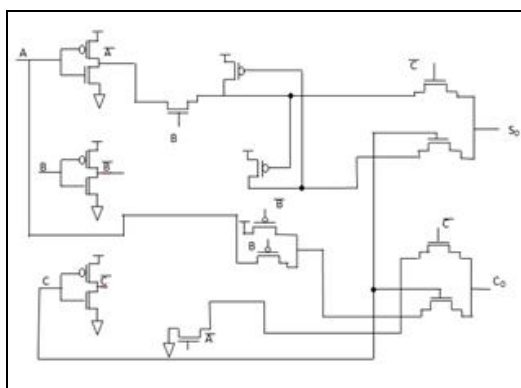


*Figure 5: Approximate Adder-4*

| Inputs | | | Accurate o/p | | Approximate o/p | |
|---|---|---|---|---|---|---|
| A | B | $C_{in}$ | Sum | $C_{out}$ | Sum4 | Cout4 |
| 0 | 0 | 0 | 0 | 0 | 1× | 0✔ |
| 0 | 0 | 1 | 1 | 0 | 0× | 0✔ |
| 0 | 1 | 0 | 1 | 0 | 1✔ | 0✔ |
| 0 | 1 | 1 | 0 | 1 | 1× | 1✔ |
| 1 | 0 | 0 | 1 | 0 | 1✔ | 0✔ |
| 1 | 0 | 1 | 0 | 1 | 0✔ | 1✔ |
| 1 | 1 | 0 | 0 | 1 | 0✔ | 0× |
| 1 | 1 | 1 | 1 | 1 | 1✔ | 1✔ |

*Table 5: Truth Table for Approximate Adder-4*

## 2. Image Compression

The next part of the work deals with the implementation of adder design in the DSP application. The DSP application mainly includes image and video compression. Here the analysis of the result was done on the image compression. The 1-D DCT architecture was considered and the Mirror Adder (MA), which is the adder available in the DSP applications for industrial purposes, is here replaced by the CPL adders.

Discrete Cosine Transform (DCT) is a computation intensive algorithm has a lot of electronic applications. DCT transforms the information from the time or space domains to the frequency domain to provide compact representation, fast transmission, memory saving and so on. DCT algorithm is very effective due to its symmetry and simplicity. DCT computation requires a large number of adders and multipliers for direct implementation. Now, the 1-D DCT architecture can be considered that have been used for the project work and is shown in figure 6.
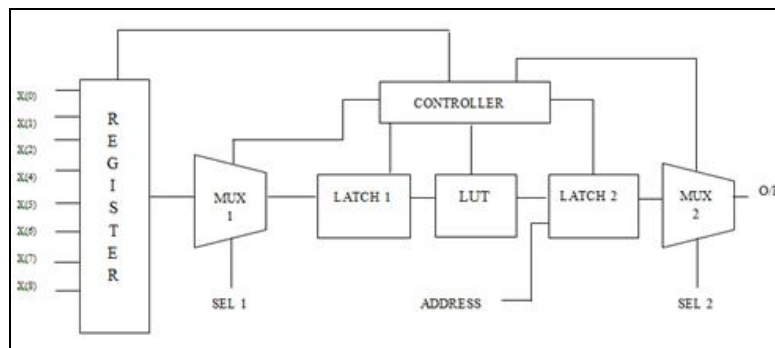


*Figure 6: 1-D DCT Architecture*

The register contains eight inputs X (0), X (1)…X (7), where each input signal is an eight bit pixel. Based on the selection input given by MUX 1 one of the samples is selected and through the LATCH 1 it is shifted to Look up Table (LUT) where the mathematical computation is carried out and the result is shifted to the MUX 2 through the LATCH 2 and hence compressed DCT output is obtained. The controller has the role of controlling the overall components of the architecture.

## 3. Result Analysis

The adder designs and its timing diagram are obtained using MICROWIND software. The simulation results for DCT architecture is done in MODELSIM and the power analysis is obtained using XILINX ISE.
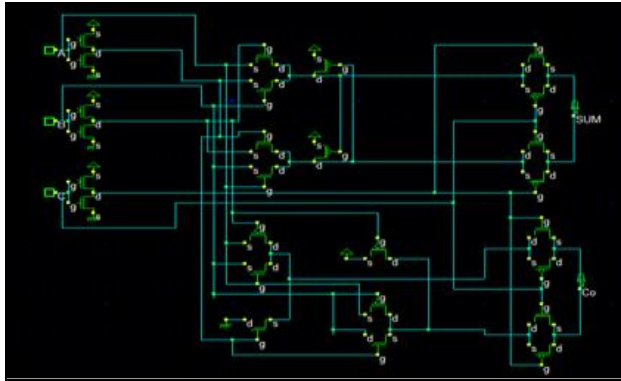
*3.1. Simulation result of Conventional CPL Adder*
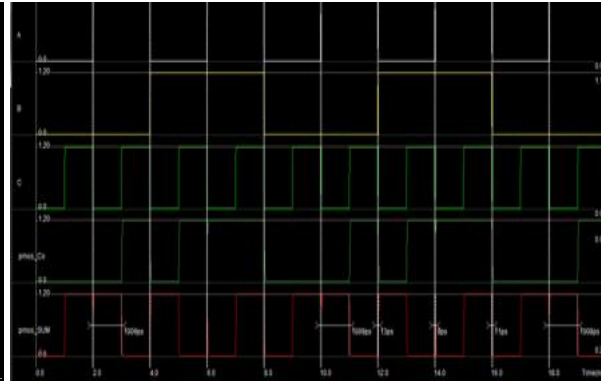



*Figure 7: Schematic layout of conventional CPL adder*
*Figure 8: Timing Diagram*

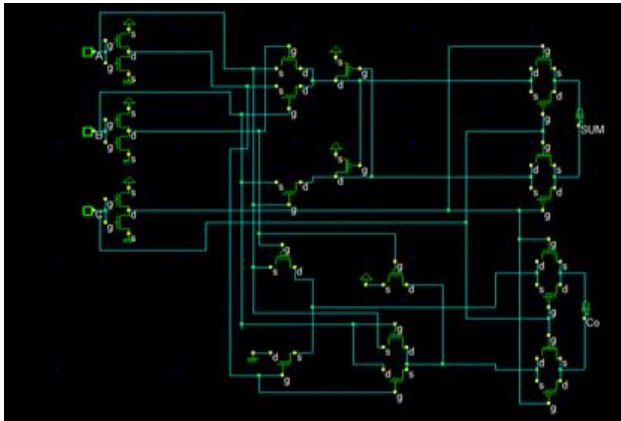*3.2. Simulation result of Approximate Adder 1*




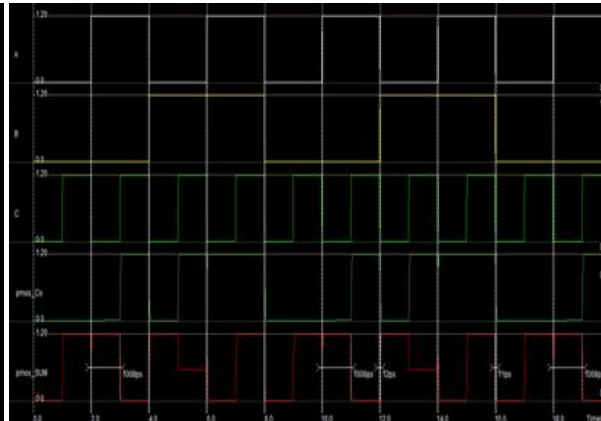*Figure 9: Schematic layout of Approximate Adder 1*
*Figure 10: Timing Diagram*
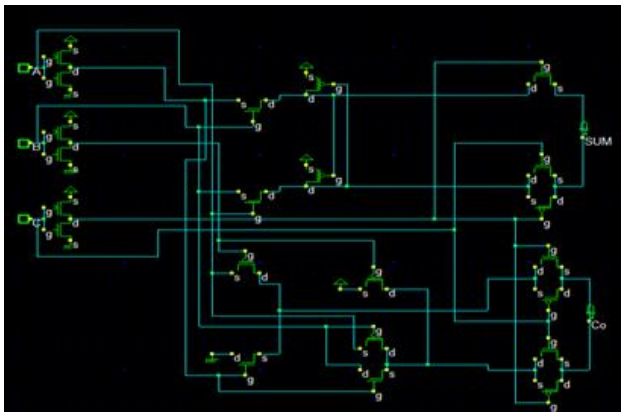
*3.3. Simulation result of Approximate Adder 2*


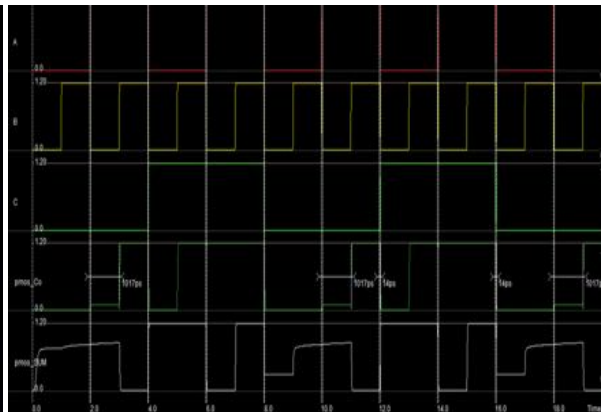

*Figure 11: Schematic layout of Approximate Adder 2*
*Figure 12: Timing Diagram*

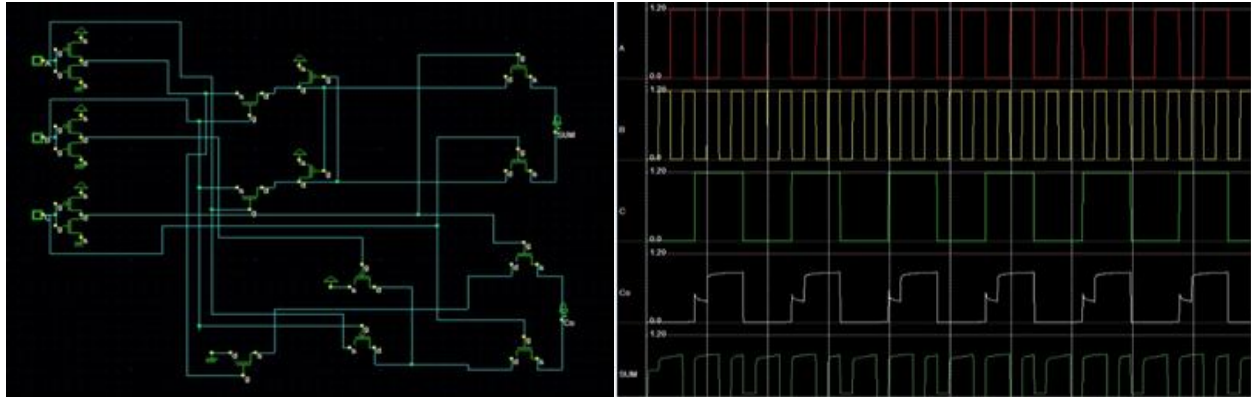*3.4. Simulation result of Approximate Adder 3*



*Figure 13: Schematic layout of Approximate Adder 3*
*Figure 14:  Timing Diagram*

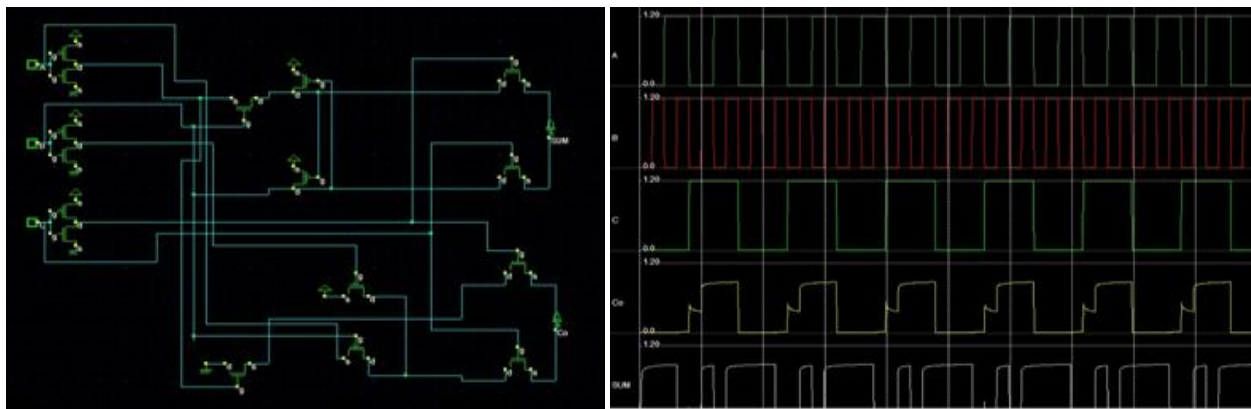*3.5. Simulation result of Approximate Adder 4*



*Figure 15: Schematic layout of Approximate Adder 4*
*Figure 16: Timing Diagram*

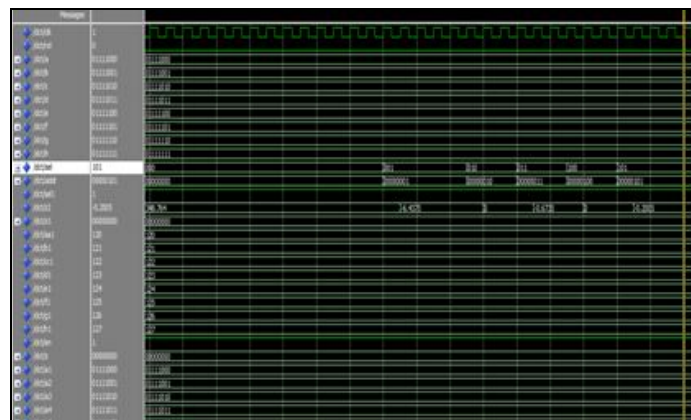*3.6. Simulation result of DCT*



*Figure 17: Simulation result of DCT*
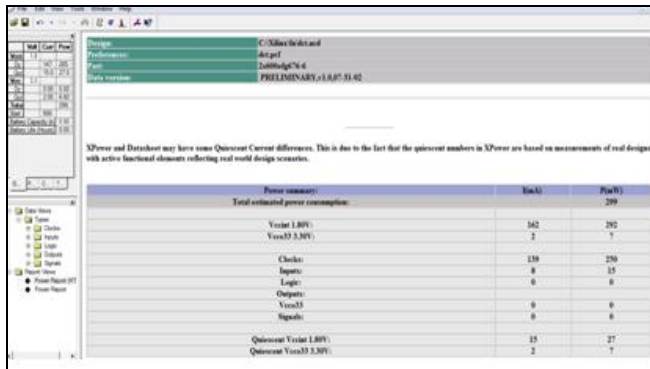
*3.7. Power Analysis*



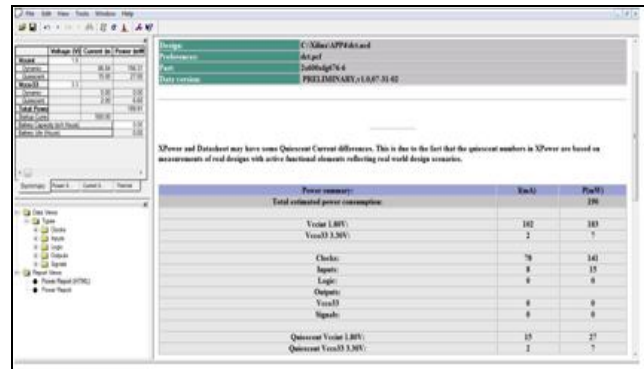*Figure 18: Power Analysis of Conventional CPL Adder*



*Figure 19: Power Analysis of Approximate Adder 4*

## 4. Power and Area Comparisons

The power comparisons for various DCT architecture designs based on the adder designare given in the table 6 and the area comparison for the different adder types are given in table 7. The table shows the power and area comparisons of design using CPL adder and the previous work using Mirror Adder (MA). The table 6 shows that the power consumed for the DCT architecture designed using approximate adder 1 has the lowest power consumption rate and that of conventional MA is the design with highest power consumption. Table 7 shows that approximate adder 4 has the most reduced area when compared to all the other four types.

| ADDER TYPE | CONVENTIONAL DESIGN | APPROXIMATION 1 | APPROXIMATION 2 | APPROXIMATION 3 | APPROXIMATION 4 |
|---|---|---|---|---|---|
| POWER ANALYSIS OF MIRROR ADDER (mW) | 588 | 583 | 580 | 578 | 577 |
| POWER ANALYSIS OF CPL ADDER (mW) | 299 | 288 | 261 | 210 | 190 |

*Table 6: Power Comparison*

| ADDER TYPE | CONVENTIONAL DESIGN | APPROXIMATION 1 | APPROXIMATION 2 | APPROXIMATION 3 | APPROXIMATION 4 |
|---|---|---|---|---|---|
| AREA FOR MIRROR ADDER ($\mu m^2$) | 612.9 | 461.9 | 475.1 | 449.9 | 433.1 |
| AREA FOR CPL ADDER ($\mu m^2$) | 460 | 430 | 401 | 352 | 316 |

*Table 7: Area Comparison*

## 5. Conclusion and Future Enhancement

*5.1. Conclusion*

In this project, several imprecise or approximate adders were designed that can be utilized effectively to trade off power and quality for error resilient DSP systems. The main aim was to reduce the complexity of a conventional Complementary Pass Transistor adder (CPL) cell by reducing the number of transistors. It was found that even though errors were generated in the result due to

approximations, it had very little impact on the output quality when applied to DSP algorithm. Conventional CPL adder design had 26 transistors which were reduced to 16 transistors in approximation 4. From the simulation results it is obtained that there is an area savings of 31.3% in the proposed design whereas it was only 29.2% in existing design. The power savings in the proposed design shows about 36% which shows the design is an efficient implementation.

*5.2. Future Enhancement*
As the need for low power DSP applications in portable multimedia devices is an inevitable and imperative requirement, it's necessary to consider techniques that can generate reduced power with minimized area and efficient performance. By taking this into consideration a new design in approximate computing can be introduced that can bring promising advances to DSP applications.
Adders using complementary pass transistor logic are estimated to bring more power savings and area reduction when compared to previous work that is by using MA and it's approximate adder design. The adder design were implemented in the 1-D DCT architecture and a small portion of image compression was shown inorder to analyze the efficiency of the approximate design but this can also be extended to video compression purposes as well and hence can find drastic changes in the DSP applications by reducing the area and power consumption to a greater extend.

## 6. References
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