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Design of Efficient Two Stage Power Amplifier Using 65nm Cmos Technology

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Abstract:
In the modern Era, VLSI design is one of the paradigm to have low noise,high power and small chip area. The design of CMOS power amplifier is an effort in this domain which is applicable for wireless communication system. The proposed design employ switching mode of two stage power amplifier to exploit it's soft switching property to achieve high output power and high efficiency.
Two stage power amplifier for WLAN applications in 65nm CMOS technology is proposed to be designed. The functionality of proposed design of two stage power amplifier will be verified for parameters like high output power and high efficiency. The main emphasis is on achieving high gain with low return losses.
The layout of the proposed power amplifier will be tried to have minimum design area with improved parameters as compared to previous literature reviewed designs.

1. Introduction

VLSI design is one of the technique of placing thousands or hundreds of thousands of electronic components on a single chip. In the modern Era, VLSI design is one of the paradigms to have low noise, high power and small chip area. The design of CMOS power amplifier is an effort in this domain which is applicable for wireless communication system.

RF amplifiers are electronic devices that accept a varying input signal and produce an output signal that varies in the same way as the input, but that has larger amplitude. The input circuit applies varying resistance to an output circuit generated by the power supply, which smoothes the current to generate an even, uninterrupted signal. Depending on load of the output circuit, one or more RF pre-amplifiers may boost the signal and send the stronger output to a RF power amplifier (PA).

The push-pull amplifier is built using a voltage comparator and a power output stage. A push–pull amplifier is more efficient than a single-ended "Class A" amplifier. The output power that can be achieved is higher than the continuous dissipation rating of either transistor or tube used alone and increases the power available for a given supply voltage.

The authors describe the design of a versatile analogue building block, termed an operational transresistance amplifier (OTRA). An operational transresistance amplifier has two low-input-impedance terminals and one low-output-impedance terminal. It is found to have a constant bandwidth independent of the gain in most closed-loop configurations.

CMOS power amplifiers are integral parts in various analog and mixed-signal circuits and systems. The two-stage power amplifier is widely used because of its structure and robustness. In designing power amplifier, numerous electrical characteristics, e.g. gain, operating voltage, operating frequency, maximum output power all have to be taken into consideration.

In the proposed design our main aim is on implementation of high efficient two stage power amplifier in VLSI for various communication applications. We are using 65 nm CMOS technology for design of two stage CMOS power amplifier.

1.1. Block diagram

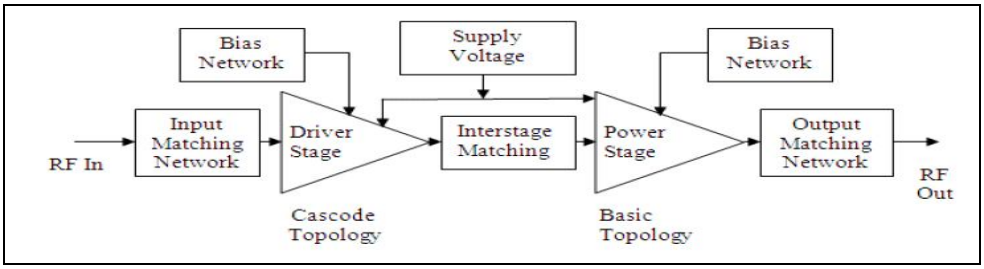

Figure 1.1: Block Diagram of Complete Two Stage CMOS Power Amplifier

The above figure shows the functional block diagram of the designed two stage Power Amplifier. Input matching and Output matching networks are used at input and output stage respectively to minimize return losses which results in increased gain and output power. Input matching is done by calculation of input impedance using the ratio of the input voltage and input current. Passive elements having some impedance are connected at the input side forming a input matching network to match this impedance. The loss occurred in this part of the circuit due to improper matching is known as Input return loss and denoted as S(1,1). The same concept is utilized to find S(2,2) at the output side. An interstage matching network is also used as two stages are used for power amplification. Driver stage and Power stage with the supply and bias network are main blocks of the power amplifier. A cascade topology is used in the driver stage and a basic power amplifier topology is used in the power stage.

2. Related Work

In the year of 2002, IEEE Journal of solid state circuits, Fully Integrated CMOS Power Amplifier Designed Using the Distributed Active-Transformer Architecture. A novel fully integrated single-stage circular geometry active-trans- former (DAT) power amplifier implemented in a low-voltage CMOS process achieves 1.9-W output power with 41% (31% single-ended) PAE at 2.4 GHz. It had used as a 450-mW 2.4-GHz amplifier with 27% PAE using a 1-V supply. The circuit includes input and output matching to 50 , requiring no external components & output matching had been fabricated using 0.35-µm CMOS transistors. It achieves a power added efficiency (PAE) of 41% at this power level. I.[1]

In the year of 2003 IEEE journal, The paper presented A fully integrated differential class-AB power amplifier has been designed in a 0.25µm CMOS technology. By using two parallel output stages that can he switched on or off, a high efficiency had been achieved for both high and low output power levels. The PA is fully integrated, including output matching network. Simulations show that an output power of 22.7 dBm may be achieved with a maximum PAE of 22%. The average efficiency has been improved by using two parallel output stages.[2]

In the year of 2007 IEEE Custom Intergrated Circuits Conference (CICC), A fully integrated 90nm CMOS PA capable of delivering 6.7 dBm of linear power in the 60 GHz band has been demonstrated. The PA has a measured efficiency of 20% and is appropriate as a pre-driver or for short range mm-wave transmitter applications. This amplifier can be used as a pre-driver or as the main PA for short range wireless communication. The output power had been boosted with on-chip or spatial power combining.[4]

In 2010 IEEE International Conference, The paper presented a 2.4 GHz fully integrated CMOS power amplifier using capacitive cross coupling, fabricated in 0.18 µm CMOS with 3.3V supply voltage. PAE_{max} and PAE at 1db compression point are 34.3% and26.8%. P_{1db}, P_{sat} and PG are 25.2dBm, 27.7dBm and26.5dB.[5]

In the year of 2010, journal of semiconductors, A two-stage differential linear power amplifier (PA) fabricated by 0.18µm CMOS technology is presented With an output matching network and a harmonic control strategy, measurements show that this PA achieves a saturated power of 21.1 dBm, a power gain of 23.3 dB and a maximum PAE of 35.4% from a 1.8 V supply at 900 MHz. The harmonics are measured to be less than40 dBc at its 1 dBCP[7].

In October 2012, a fully integrated linear and efficient PA in 0.25- µm SiGe:C BiCMOS technology is presented and works at 2 GHz with a supply voltage of 2.5 V. The experimental results show a gain of 13 dB and a maximum output power of 23 dBm with a PAE of 38%.The efficiency enhancement is achieved using a switchable biasing and a reconfigurable output-matching network based on the available input power which is monitored by an on-chip envelope detector.[8]

In August 2013 paper, Authors have used 0.13µm bandwidth to achieve Output power of 20.028 dBm with high efficiency of 44.669% is obtained at 1dB compression point using CMOS device for the power amplifier. Driver stage as the input stage and power stage as the output stage are the two stages. A cascode topology is used in the driver stage and basic topology is used in the power stage [11]

In the year of 2013, They have designed OTA, it is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source. Operational transconductance amplifier is one of the most significant building-blocks in integrated continuous-time filters. In this paper two stage OTA is optimized and simulated in 0.18µm and 0.35µm technology. Power supply of the architecture is 1.8V. Gain is 47.86 dB, gain margin is 15.40 dB and phase margin is 217.530. Slew rate is 37.58 V/µs and power dissipation is 1.3 mW and Power supply of the architecture is 3.3V. Gain is 46.75 dB, gain margin is 16.94 dB and phase margin is 2250. Slew rate is 31.67 V/µs and power dissipation is 3.2 mW.[12]

In the Solid State Circuits, IEEE journal presents a 1 W, Class-E power amplifier That implemented on 0.35 µm CMOS technology. At 2V supply and 1.98 GHz, The power amplifier achieves 48% power –added efficiency.[13]
As an improvement to the above literature reviews we will design a two stage power amplifier by using 65 nm CMOS technology for various communication applications.

3. Technology Used
The technology we are using to convert the given network in analog VLSI chip design is 65nm CMOS technology. The analog components used are comprised of multipliers and adders along with the tan-sigmoid function circuit.

3.1. VLSI Technology
We are using VLSI technology for implementation of two stage power amplifier.
The most important message here is that the logic complexity per chip has been (and still is) increasing exponentially. The monolithic integration of a large number of functions on a single chip usually provides:

- Less area/volume and therefore, compactness
- Less power consumption
- Less testing requirements at system level
- Higher reliability, mainly due to improved on-chip interconnects
- Higher speed, due to significantly reduced interconnection length
- Significant cost savings

3.2. 65nm CMOS Technology
The 65nm is starting to be considered as a new attractive solution in view of the development of high-density, high-performance, mixed-signal readout circuits. Some of the key features of 65 nm technologies from various providers like TSMC, Fujitsu, and Intel are as given below.

Sr. No.	Parameter	Value
1	VDD (V)	0.8-1.2 V.
2	I_{off}N (Na/µm)	5-100
3	I_{off} P (Na/µm)	5-100
4	Gate dielectric	SiON
5	No. of metal layers	8-10

Table 3.1: Key Features of 65 nm Technology

Compared to 90-nm technology, 65 nm technologies has to offer:

- 1.3 times faster speed.
- 0.6 times lower power.
- 2 times higher density

Considering the advantage of 65 nm technologies over 90 nm technology, the proposed work is done with 65 nm technology.

3.3. Microwind 3.1 software
Here for the design using VLSI technology, microwind 3.1 VLSI Backend software is used. Design and simulation of an integrated circuit at physical description level is possible using microwind 3.1 software. Low leakage transistors are used for low power operation and will compromise a little bit on frequency.
As seen in the palette figure 3.1, the available metal layers in 45nm technology range from metal1 to metal8. The layer metal1 is situated at the lowest altitude, close to the active device, while metal8 is nearly 10µm above the silicon surface. Labeling of the metal layers is done according to the order in which they are fabricated, from the lower level (metal1) to the upper level (metal8).
In Microwind3.1, the macros which ease the addition of contacts in the layout have been updated to handle up to 8 layers of metal.

Figure 3.1: Window with the palette of layers including 8 levels of metallization

4. Design Methodology

4.1. Design flow graph

Following steps are involved to obtain the proposed design.

- Schematic design for two stage power amplifier.
- Design for the driver stage of amplifier will be implemented first..
- Above design will be followed by design for the power stage of amplifier.
- Then it will be followed by impedance matching.
- Then biasing of circuit will be done.
- Finally simulation result will be achieved.

First the schematic design of two stage amplifier is designed . Next stage is to driver stage of amplifier which is main block of power amplifier for this formal verification is done and CMOS layout is designed. Following to this power stage of amplifier which is also the main block of amplifier is designed for this again formal verification is done and CMOS layout is designed. Then impedance matching is carried out at the input and output side of amplifier to minimize return losses which results in increased gain and output power and verification of different parameter such as operating voltage, gain , frequency, efficiency is done. And finally if the verification is satisfactory the amplifier is designed otherwise we have to test it from first step.

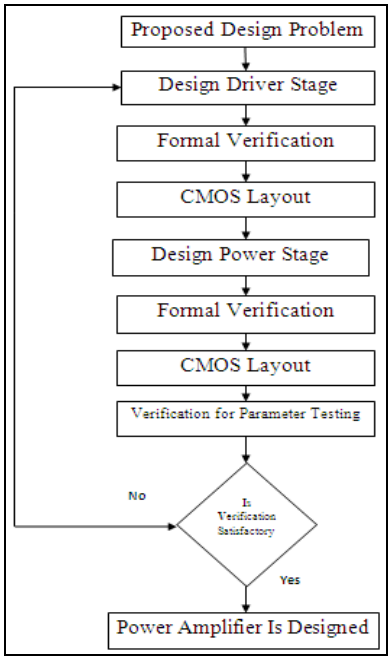

Figure 4.1: Flow Chart

5. System Model Description & It's Experimental Results

5.1. Push –Pull Amplifier

The push-pull amplifier is built using a voltage comparator and a power output stage. Its schematic diagram is reported in figure 5.1, with some details about the important voltage nodes. The difference between Vp and Vm is amplified and produces a result, codified Vout. Transistors Nb and Pb are connected as diodes in series to create an appropriate voltage reference Vbias, fixed between the nmos threshold voltage Vtn and half of VDD. The differential pair consists of transistors N1 and N2. This time, two stages of current mirrors are used: P1, P2 and P3, PO.

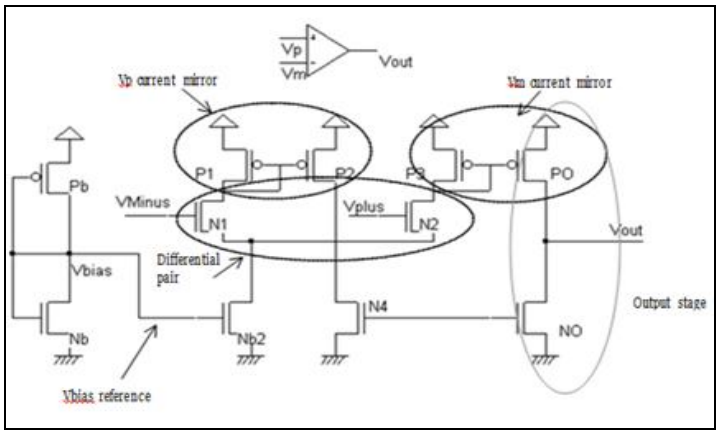

Figure 5.1: Circuit diagram for Push Pull Amplifier

5.1.1. Schematic for Push Pull Amplifier

The figure 5.2 shows the schematic of Push Pull Amplifier

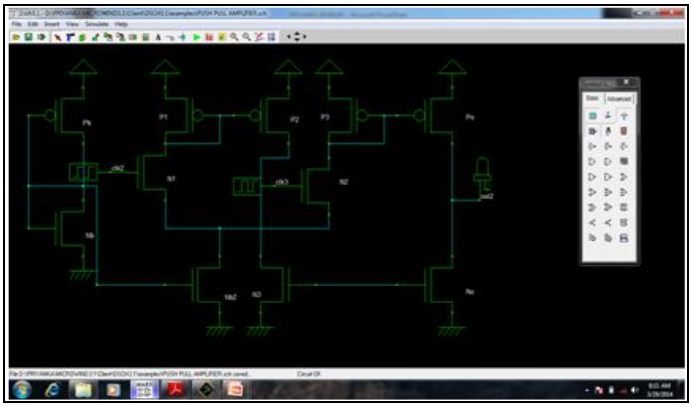

Figure 5.2: Schematic for Push Pull Amplifier

The output stage consists of transistors PO and NO. These transistors are designed with large widths in order to lower the output resistance. Such a design is justified when a high current drive is required: high output capacitor, antenna dipole for radio-frequency emission, or more generally a low impedance output. The ability to design the output stage according to the charge is a key advantage of this structure compared to the simple differential pair presented earlier. The implementation shown in figure 5.1 uses NO and PO output stage devices with a current drive around five times larger than the other devices. In practice, the ratio may rise up to 10-20.

5.1.2. CMOS layout for Push Pull Amplifier

The figure 5.3 shows the layout of Push Pull Amplifier which is designed using, 65nm VLSI technology & it is the basic amplifier design.

The first input voltage signal is Vin1= 0.35V.

The second input voltage signal is Vin2= 0.34V.

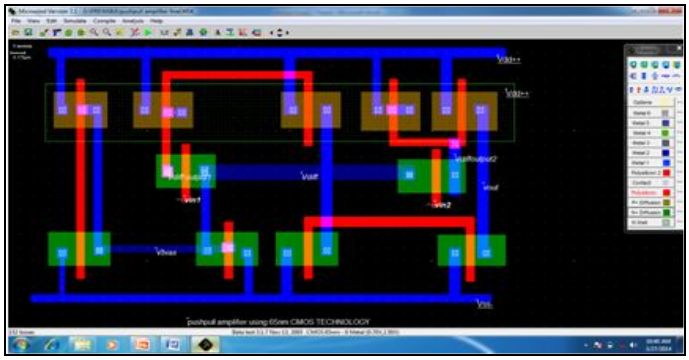

Figure 5.3: CMOS layout for Push Pull Amplifier

Table 5.1 contains the number of CMOS transistors used, length and width of each transistor in designed push pull amplifier.

Sr. No.	Transistor	Length × Width
1	N1	0.420×0.105µm
2	N2	0.455×0.105µm
3	N3	0.455×0.105µm
4	N4	0.455×0.140µm
5	N5	0.455×0.105µm
6	N6	0.455×0.105µm
7	P1	0.525×0.105µm
8	P2	0.525×0.140µm
9	P3	0.490×0.105µm
10	P4	0.490×0.105µm
11	P5	0.490×0.105µm

Table 5.1: Transistors used in Push Pull Amplifier

5.1.3. Simulation of Push- Pull Amplifier

Figure 5.4 shows the voltage versus time response of Push Pull Amplifier.
Here output voltage obtained is 0.83 V and power required by Push Pull Amplifier is 82.960µW.

Figure 5.4: Simulation Result of push Pull Amplifier (Voltage Vs Time)

The transient simulation shows an interesting phenomenon called ringing. The oscillation appearing at time 0.1ns is typical for a feedback circuit with a large loop delay and a very powerful output stage. Its voltage is strongly driven by the powerful devices PO and NO. The oscillation can be dangerous as it introduces instability. It also signifies that the output stage is too strong compared to its charge.

5.2. Operational Transresistance Amplifier.

Recently, great interest has been devoted to the design of the operational transresistance amplifiers (OTRAs) . This great interest is mainly because the OTRA is not slew limited in the same fashion as voltage op amps. It can provide a high bandwidth independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op amps circuits. The OTRA is a three -terminal analog building block that is defined by the following matrix equation:

$$\begin{bmatrix} V+ \\ V- \\ V0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ Rm & -Rm & 0 \end{bmatrix} \begin{bmatrix} I+ \\ I- \\ I0 \end{bmatrix}$$

Where Rm is the transresistance gain.

The block diagram of the OTRA is shown in Fig. 5.5. The input terminals are virtually grounded, leading to circuits that are insensitive to stray capacitances. Ideally the transre- sistance gain Rm approaches infinity and applying external negative feedback will force the two input currents, I+ and I− to be equal.

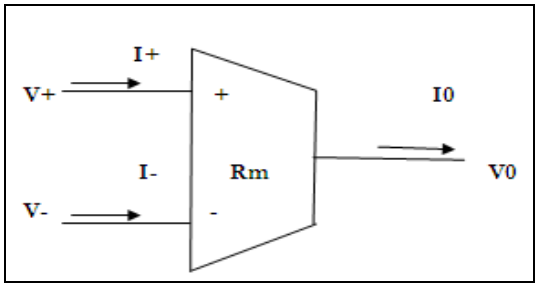

Figure 5.5: Block Diagram of OTRA

5.2.1. Circuit description

The CMOS realization of the proposed high open loop gain differential OTRA is shown in Fig. 5.6. A differential gain stage is used instead of the single common source amplifier. The transistors Mx4–Mx7 produce the non-inverting output, while the tran- sistors My4–My7 produce the inverting output. It is clear that the differential gain stage added has reduced the DC off- set current and increased the DC open loop transresistance gain.

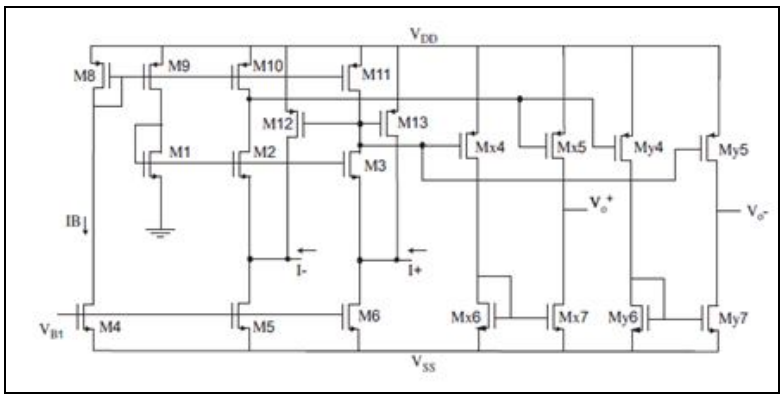

Figure 5.6: Circuit diagram of OTRA

5.2.2. Schematic for OTRA

The figure 5.7 shows the schematic of OTRA.

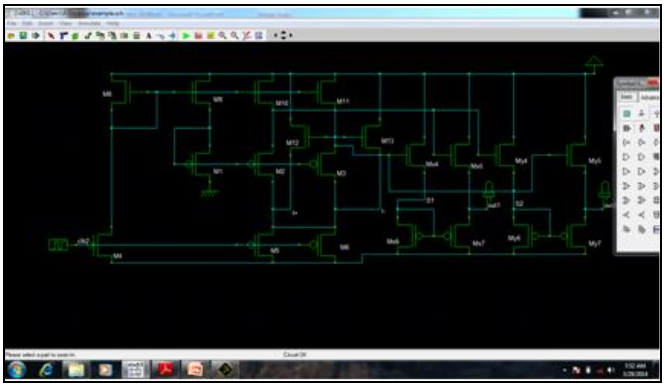

Figure 5.7: schematic of OTRA

5.2.3. CMOS layout for OTRA

The figure 5.6 shows the layout of OTRA which is designed using, 65nm VLSI technology & it is the basic amplifier design. The input clock applied = 0.35V.

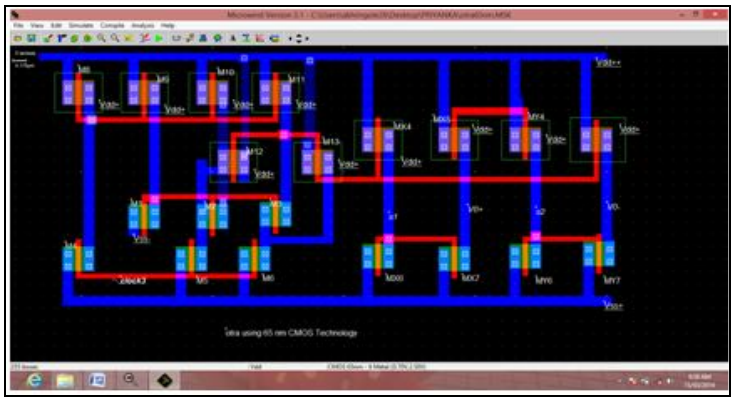

Figure 5.8: CMOS layout for OTRA

Table 5.2 contains the number of CMOS transistors used, length and width of each transistor in designed push pull amplifier.

Sr. No.	Transistor	Length × Width
1	M1-M11	0.35×0.070µm
2	Mx4	0.35×0.070µm
3	Mx5	0.35×0.070µm
4	Mx6	0.35×0.070µm
5	Mx7	0.35×0.070µm
6	My4	0.35×0.070µm
7	My5	0.35×0.070µm
8	My6	0.35×0.070µm
9	My7	0.35×0.070µm

Table 5.2: Transistors used in OTRA

5.2.4. Simulation of Operational Transresistance Amplifier

Figure 5.9 shows the voltage versus time response of Operational Transresistance Amplifier.

Here output voltage V0+ obtained is 0.83 V and V0- obtained is 0.00 V. Power required by Operational Transresistance Amplifier is 0.643µW.

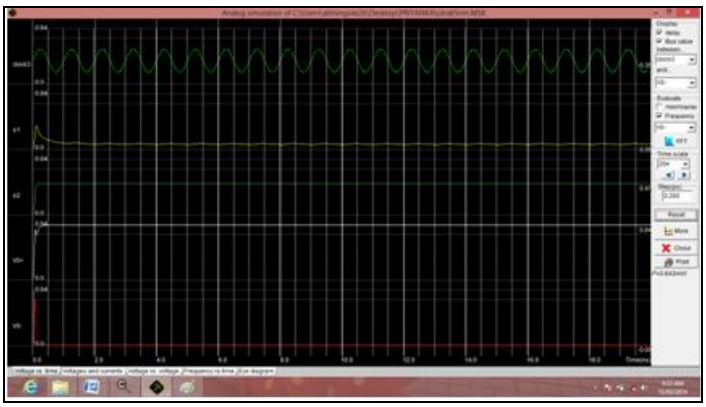

Figure 5.9: Simulation Result of Operational Transresistance Amplifier (Voltage Vs Time)

5.3. Two Stage Power Amplifier

5.3.1. Schematic for Two Stage power Amplifier

The figure 5.10 shows the layout of two stage power Amplifier.

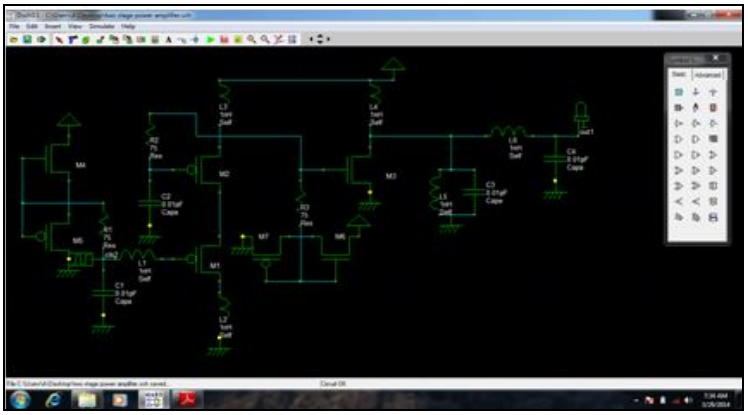

Figure 5.10: Schematic of Two stage power amplifier

5.3.2. CMOS Layout of Two Stage Power Amplifier

The figure 5.11 shows the layout of Two Stage Power Amplifier which is designed using, 65nm VLSI technology & it is the main amplifier design.

The input voltage applied = 0.34V.

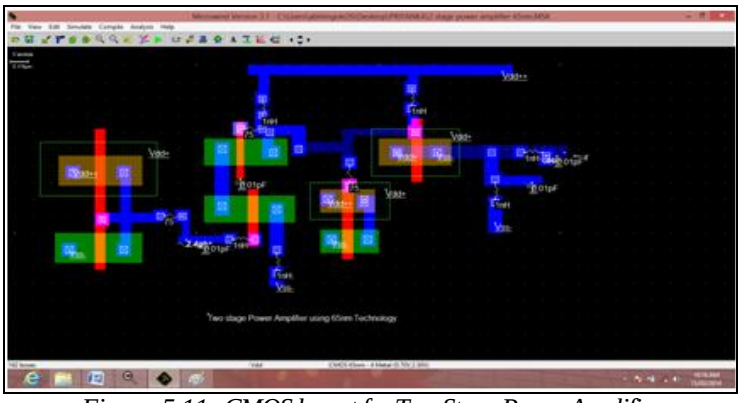

Figure 5.11: CMOS layout for Two Stage Power Amplifier

Table 5.3 contains the number of CMOS transistors used, length and width of each transistor in designed two stage power amplifier.

Sr. No.	Transistor	Length × Width
1	N1	0.245×0.105µm
2	N2	0.280×0.105µm
3	N3	0.280×0.070µm
4	N4	0.315×0.105µm
5	P1	0.280×0.105µm
6	P2	0.245×0.105µm
7	P3	0.315×0.105µm

Table 5.3: Transistors used in two stage power amplifier

5.3.3. Simulation of Two Stage Power Amplifier

Figure 5.12 shows the voltage versus time response of Two Stage Power Amplifier.
Here output voltage obtained is 0.43 V. Power required by Operational Transresistance Amplifier is 12.722 mW.

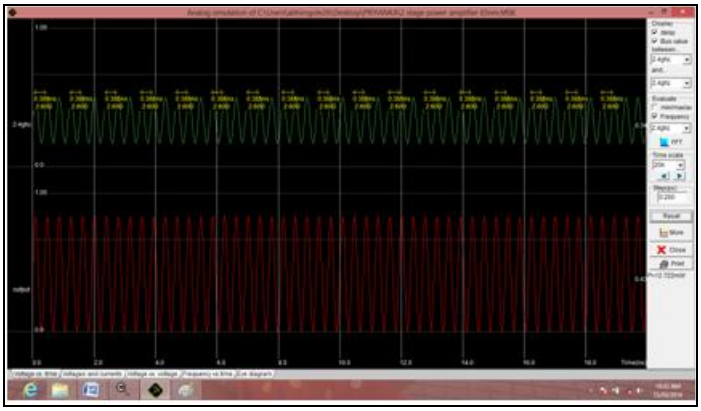

Figure 5.12: Simulation Result of two stage power Amplifier (Voltage Vs time)

Figure 5.13 shows the voltage versus current response of Two Stage Power Amplifier.

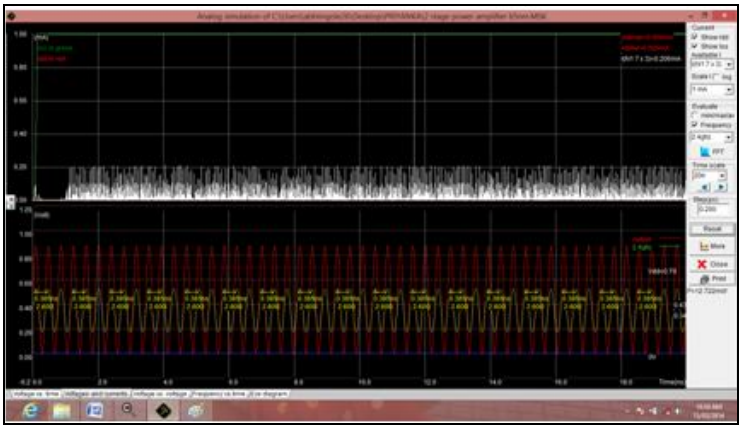

Figure 5.13: Simulation Result of two stage power Amplifier (Voltage Vs current)

Figure 5.14 shows the voltage versus voltage response of Two Stage Power Amplifier.

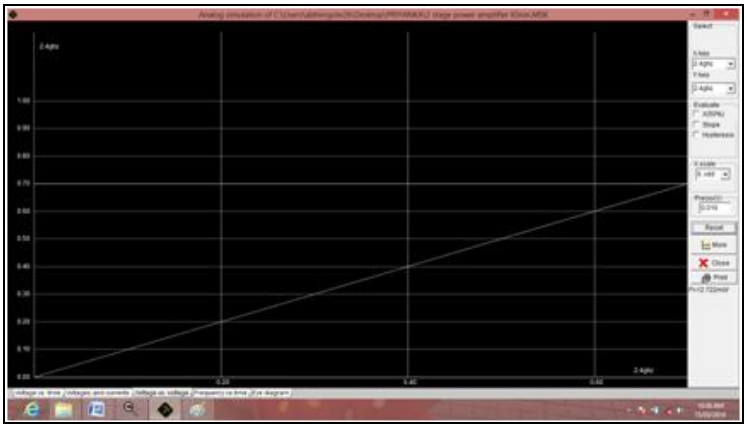

Figure 5.14: Simulation Result of two stage power Amplifier (Voltage Vs voltage)

Figure 5.15 shows the frequency versus time response of Two Stage Power Amplifier.

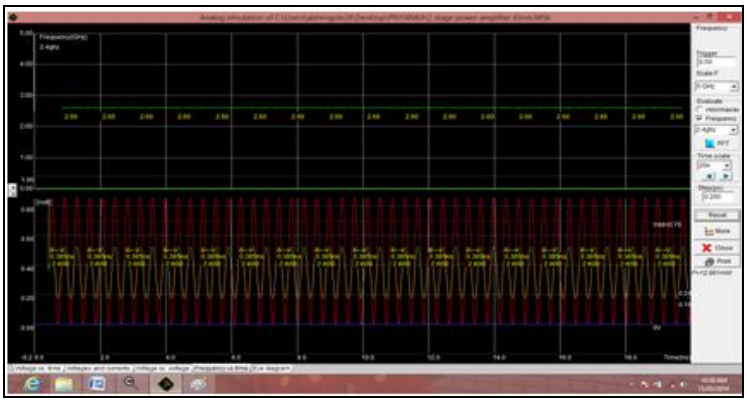

Figure 5.15: Simulation Result of two stage power Amplifier(frequency vs time)

Figure 5.16 shows the eye diagram of Two Stage Power Amplifier.

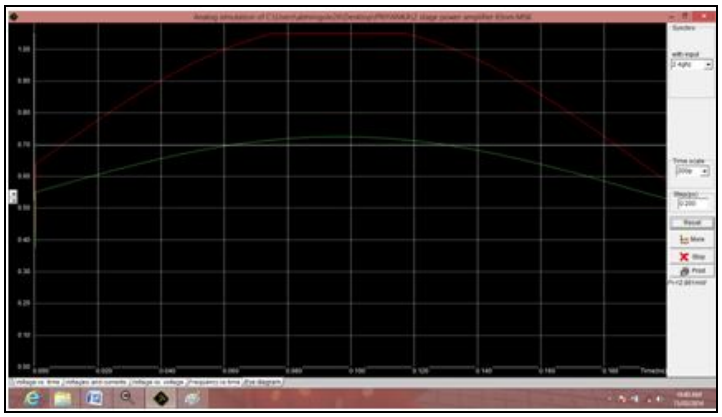

Figure 5.16: Simulation Result of two stage power Amplifier(eye diagram)

SR. NO.	PARAMETERS	VALUE
1	VDD(V)	0.8-1.2 V.
2	I_{off} N (nA/μm)	5-100
3	I_{off} P (nA/μm)	5-100
4	Gate dielectric	SiON
5	Input voltages of push pull amplifier	V_{in1}=0.35V, V_{in2}=0.34V
6	Output voltage of push pull amplifier	V_{out}=0.83V
7	Input voltage of operational transrsistance amplifier.	V_{in}=0.35V
8	Output voltages of operational transrsistance amplifier	V_{out}=0.83
9	Input voltage of two stage power amplifier.	V_{in}=0.34V
10	Output voltages of two stage power amplifier.	V_{out}=0.43V
11	No. of NMOS & PMOS transistors in push pull amplifier	6 NMOS, 5 PMOS
12	No. of NMOS & PMOS transistors in operational transrsistance amplifier	10 NMOS, 10 PMOS
13	No. of NMOS & PMOS transistors in two stage power amplifier.	4 NMOS, 3 PMOS
14	Power required for push pull amplifier	82.960 mW
15	Power required for operational transrsistance amplifier	0.643 mW
16	Power required for two stage power amplifier.	12.722 mW

Table 5.4: Parametric summary of proposed two stage power amplifier

From the parametric analysis of design tool, the power dissipation measured by V_{DD} at 1.2Volt is found to be 82.960mwatt for push pull amplifier, 0.643mwatt for operational transresistance amplifier and 12.722mwatt for two stage amplifier which shows that power consumption is very low.
Following table shows the comparative analysis of proposed work with previous work done on amplifier.

Parameters	Existing Design	Proposed Design
Technology used	130nm CMOS technology	65nm CMOS technology
Input voltage	Vin= 0.5V,	Vin=0.34V,
Output voltage	V_{out}=0.75V	V_{out}=0.43V
VDD Supply	2.5 Volt	0.8-1.2 Volt
Power	20.028dBm	20.09dBm
Efficiency	44.669%	81.90%

Table 5.5: Comparison of proposed work with existing design

6. Advantages

- Input signal voltage given is low.
- Power required by the amplifier to achieve higher efficiency is very less i.e. in the range of few micro watts.
- Area consumed by the network is very less.
- Higher speed, due to significantly reduced interconnection length.
- Significant cost savings

7. Limitation

- Parametric value can be changed in accordance with the supply voltage if technology is changed.

8. Applications

- It is used in WLAN Applications.
- It is used in Modulator.
- It is also used in Transmitter.
- It is used in Bluetooth Applications.

9. Conclusion

As 65 nm CMOS technology increases the switching speed of device which is mainly due to significantly reduced interconnection length therefore high output power with high efficiency is obtained using CMOS device for the power amplifier. As shown in the results this power amplifier dissipates low amount of power which is due to gate width is reducd and therefore is responsible for high efficiency. Efficiency can be increased or decreased depending on the power requirement.

In the proposed work , with the help of 65 nm CMOS technology two stage power amplifier is designed to achieve Output power of 20.09 dBm with efficiency of 81.09% , frequency of 2.6 GHz and gain is of 1.26 is obtained with supply voltage of 1.2 V.

10. Referances

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