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Effect of Interfacial Native Oxide in Sulphur Passivated N-Indium Phosphide MIS Capacitor with Anodic Oxide and PECVD Silicon Nitride as Gate Di-Electric

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Abstract:
This paper deals with the studies on the surface passivation of Indium phosphide (InP) using $(NH_4)_2S_x$ chemical treatment followed by anodic native oxidation and PECVD silicon nitride deposition. MIS capacitors fabricated on n-InP substrates are used as test vehicle for this study. Here MIS capacitors are fabricated by first treating the n-InP substrate with $(NH_4)_2S_x$ at 80^0 C followed by anodisation in an aqueous solution of tartaric acid and glycol, PECVD silicon nitride deposition for gate di-electric and alumunium metal for gate metal formation. The current – voltage (I-V) and capacitance – voltage (C-V) characteristics as well as breakdown voltage of these devices are obtained after sequential post metallization annealing carried out at temperatures in the range of 200^0 C to 450^0 C. MIS having anodic oxide thickness in the range 0 to 10nm are fabricated to study effects of the oxide thickness on the effectiveness of surface passivation. It is shown that the devices having an oxide thickness of 2nm show reduction in the Interface State density, frequency dispersion and hysterisis on C-V compared to the devices having no oxide layer or the devices with thicker oxide range.

Keywords*: PECVD, InP, Sulphur Passivation and nm.*

1. Introduction

Indium phosphide is a compound semiconductor material for its high speed and high-density integrated circuits. InP is a direct band gap material. Therefore it can be used for fabricating opto-electronic devices [3]. The wider energy gap of InP makes it attractive for operation at higher temperatures. InP has high electron mobility and high velocity overshoot effects than GaAs. The native oxide of Indium phosphide is largely beneficial in bringing down number of interface states, which is indicative of good interface properties. It is required to have good di-electric properties double di-electric layer consisting of native oxide and PECVD silicon nitride deposited on n-InP. Passivating the InP surface is needed prior to deposition of double di-electric layer. The literature survey clearly points out that passivation of InP surface with $(NH_4)_2S_X$ treated is an efficient and simple technique. To realize a MIS structure on $(NH_4)_2S_X$ treated InP samples, a di-electric film is required. For this purpose, Silicon nitride is chosen because it acts as an excellent barrier to humidity and mobile ions like sodium. When InP sample is treated With $(NH_4)_2S_X$ the excess sulphur in the inorganic compound bonds to indium and phosphorous on the surface reducing the dangling bonds, thus leading to reduction in interface state density. When the interface state density is reduced, the surface is said to be passivated and now becomes ideal for MIS device fabrication. In this paper following the introduction the description of wafer cleaning, metallization for back contact, $(NH_4)_2S_X$ treatment on n-InP sample, anodic oxidation with experimental set up and details of anodization, PECVD silicon nitride deposition and finally Al metallization are presented here. At last the interface state density D_{it} effects and their values are tabulated in table 3 and 4.

2 Details of Fabrication Steps of MIS Capacitor

Figure 1 shows the structure of MIS capacitor of InP semiconductor. The following steps gives the fabrication details [1].

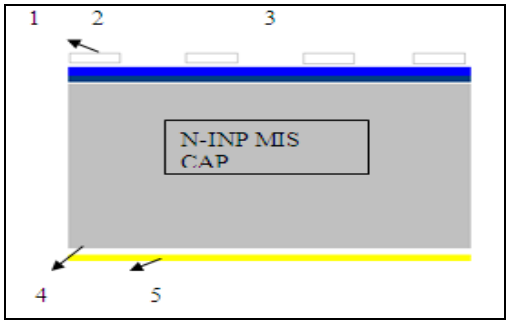

Figure 1: MIS InP capacitor structure

2.1. Steps for Fabrication

- Cleaning the InP wafers with TCE, Acetone and Blow with nitrogen jet.
- Au:ge Metallization and Al Metallization on one side of wafer.
- Anodic oxide on n-InP by constant voltage source method of various thickness 0 to 10 nm.
- Silicon Nitride Deposition on Oxide layer using PECVD
- Final Alumunium Metallization

2.2. Surface Passivation

The n- InP wafers are etched prior to surface passivation. Here the etchant used is 10% (NH_4) OH solution by volume in H_2O used for n-InP wafers. Prior to etching wafers are coated with PPR on backside to protect back contact (Au –Ge) from the etchants. Now the wafers are kept in post baking oven at 120^{o}C at 30 minutes. The front surface of sample is now etched in the etchant 10% (NH_4) OH for 60 seconds. After etching wafers are rinsed in DI water for two minutes. Finally wafers are warmed in acetone to remove PPR on back surface of the sample. Again the wafers are rinsed in DI water for 2 minutes and dried by giving nitrogen blow using air gun. Now InP wafers dipped in 50 ml solution of 40% $(NH_4)_2S_X$ solution taken in beaker. The beaker is kept in constant temperature bath, being controlled at a preset temperature controller. Here the sulphur treatment is done at 80^{o}C for 20 minutes duration. After keeping the beaker in the bath for determined duration, it is taken out of bath and DI water is poured 2 to 3 times into beaker to dilute the $(NH_4)_2S_X$ thoroughly so that all previously yellowish solution becomes crystal clear solution now [4] [5]. Then the samples are taken out safely and given exactly one minute DI water rinse. This one –minute is very important in achieving process consistency. The wafers are ready for anodic oxidation.

2.3 Anodic Oxidation & PECVD

Silicon nitride and Anodic oxide acts as double dielectric layer. Anodic oxide is carried out at room temperature using anodisation. Figure 1 shows Capacitance structure of MIS device. The purpose of any passivation is to retain the integrity of the surface under the passivating layer. Therefore passivation is successful, only if the electronic state of surface being passivated is invariant with time. It can be expected that passivation techniques would result in MIS device with long-term stable electrical characteristics. The anodisation can be carried out by constant current source or voltage source. In constant current source anodisation, the cell voltage increases linearly as function of time and saturates at a value supply by limited voltage. Here oxide thickness is linear function of time. The anodic oxides composed of In_2O_3 and P_2O_5 is thus formed

In this experiment anodic oxide thickness of 0,2 nm, 5nm, 10nm are fabricated on different n-type InP wafers respectively. After anodisation the Silicon nitride is deposited on the wafer and Alumunium metallization is done. Now the wafers are ready for characterization.

3. IV & CV Measurement of INP MIS Capacitor

The samples are probed for their I-V characteristics using parametric analyzer to check the devices leaky or not. C-V characteristics are also done using HP 4275 – LCR METER for 1 MHz frequency. The device that has proper I-V characteristics and low leakage current, are noted down. There are two sets of devices with annealing conditions

SET – I $(NH_4)_2 S_X$ treated, followed by anodic oxide thickness of different thickness and then PECVD SiN of thickness 47nm. The four wafers in the set having anodic oxide thickness as follows

1. t_{ox} = 0 2. . t_{ox} = 2nm 3. . t_{ox} = 5nm 4. . t_{ox} = 10nm along with 50nm SiN thickness.

SET – II - Same as SET I except in that all the four wafers, the PECVD SiN thickness is 100nm instead of 50 nm. Devices are annealed from 200^{o}c to 450^{o}c. in steps of 50^{o}c

3.1. I-V characteristics

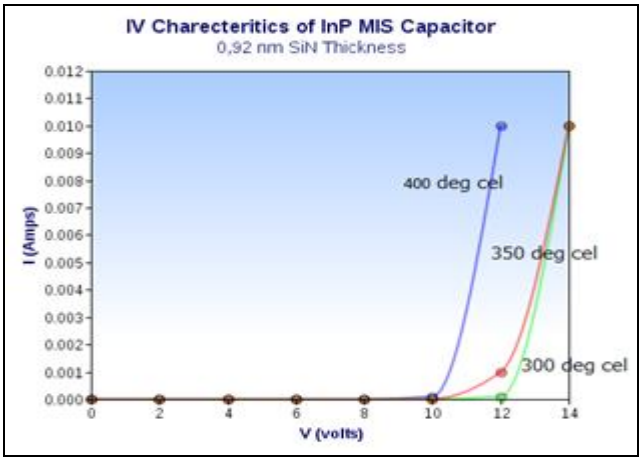

Figure 2: 2nm oxide thickness and 92 nm SiN thickness

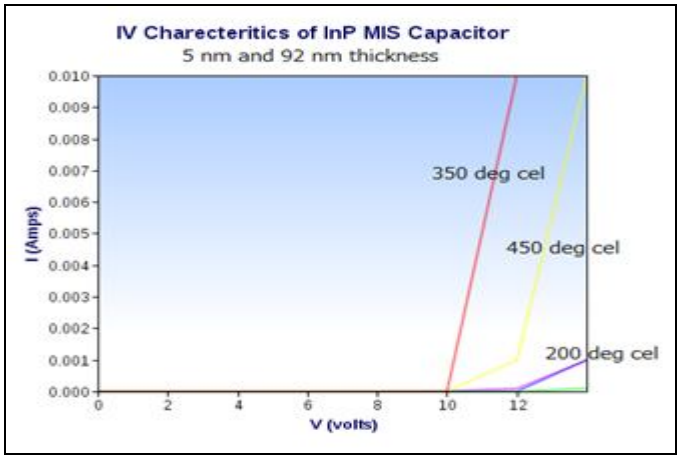

Figure 3: 2nm oxide thickness and 92 nm SiN thickness

Fig 2,3 I-V shows characteristics of 0 ,2 nm for anodic oxide thickness and 92 nm SiN thickness. The Leakage current – 1e-9 and breakdown voltage 11.5v for 300^{o}C PMA conditions are noted down.From the above figure it is found that leakage current is **2E-11** and breakdown voltage is 13v for 300^{o}C PMA and anodic oxide thickness is 5nm of 92 nm of SiN thickness. The other I-V curves for different values of anodic oxide thickness and SiN thickness are drawn; from the graph 5nm and 2nm anodic oxide thickness gives lower leakage current and higher breakdown voltage. Therefore MIS capacitor of less thickness of anodic oxide are useful for fabrication of MIS devices.

3.2. C-V Characteristics

The C-V curves of 0,2,5,10 nm anodic oxide thickness and 47, 92 nm of SiN thickness are drawn for 10 KHz and1MHz frequency. Here proper accumulation, depletion, inversion regions are noted down. From the C-V curves Interface state density, Frequency dispersion and Hysterisis can be calculated. Fig 4,5 shows C-V curves at 200^{0}C at 10 KHz,1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness. From the above graph curves are all not showing proper accumulation, depletion, inversion regions. Figure 6,7 shows C-V curves with appropriate accumulation, depletion, and inversion regions. But figure 7 shows with less hysterisis therefore anodic oxide thickness of 2nm and 92 nm of SiN thickness at 350 C PMA gives well-defined accumulation, inversion, and depletion regions. From the above curves frequency dispersion, Hysterisis, maximum capacitance and minimum capacitance are calculated and tabulated in table 1 as below. These parameters are helpful in finding the range of oxide and nitride thickness useful for fabrication of MIS devices of InP.

Table I gives Frequency dispersion (ratio of capacitance at 10KhZ freq to capacitance at 1 MhZ freq), Hysterisis and capacitance ratio of MIS devices. Frequency dispersion is useful for finding how much deviation in the curve at different frequency, so that smooth curve with less Frequency dispersion needed to study the C-V curves and regions. Hysterisis gives how much impurities affect curves. From the table I it is clear that 2nm devices exhibit low hysterisis and Frequency dispersion. Similarly for 92 nm SiN thickness 2nm anodic oxide gives good results.

4 Interface State Density – DIT Measurement

Capacitance and voltage values are calculated from MIS CAPACITOR using HP 4275 – LCR METER for 1 MHz frequency. From the graph interface surface density Dit is calculated from equation 1.

D_{it} is found from relation

$$D_{it} = 1/q \{ ((\Delta V_g / \Delta\phi_s) - 1) C_I - C_d \} \quad (1)$$

Different values of Dit vs surface potential is plotted and graphs are drawn in figure 8. Fig 8 Interface state density Vs surface potential (anodic oxide – 2 nm and SiN thickness – 47 nm) $\Delta\phi_s$ – Surface potential, C_i – Inversion capacitance and C_d – Depletion capacitance. It is found from the graph that 450^{o}C curve with 15 minutes PMA gives minimum interface state density – 6.012E12 /cm^{2}/ev. The results for other devices are tabulated in table 2.

5. Capacitance Values from C-V

Figure 4,5 – C-V characteristics of 200^{0}C at 10 KHz, 1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness.

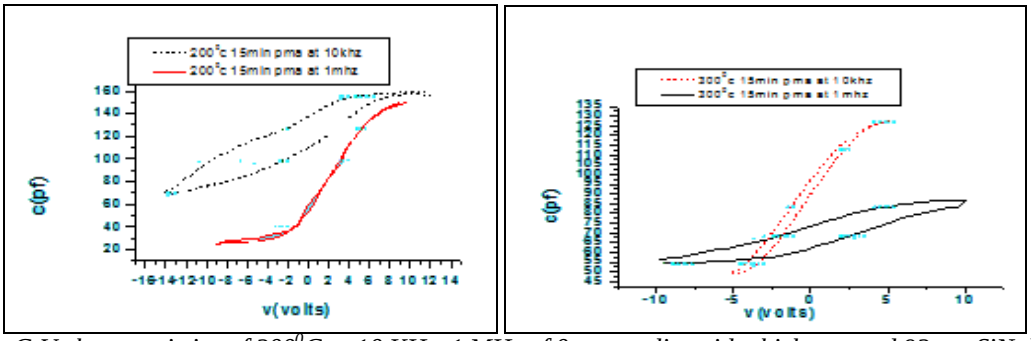

Figure 4: C-V characteristics of 200^{0}C at 10 KHz, 1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness.
Figure 5: C-V characteristics of 300^{0}C at 10 KHz, 1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness.

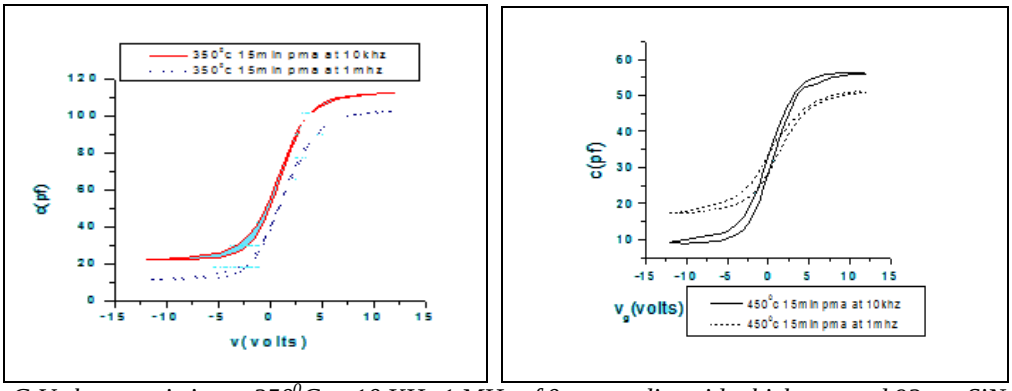

Figure 6: C-V characteristics at 350^{0}C at 10 KHz,1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness
Figure 7: C-V characteristics at 350^{0}C at 10 KHz,1 MHz of 0nm anodic oxide thickness and 92 nm SiN thickness

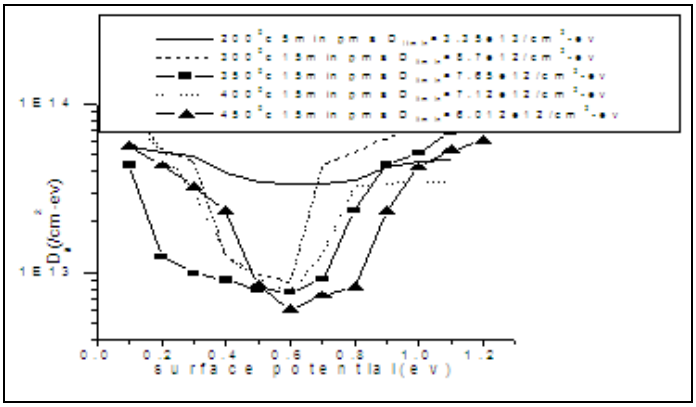

Figure 8 - Interface state density Vs surface potential (anodic oxide –2 nm and SiN thickness – 47 nm)

Below Table 3 and 4 gives the theoretical values and practical values of capacitance calculated from the C-V curves. Table 3 gives Comparison of MAXIMUM capacitance values of estimated and experimental values. From the Table 3 and 4 maximum and minimum capacitance values tabulated, It is found that 2nm anodic oxide thickness gives nearly matched values both estimated and experimented values. Experimented values are calculated from C-V curves directly Extracted values from capacitance relation (Cd, Ci, C) [6].

6. Conclusion

- Anodic oxide thickness of 2nm, 5 nm with 92nm and 47 nm of SiN as low leakage current and high breakdown voltage.
- From the C-V characteristics obtained in all devices, it is observed that after Post Metallization Annealing at 350^{o}C gives better C-V characteristics than other curves.
- MIS capacitors fabricated with 2nm oxide thickness show a reduction in the interface state density.
- Frequency dispersion and Hysterisis also low for 2nm oxide thickness.

Therefore the best results of InP MIS devices can be achieved when they are fabricated with 2nm Anodic oxide thickness with sulphur passivation. The results also indicated that optimum PMA plays important role in reducing Interface state density.

PASSIVATED 20 MIN AT 80^{O}C - FREQ AT 1 MhZ					
SiN THICKNESS (nm)	**OXIDE THICKNESS (nm)**	**PMA C CONDITIONS (^{O}C)**	**C_M /$C_{MAX(}$**	**$C_{M(10K)}$ / $C_{MAX(1M)}$ FREQ DISPERSION**	**HYSTERISIS (VOLTS)**
SiN –47	0	200^{O}C 15MIN PMA	1.3	1.32	3.9 to 7.4
		300^{O}C 15MIN PMA	4	1.003	3.6 to 7.2
		350^{O}C 15MIN PMA	3.93	1.1	2.9 to 4.9
		400^{O}C 15MIN PMA	4.77	1.04	2 to 4.6
		450^{O}C 15MIN PMA	6.2	1.16	1.8 to 2.9
	2	200^{O}C 15MIN PMA	3.4	**1.035**	1.5 to 4.2
		300^{O}C 15MIN PMA	2.08	1.09	1.1 to 3.7
		350^{O}C 15MIN PMA	4.66	1.64	**2.3 to 3.2**
		400^{O}C 15MIN PMA	8.5	1.3	1.1 to 6.3
		450^{O}C 15MIN PMA	3.9	1.72	1.4 to 2.5
	5	200^{O}C 15MIN PMA	6.3	1.42	3.3 to 6.3
		300^{O}C 15MIN PMA	13.7	1.08	2.6 to 6.7
		350^{O}C 15MIN PMA	4.38	1.82	5.1 to 8.9
		400^{O}C 15MIN PMA	8.6	1.043	.7 to 2.16
		450^{O}C 15MIN PMA	8.6	1.072	3.4 to 4.9
	10	200^{O}C 15MIN PMA	5.1	1.17	3 to 6.1
		300^{O}C 15MIN PMA	25	1.1	2.8 to 6.9
		350^{O}C 15MIN PMA	4.7	1.532	3.3 to 4
		400^{O}C 15MIN PMA	4.36	1.078	1.9 to 3.5
		450^{O}C 15MIN PMA	6.2	1.306	2.8 to 4

Table 1: Frequency dispersion, capacitance ratio, Hysterisis of InP MIS Device employing passivation with different anodic oxide thickness and SiN thickness of 47 nm.

SiN THICKNESS (nm)	OXIDE THICKNESS (nm)	PMA CONDITIONS	Dit (/cm^2/ev)
SET – I SiN – 92 nm	0	200^{o}C – 5 min PMA	4.41E13
		300^{o}C – 5 min PMA	2.92E13
		350^{o}C – 5 min PMA	3.41E13
		400^{o}C – 5 min PMA	4.03E13
		450^{o}C – 5 min PMA	5.48E13
	2	200^{o}C – 5 min PMA	3.32E13
		300^{o}C – 5 min PMA	8.7E12
		350^{o}C – 5 min PMA	6.75E12
		400^{o}C – 5 min PMA	7.12112
		450^{o}C – 5 min PMA	**6.012E12**
	5	200^{o}C – 5 min PMA	1.01E13
		300^{o}C – 5 min PMA	1.1E13
		350^{o}C – 5 min PMA	3.46E13
		400^{o}C – 5 min PMA	3.12E13
		450^{o}C – 5 min PMA	4.14E13
	10	200^{o}C – 5 min PMA	2.99E13
		300^{o}C – 5 min PMA	2.34E13
		350^{o}C – 5 min PMA	4.22E13
		400^{o}C – 5 min PMA	3.8E13

Table 2: Values of interface state density of SiN thickness – 47nm

ANODIC OXIDE THICKNESS (nm)	SiN THCKNESS (nm)	Cmax ESTIMATED VALUE(pf)	Cmax EXPERIMENTAL VALUE (pf)
0	47	258	172
	92	132	130
2	47	**245**	**244**
	92	**126**	**128**
5	47	224	95
	92	122	102
10	47	197	140
	92	114	55

Table 3: Comparison of MAXIMUM capacitance values of estimated and experimental values

ANODIC OXIDE THICKNESS (nm)	SiN THCKNESS (nm)	Cmin ESTIMATED VALUE (pf)	Cmin EXPERIMENTAL VALUE (pf)
0	47	35	40
	92	31	20
2	47	**34**	**30**
	92	**30**	**31**
5	47	34	23
	92	31	33

Table 4: Comparison of MINIMUM capacitance values of estimated and experimental

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