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Online Built-In-Self Test Architecture Using SRAM Cells

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Abstract:
In this brief, we present a novel input vector monitoring concurrent BIST scheme, which is based on the idea of monitoring a set (called window) of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the relative location of the vectors that reach the circuit inputs in the examined window; the proposed scheme is shown to perform significantly better than previously proposed schemes with respect to the hardware overhead and concurrent test latency (CTL) trade off. In this paper two methods will be discussed, window monitoring concurrent bist and input vector monitoring concurrent bist using sram,

Keywords*: Built-in-selftest, design for testability, testing, window monitoring bist.*

1. Introduction

BIST is a design-for-testability technique that places the testing functions physically with the circuit under test (CUT). The basic BIST architecture requires the addition of three hardware blocks to a digital circuit: a test pattern generator, a response analyzer, and a test controller. The test pattern generator generates the test patterns for the CUT. Examples of pattern generators are a ROM with stored patterns, a counter, and a linear feedback shift register (LFSR). A typical response analyzer is a comparator with stored responses or an LFSR used as a signature analyzer. It compacts and analyzes the test responses to determine correctness of the CUT. A test control block is necessary to activate the test and analyze the responses. However, in general, several test-related functions can be executed through a test controller circuit.

In normal operation, the CUT receives its inputs from other modules and performs the function for which it was designed. During test mode, a test pattern generator circuit applies a sequence of test patterns to the CUT, and the test responses are evaluated by a output response compactor. In the most common type of BIST, test responses are compacted in output response compactor to form (fault) signatures. The response signatures are compared with reference golden signatures generated or stored on-chip, and the error signal indicates whether chip is good or faulty. Four primary parameters must be considered in developing a BIST methodology for embedded systems; these correspond with the design parameters for on-line testing techniques. BIST can be used for non-concurrent, on-line testing of the logic and memory parts of a system.

It can readily be configured for event-triggered testing, in which case, the BIST control can be tied to the system reset so that testing occurs during system start-up or shutdown. BIST can also be designed for periodic testing with low fault latency. This requires incorporating a testing process into the CUT that guarantees the detection of all target faults within a fixed time. On-line BIST is usually implemented with the twin goals of complete fault coverage and low fault latency.

2. Window Monitoring Concurrent Bist

Window monitoring concurrent bist is one type of bist. W-MCBIST is based on the separation of the test set into non-overlapping subsets called windows. Each one of size ws=2^w where 0<w<n

2.1. BIST Architecture

The normal operation of window monitoring concurrent bist exploits the arrival of any test vector belonging to a specific window called active window. The input vector is compared against a set of ws vectors that constitute the active as follows. n-wbits of a n-bit input vector are compared with the output of the test generator and if they match cmp is enabled. The remaining w bits of the input

vector are driven to the inputs of a wxWS decoder whose enable in driven by cmp. Therefore, if the input vector belongs to the active window, one of the D[i] signals is enabled. When al vectors of a window have performed a hit, that signal test generator enable (tge) triggers the test generator to the next state ,in order to examine a new window. After the test generator has generated al its 2^n-w states, we examine the signature captured in RV and decided whether the CUT is faulty.
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2.2. Technique of Window Monitoring Concurrent BIST
The logic module consists of Ws logic cells .Each logic cells[i],1<i<Ws, corresponds to a vector that belongs to the active window and can be either empty or full, depending on whether the corresponding vector has reached the CUT inputs during the examination of the current active window. This is indicated by the value of the signal full. When all logic cells are full, the signal tge is enabled, at the next clock cycle, all cells are emptied and the next active window is examined.

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2.3. Logic Module
The Window monitoring concurrent bist can switch from normal to test mode. If at time some of the vectors belonging to the current window have reached the CUT inputs, the remaining vectors of the current active window are applied offline before proceeding to examine the next window. The response verifier compresses the CUT outputs. Since in W-MCBIST the order of the vectors that perform hit during the examination of the window is not fixed.
The final signature must be independent of the order of the output vectors of the CUT. Thus, an order –independent RV is used with Window monitoring concurrent BIST. The accumulator –based compaction is an order-independent response verification technique that has been shown to have aliasing properties similar to the best compactors based on cellular automata and multiple input signature registers and is utilized with Window monitoring concurrent BIST.

3. SRAM Cells

The module is reset through the external reset signal. When reset is issued, the tge signal is enabled and all the outputs of the decoder are enabled. The CD signal is enabled therefore, a one is written to the right hand side of the cells and a zero value to the left hand side of the cells. The normal mode, the inputs to the CUT is driven from the normal inputs. The n inputs are also driven to the CBU as follows the w low-order inputs are driven to the inputs of the decoder; the k high-order inputs are driven to the inputs of the comparator. During the first half of the clock cycle (clk and cmp are enabled) the addressed cell is read; because the read value is zero, the w-stage counter is triggered through the NOT gate with output the response verifier enable (rve) signal. During the second half of the clock cycle, the left flip-flop (the one whose clock input is inverted) enables the AND gate (whose other input is clk and cmp), and enables the buffers to write the value one to the addressed cell. If the cell corresponding to the incoming vector contains a one i.e., the respective vector has reached the CUT inputs during the examination of the current window before. The rve signal is not enabled during the first half of the clock cycle; hence, the w-stage counter is not triggered and the AND gate is not enabled during the second half of the clock cycle. When all the cells are full (value equal to one), then the value of the w-stage counter is all one. Hence, the activation of the rve signal causes the counter to overflow; hence in the next clock cycle(through the unit flop delay) the tge signal is enabled and all the cells(because all the outputs of the decoder are enabled are set to zero.
When switching from normal to test mode, the w-stage counter is reset. During test mode, the w-bit output of the counter is applied to the CUT inputs. The outputs of the counter are also used to address a cell. If the cell was empty (reset), it will be filled (set) and the RV will be enabled. Otherwise, the cell remains full and the RV is not enabled. Accumulator based compaction method is used to reduce the concurrent test latency and hardware overhead.

4. Simulation Results

The simulation results will be shown for both window monitoring concurrent bist and Sram cells. The waveform will be shown in below .ROM modules will be tested in varies size,16k,64k,128k,256k for window monitoring concurrent bist and Sram cells. The flow summary will be shown how many logical elements will be used and propagation delay. The below waveform is for 16k ROM for window monitoring concurrent bist.

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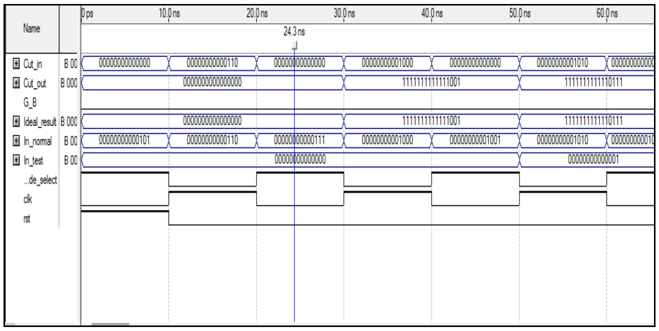


Figure 1: Simulation result for 16K ROM in window monitoring concurrent BIST.

The waveform will be generated based on the mode select.If the mode select will be zero,the normal mode values are generated in the CUT input.The cut output is produced and it is equal to the ideal result.The GB will be zero when the cut output is not equal to ideal result.The GB will be one when the cut output is equal to ideal result.Similarly the waveform for 64K ROM for window monitoring concurrent bist is shown below.

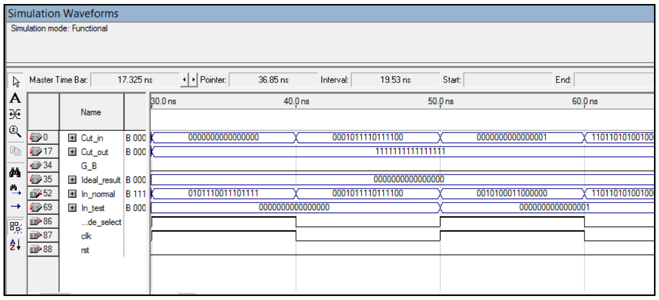

Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 17.325 ns Pointer: 36.85 ns Interval: 19.53 ns Start: End:
Name
30.0 ns
40.0 ns
50.0 ns
60.0 ns
0 Cut_in B 000 0000000000000000 0001011110111100 0000000000000001 11011010100100
17 Cut_out B 000 1111111111111111
34 G_B
35 Ideal_result B 000 0000000000000000
52 In_normal B 111 0101110011101111 0001011110111100 0010100011000000 11011010100100
69 In_test B 000 0000000000000000 0000000000000001
86 ...de_select
87 clk
88 rst

Figure 2: Simulation result for 64K ROM in window monitoring concurrent BIST.

ROM modules will be tested in SRAM cells and the simulation results will be obtained. SRAM cells will be more efficient compare to window monitoring concurrent BIST. The simulation results for 16K ROM in SRAM cells will be shown below.

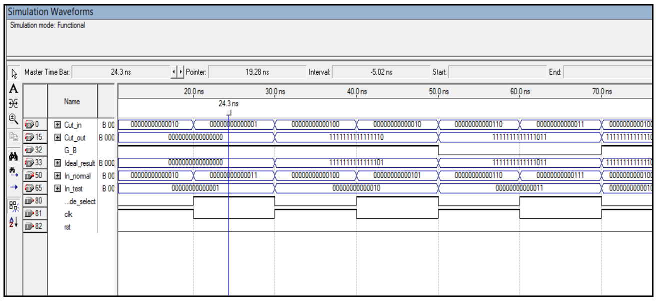

Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 24.3 ns Pointer: 19.28 ns Interval: -5.02 ns Start: End:
Name
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
24.3 ns
0 Cut_in B 00 00000000000010 00000000000001 00000000000100 00000000000010 00000000000110 00000000000011 0000000000100
15 Cut_out B 000 0000000000000000 1111111111111110 1111111111111011 111111111111110
32 G_B
33 Ideal_result B 000 0000000000000000 1111111111111101 1111111111111011 111111111111110
50 In_normal B 00 00000000000010 00000000000011 00000000000100 00000000000101 00000000000110 00000000000111 0000000000100
65 In_test B 00 00000000000001 00000000000010 00000000000011 0000000000010
80 ...de_select
81 clk
82 rst

Figure 3: Simulation results for 16K ROM in SRAM cells.

The waveform will be generated based on the mode select.If the mode select will be zero,the normal mode values are generated in the CUT input.The cut output is produced and it is equal to the ideal result.The GB will be zero when the cut output is not equal to ideal result.The GB will be one when the cut output is equal to ideal result.Similarly the waveform for 64K ROM for SRAM cells BIST is shown below.

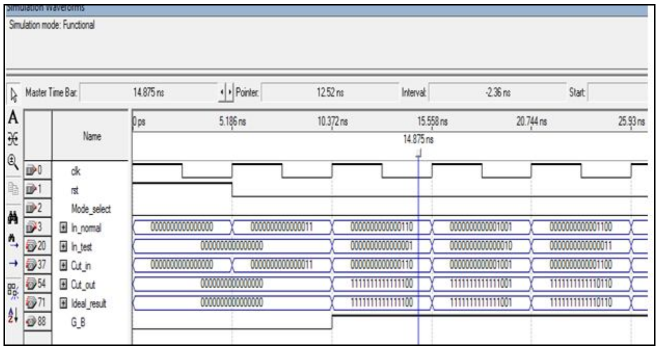

Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 14.875 ns Pointer: 12.52 ns Interval: -2.36 ns Start:
Name
0 ps
5.186 ns
10.372 ns
15.558 ns
20.744 ns
25.93 ns
14.875 ns
0 clk
1 rst
2 Mode_select
3 In_normal 0000000000000000 0000000000000011 0000000000000110 0000000000001001 0000000000001100
20 In_test 0000000000000000 0000000000000001 0000000000000010 0000000000000011
37 Cut_in 0000000000000000 0000000000000011 0000000000000110 0000000000001001 0000000000001100
54 Cut_out 0000000000000000 1111111111111100 1111111111111001 1111111111110110
71 Ideal_result 0000000000000000 1111111111111100 1111111111111001 1111111111110110
88 G_B

Figure 4: Simulation results for 16K ROM (Normal mode) in SRAM cells

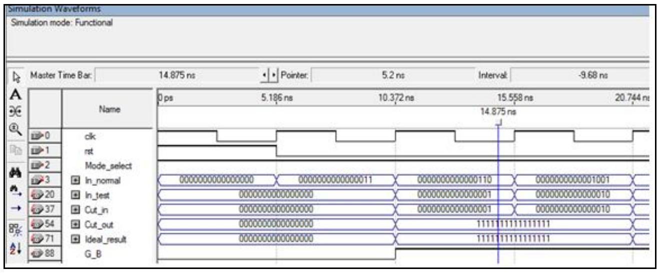
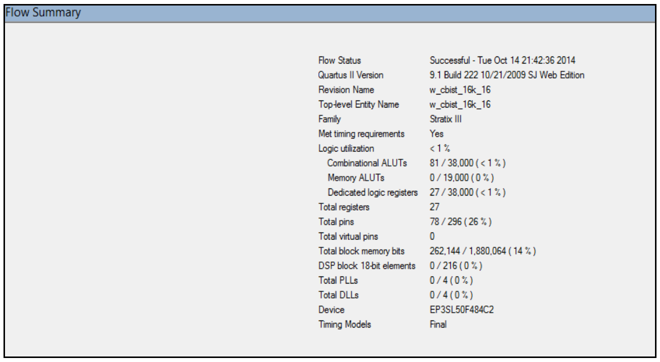

Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 14.875 ns Pointer: 5.2 ns Interval: -9.68 ns
Name
0 ps
5.186 ns
10.372 ns
15.558 ns
20.744 ns
14.875 ns
0 clk
1 rst
2 Mode_select
3 In_normal 0000000000000000 0000000000000011 0000000000000110 0000000000001001
20 In_test 0000000000000000 0000000000000001 0000000000000010
37 Cut_in 0000000000000000 0000000000000001 0000000000000010
54 Cut_out 0000000000000000 1111111111111111
71 Ideal_result 0000000000000000 1111111111111111
88 G_B

Figure 5: Simulation results for 64K ROM (Test mode) in SRAM cells

5. Flow Summary

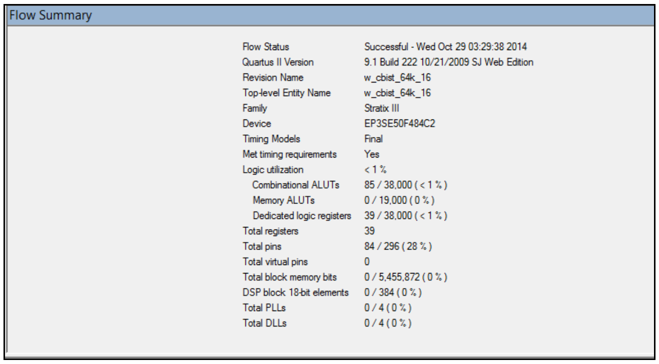
The flow summary will give all the information about the process. It shows the number of combinational ALUTs, memory ALUTs, dedicated logic registers. The total block memory bits, total registers, total pins also shown.



```
Flow Status                    Successful - Tue Oct 14 21:42:36 2014
Quartus II Version             9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name                  w_cbist_16k_16
Top-level Entity Name          w_cbist_16k_16
Family                         Stratix III
Met timing requirements        Yes
Logic utilization              < 1 %
    Combinational ALUTs        81 / 38,000 ( < 1 % )
    Memory ALUTs               0 / 19,000 ( 0 % )
    Dedicated logic registers  27 / 38,000 ( < 1 % )
Total registers                27
Total pins                     78 / 296 ( 26 % )
Total virtual pins             0
Total block memory bits        262,144 / 1,880,064 ( 14 % )
DSP block 18-bit elements      0 / 216 ( 0 % )
Total PLLs                     0 / 4 ( 0 % )
Total DLLs                     0 / 4 ( 0 % )
Device                         EP3SL50F484C2
Timing Models                  Final
```

Figure 6: Flow summary for 16k ROM in window monitoring concurrent BIST.

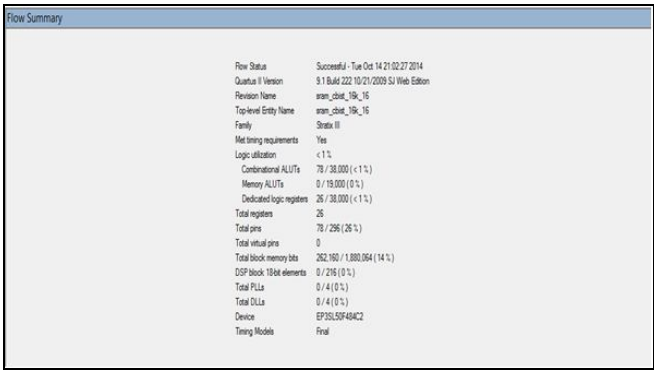
The tota l logic elements, which is used for window monitoring concurrent bist in 16k ROM is 81 out of 38,000 logic elements. The total logical registers used for 16K ROM in window monitoring concurrent bist is 27 out of 38,000.The total pins used for 16K ROM in window monitoring concurrent bist is 78 out of 296.The total block memory bits used in 16K ROM is 262,144 out of 1,880,064. The flow summary for 64K ROM in window monitoring concurrent BIST is shown below.



```
Flow Status                    Successful - Wed Oct 29 03:29:38 2014
Quartus II Version             9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name                  w_cbist_64k_16
Top-level Entity Name          w_cbist_64k_16
Family                         Stratix III
Device                         EP3SE50F484C2
Timing Models                  Final
Met timing requirements        Yes
Logic utilization              < 1 %
    Combinational ALUTs        85 / 38,000 ( < 1 % )
    Memory ALUTs               0 / 19,000 ( 0 % )
    Dedicated logic registers  39 / 38,000 ( < 1 % )
Total registers                39
Total pins                     84 / 296 ( 28 % )
Total virtual pins             0
Total block memory bits        0 / 5,455,872 ( 0 % )
DSP block 18-bit elements      0 / 384 ( 0 % )
Total PLLs                     0 / 4 ( 0 % )
Total DLLs                     0 / 4 ( 0 % )
```

Figure 7: Flow summary for 64k ROM in window monitoring concurrent BIST.

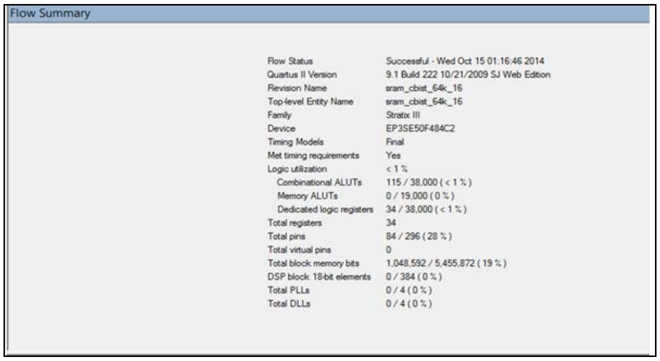
The tota l logic element which is used for window monitoring concurrent bist in 64k ROM is 85 out of 38,000 logic elements. The total logical registers used for 64K ROM in window monitoring concurrent bist is 39 out of 38,000.The total pins used for 64K ROM in window monitoring concurrent bist is 84 out of 296. Similarly the flow summary for 16K ROM in SRAM cells is shown below.



```
Flow Status                    Successful - Tue Oct 14 21:02:27 2014
Quartus II Version             9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name                  sram_cbist_16k_16
Top-level Entity Name          sram_cbist_16k_16
Family                         Stratix III
Met timing requirements        Yes
Logic utilization              < 1 %
    Combinational ALUTs        78 / 38,000 ( < 1 % )
    Memory ALUTs               0 / 19,000 ( 0 % )
    Dedicated logic registers  26 / 38,000 ( < 1 % )
Total registers                26
Total pins                     78 / 296 ( 26 % )
Total virtual pins             0
Total block memory bits        262,160 / 1,880,064 ( 14 % )
DSP block 18-bit elements      0 / 216 ( 0 % )
Total PLLs                     0 / 4 ( 0 % )
Total DLLs                     0 / 4 ( 0 % )
Device                         EP3SL50F484C2
Timing Models                  Final
```

Figure 8: Flow summary for 16k ROM in SRAM cells

The tota l logic elements, which is used for SRAM cells in 16k ROM is 78 out of 38,000 logic elements. The total logical registers used for 16K ROM in SRAM cells is 26 out of 38,000.The total pins used for 16K ROM in window monitoring concurrent bist is 78 out of 296. The total block memory bits used in 16K ROM is 262,120 out of 1,880,064
In SRAM cells.The flow summary for 64K ROM in SRAM cells is shown below.



Flow Summary

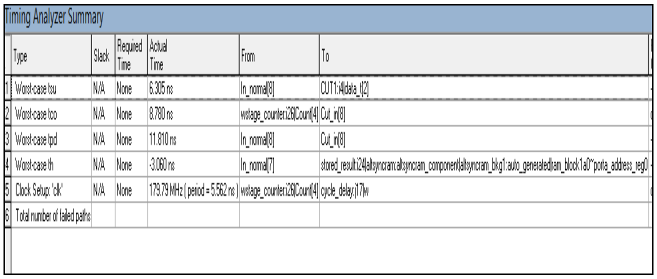
Flow Status	Successful - Wed Oct 15 01:16:46 2014
Quartus II Version	9.1 Build 222 10/21/2009 SJ Web Edition
Revision Name	sram_cbist_64k_16
Top-level Entity Name	sram_cbist_64k_16
Family	Stratix III
Device	EP3SE50F484C2
Timing Models	Final
Met timing requirements	Yes
Logic utilization	< 1 %
Combinational ALUTs	115 / 38,000 (< 1 %)
Memory ALUTs	0 / 19,000 (0 %)
Dedicated logic registers	34 / 38,000 (< 1 %)
Total registers	34
Total pins	84 / 296 (28 %)
Total virtual pins	0
Total block memory bits	1,048,592 / 5,455,872 (19 %)
DSP block 18-bit elements	0 / 384 (0 %)
Total PLLs	0 / 4 (0 %)
Total DLLs	0 / 4 (0 %)

Figure 9: Flow summary for 64k ROM in SRAM cells

The total logic element which is used for SRAM cells in 64k ROM is 115 out of 38,000 logic elements. The total logical registers used for 64K ROM in SRAM cells is 34 out of 38,000.The total pins used for 64K ROM in SRAM is 84 out of 296. The total block memory bits used in 64K ROM is 1,048,592 out of 5,455,872 in SRAM cells.

6. Timing Analyzer

Timing analysis report provides the propagation delay time used for window monitoring concurrent bist for 16k ROM of maximum operating frequency 179.79MHZ is 5.562ns without any failed paths. The timing ananlyzer for window monitoring concurrent bist for 16k ROM is shown in below diagram.

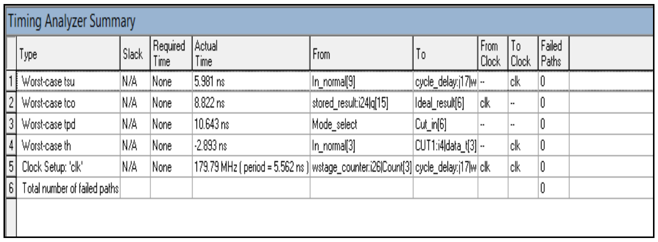


Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	6.305 ns	In_normal[8]	CUT1:i4|data_t[2]
2	Worst-case tco	N/A	None	8.780 ns	wstage_counter:i26|Count[4]	Cut_in[8]
3	Worst-case tpd	N/A	None	11.810 ns	In_normal[8]	Cut_in[8]
4	Worst-case th	N/A	None	-3.060 ns	In_normal[7]	stored_result:i24|altsyncram:altsyncram_component|altsyncram_bkg1:auto_generated|ram_block1a0~porta_address_reg0
5	Clock Setup: 'clk'	N/A	None	179.79 MHz (period = 5.562 ns)	wstage_counter:i26|Count[4]	cycle_delay:j17|w
6	Total number of failed paths					

Table 1: Timing analyzer report for 16K ROM in window monitoring concurrent BIST

For 64K ROM ,the timing analysis report provides the propagation delay time used in window monitoring concurrent BIST is also same as maximum operating frequency 179.79MHZ is 5.562ns without any failed paths. The timing ananlyzer for window monitoring concurrent bist for 64k ROM is shown in below diagram.

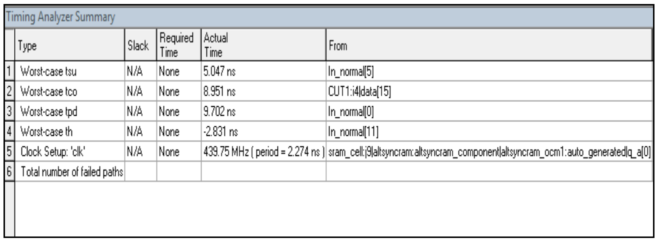


Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	5.981 ns	In_normal[9]	cycle_delay:j17|w	--	clk	0
2	Worst-case tco	N/A	None	8.822 ns	stored_result:i24|q[15]	Ideal_result[6]	clk	--	0
3	Worst-case tpd	N/A	None	10.643 ns	Mode_select	Cut_in[6]	--	--	0
4	Worst-case th	N/A	None	-2.893 ns	In_normal[3]	CUT1:i4|data_t[3]	--	clk	0
5	Clock Setup: 'clk'	N/A	None	179.79 MHz (period = 5.562 ns)	wstage_counter:i26|Count[3]	cycle_delay:j17|w	clk	clk	0
6	Total number of failed paths								0

Table 2: Timing analyzer report for 64K ROM in window monitoring concurrent BIST

The propagation delay time used for SRAM cells for 16k ROM of maximum operating frequency 179.79MHZ is 5.562ns without any failed paths. The timing ananlyzer for SRAM cells for 16k ROM is shown in below diagram.

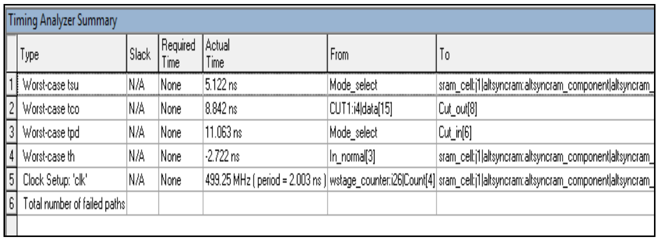


Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From
1	Worst-case tsu	N/A	None	5.047 ns	In_normal[5]
2	Worst-case tco	N/A	None	8.951 ns	CUT1:i4|data[15]
3	Worst-case tpd	N/A	None	9.702 ns	In_normal[0]
4	Worst-case th	N/A	None	-2.831 ns	In_normal[11]
5	Clock Setup: 'clk'	N/A	None	439.75 MHz (period = 2.274 ns)	sram_cell:j9|altsyncram:altsyncram_component|altsyncram_ocm1:auto_generated|q_a[0]
6	Total number of failed paths				

Table 3: Timing analyzer report for16K ROM in SRAM cells

The propagation delay time used for SRAM cells for 64k ROM of maximum operating frequency 499.25MHZ is 2.003ns without any failed paths. The timing analyzer for SRAM cells for 64k ROM is shown in below diagram.



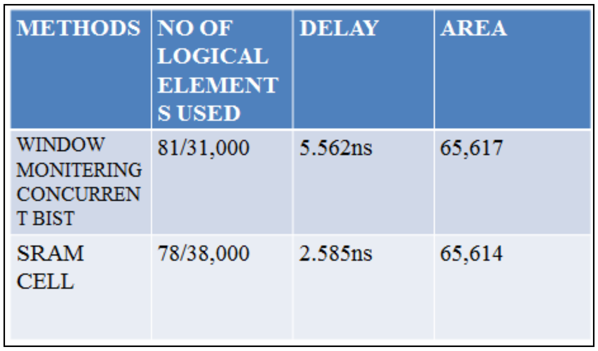
Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	5.122 ns	Mode_select	sram_cell:j1|altsyncram:altsyncram_component|altsyncram_
2	Worst-case tco	N/A	None	8.842 ns	CUT1:i4|data[15]	Cut_out[8]
3	Worst-case tpd	N/A	None	11.063 ns	Mode_select	Cut_in[6]
4	Worst-case th	N/A	None	-2.722 ns	In_normal[3]	sram_cell:j1|altsyncram:altsyncram_component|altsyncram_
5	Clock Setup: 'clk'	N/A	None	499.25 MHz (period = 2.003 ns)	wstage_counter:i26|Count[4]	sram_cell:j1|altsyncram:altsyncram_component|altsyncram_
6	Total number of failed paths					

Table 4: Timing analyzer report for 64K ROM in SRAM cells

7. Comparison Table

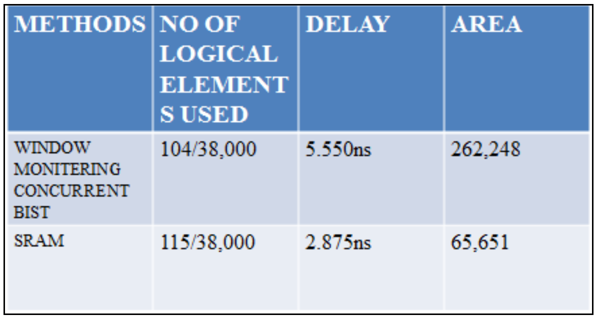
Comparison table shows the logical elements used for both the window monitoring concurrent bist and input vector monitoring concurrent BIST using sram cells.It also shows the propagation delay for 16k ,64k.



METHODS	NO OF LOGICAL ELEMENTS USED	DELAY	AREA
WINDOW MONITERING CONCURRENT BIST	81/31,000	5.562ns	65,617
SRAM CELL	78/38,000	2.585ns	65,614

Table 5: Comparison Table for 16 K ROM for window monitoring concurrent bist and SRAM cells.

For 16K ROM, the number of logical elements used in window monitoring concurrent BIST is 81 out of 31,000.The number of logical elements used in SRAM cells is 78 out of 38,000.The propagation delay obtained in window monitoring concurrent BIST is 5,562ns.The propagation delay obtained in SRAM cells is 2.585ns.The area obtained in window monitoring concurrent bist is 65,617.The area obtained in SRAM cells is 65,614.



METHODS	NO OF LOGICAL ELEMENTS USED	DELAY	AREA
WINDOW MONITERING CONCURRENT BIST	104/38,000	5.550ns	262,248
SRAM	115/38,000	2.875ns	65,651

Table 6: .Comparison Table for 64K ROM for window monitoring concurrent bist and SRAM cells.

For 64K ROM, the number of logical elements used in window monitoring concurrent BIST is 104 out of 31,000.The number of logical elements used in SRAM cells is 115 out of 38,000.The propagation delay obtained in window monitoring concurrent BIST is 5.550ns.The propagation delay obtained in SRAM cells is 2.875ns.The area obtained in window monitoring concurrent bist is 262,248.The area obtained in SRAM cells is 65,651.

8. Conclusion

The window monitoring concurrent BIST and input vector monitoring concurrent BIST using SRAM cells have been implemented on QUARTUS II 9.1.The propagation delay for 64K ROM will be shown in SRAM cells is2.875ns.It is therefore seen that the online build- in- self test using SRAM cells is superior with respect to delay and area when compared to window monitoring concurrent BIST. The online –build- in self-test will reduce more delay when compared to offline BIST. Accumulator based compaction method is used to reduce the delay, area and hardware requirements.

9. References

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