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Design and Implementation of Alias-Locked Loop in 90nm Technology for RF Applications

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Abstract:
Contemporary digital systems use clocks for sequencing their operations and for synchronization among its functional block units. Clock frequencies and data transfer rates have been constantly increasing with every generation of processing technology. Phase locked-loops (PLLs) are widely used in order to generate well -timed on-chip clocks to be used in high performance digital systems. A PLL is a closed loop system in which that locks the phase of its output signal to an input reference signal. In the devices like computer, radio and telecommunications systems PLL's are widely used, where it is necessary to stabilize a generated signal or to detect incoming signals. Advances in CMOS technology permits realization of high speed and low noise integrated frequency synthesizers and reduction in system costs.
The Phase-locked Loop (PLL) is referred to as an alias-locked loop (ALL) if it uses an aliasing divider in its feedback loop. With the use of an aliasing divider, the ALL architecture makes it possible to create high-speed frequency synthesis circuits without relying on a traditional divider clocked at fVCO in the feedback loop. In this design, I used five stage current starved VCO which provides both a high oscillating frequency and a wide tuning range. Here ALL is designed in 90-nm CMOS technology which locks the reference signal and the feedback signal i.e., VCO output in the range of 200MHz to 12.5GHz which consumes a power of 0.331mw with a supply voltage of 1.8v.
The schematics are designed and simulated using Cadence Virtuoso® Editor and Spectre® Simulator.

Keywords: *Alias locked loop (ALL), phase locked loop (PLL), voltage controlled oscillator (VCO).*

1. Introduction

The electronics industry has achieved a phenomenal growth over the last two decades, due to the rapid advances in integrated technology, large-scale systems design - in short, due to the advent of VLSI. The steady increase has been achieved in high performance computing, telecommunication and consumer electronics at a very high face because of the no applications in integrated circuits. Typically, the required computational power (or, in other words, the intelligence) of these applications is the driving force for the fast development of this field. Phase locked loop, popularly known as phase-locked loop (PLL) is one of the important constituent of modern electronic systems. Having wide range of applications over a broad frequency spectrum PLL has become one of the most essential element in microprocessor boards of complex systems, wired and wireless communication systems and many other systems. The phase-locked loop (PLL) is a critical component in many circuits and systems as it provides the timing basis for functions such as clock control, data recovery, and Synchronization. In a traditional PLL implementation, a divider in the feedback path converts higher frequencies to lower frequencies. Unfortunately, a traditional divider in PLL is based on flip-flops and will not work at such high frequencies. Designers usually resort to regenerative dividers or injection locked dividers to extend the operating frequency of their devices. However, both injection locked dividers and regenerative dividers typically rely on shunt peaking inductors that cost large areas and have limited tuning range. To alleviate this problem, a new frequency synthesizer architecture, the alias-locked loop (ALL), was proposed.

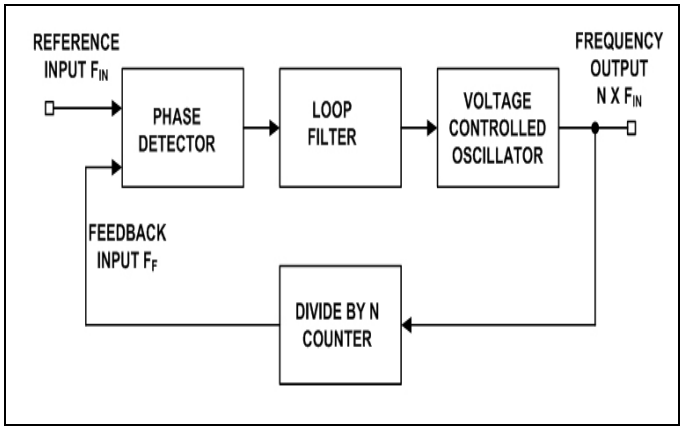

Figure 1: Proposed PLL Architecture

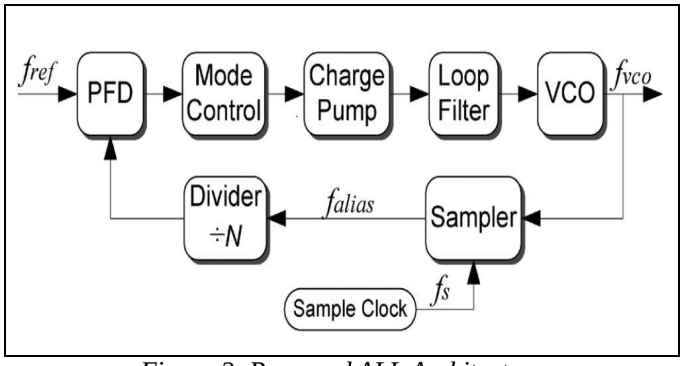

Figure 2: Proposed ALL Architecture

In the Alias Locked Loop (ALL) architecture, the traditional divider is replaced by an aliasing divider, implemented with a high speed digital sampling latch, although a D flip-flop (D-FF) can be used. This sampling circuit uses a stable reference clock to sample the voltage-controlled oscillator (VCO) signal. Since the sampling frequency is significantly lower than the sampled signal, the voltage-controlled oscillator (VCO) signal will be sub-sampled, creating an alias divided frequency. In this way the high frequency of the output signal of the VCO can be lowered, which in turn can be fed into a CMOS divider or directly to a conventional phase-frequency detector (PFD).

2. Background

Fig. 2 shows a general structure of an ALL. Most of the modules in an ALL are the same as that of PLL. A phase-frequency detector (PFD) compares the phase (frequency) of the reference clock with the feedback signal and then generates a control signal for a charge pump and then charge pump converts the phase difference to current that controls the charging or discharging operation of the capacitor in the loop filter, thereby the control voltage of the VCO is tuned. Differently from a traditional PLL, however, the divider-by-N between the VCO and the PFD is replaced by a high speed sampling circuit. In addition, a divider is applied after the sampling circuit. an alias locked loop is able to lock the desired frequency after a period of time. As shown in Fig. 1, the output of the VCO is subsampled with a pulse clock, whose frequency is much lower than the VCO signal. The output of the sampling circuit is a so-called alias signal of the VCO output. The frequency of the alias signal *falias* is determined by both the VCO frequency *fvco* and the sampling frequency *fs* , as shown in Fig. 3

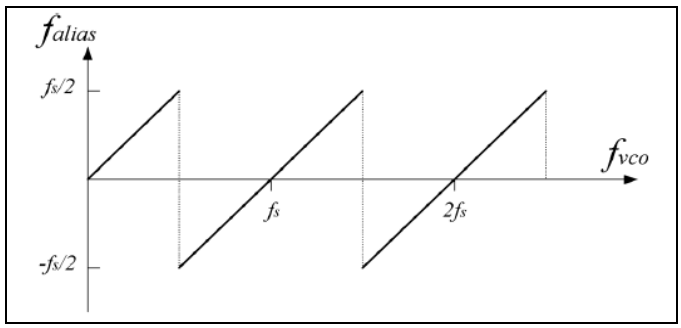

Figure 3: Frequency produced by the aliasing divider

3. Implementation

3.1. Phase frequency detector

The idea of PFD is to measure the phase difference between the reference and feedback signal. If there occurs difference in phase between these two signals then PFD generates UP or DOWN synchronized signals to the charge pump. If the PFD produces UP signal then charge pump pumps the charge onto the LPF capacitor which in turn increases the control voltage Vcntrl which is applied as input to the VCO and decreases control voltage when it produces DOWN signal.

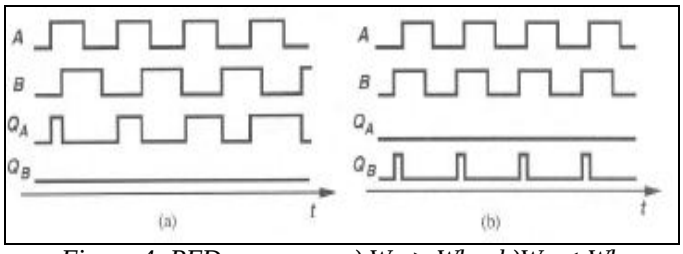

Figure 4: PFD responses a) Wa > Wb b)Wa < Wb

The operation of the PFD is as follows if Wa>Wb then PFD produces +ve pulses at Qa while Qb remains at zero. Conversely if Wa<Wb then +ve pulses appear at Qb while Qa at zero.

If Wa=Wb, then the ckt generates pulses at either Qa or Qb with width equal to the pulse difference between two inputs. Thus the average value of Qa & Qb is an indication of the frequency or phase difference between A & B. The outputs Qa & Qb are usually called up and Down signals.

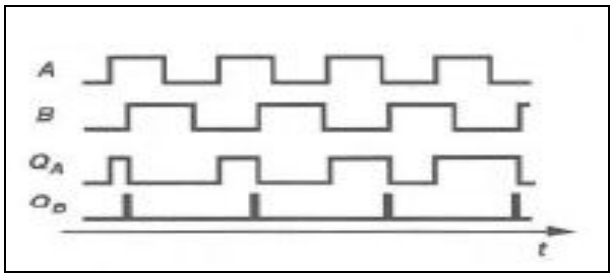

Figure 5: PFD output

Here if Qa=Qb=0, clock A causes Qa to go high , subsequent transition on A have no effect on Qa, and where B goes high ,the And gate activates reset of both flip flop, thus Qa & Qb are simultaneously high for a duration given by the total delay through the AND gate and the reset path of the filpflop**.**

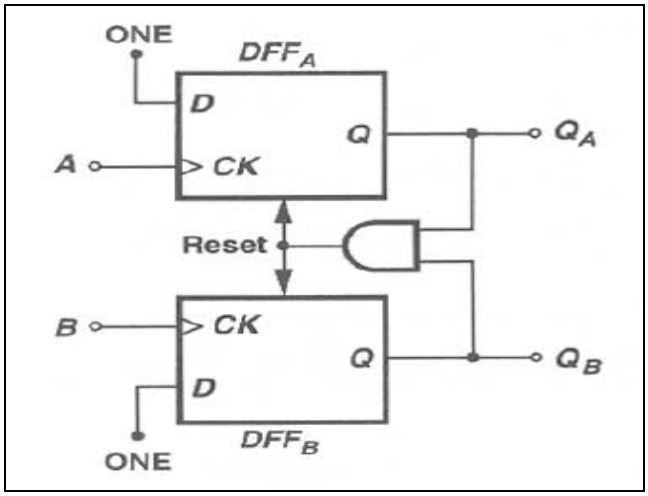

Figure 6: Block diagram of Phase/frequency Detector

The circuit consists of two edge triggered resettable D flip flops with their D inputs are connected to VDD, signals A&B as clock inputs.

3.2. Charge Pump and Loop Filter

The PFD has three states those states are controlled by a three position electronic switch which is known as charge pump. When the switch is in the up or down position charge pump delivers a pump voltage to the loop filter.

When both up and down of PFD are off, i.e., N position, the switch is open, thus the loop filter is isolated from the charge pump and PFD.

Conversion of phase difference produced by PFD to current is done by charge pump which in turn controls the charging and discharging operation of the capacitor in the loop filter there after VCO is tuned with the help of this control voltage.

To achieve the ALL to be in locked state it is important to choose the correct values for the loop filter otherwise it may either lead the loop to oscillate for long without reaching the locked state or after in lock state also it may happen, small variations in the input data may cause the loop to unlock

Totally, we have two poles at the origin i.e., one which is produced by PFD/CP/LPF combination and other one is produced by VCO here instability occurs because two poles at the origin ,so in order to stabilize the system, add resistor in series with the capacitor. The compensated PLL also suffers from a major shortcoming. Large surge may occur in the control voltage, due to the injection of current into the loop filter when the charge pump drives the series combination of the resistor and capacitor. To overcome this problem another capacitor is usually added in parallel with the RC network.

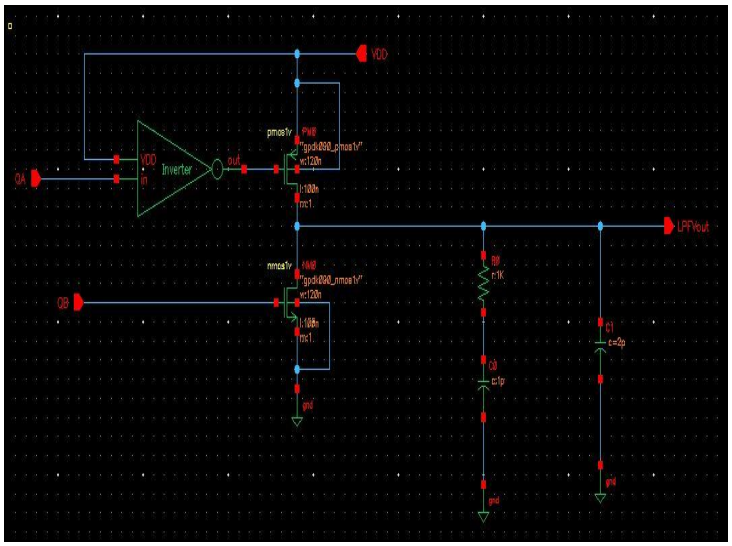

Figure 7: Charge Pump with Loop Filter

3.3. Voltage Controlled Oscillator

Here in phase locked loops, a voltage controlled oscillator is the main building block for both in analog and digital circuits. the applications of VCO is to increase the oscillation frequency range and also the quality of communication link in wireless communication systems which is done by the use of characteristic VCO, so VCO's have greater frequency range in today's wireless communication system.

Usually, in CMOS technology VCO is being used for low frequency applications but with the improved submicron process the CMOS oscillators have achieved greater frequency range (i.e., in the range of GHz). This range is made possible with the use of instinctive swing control. VCO can be built using many different techniques here in this paper, I have used current starved VCO.

3.4. Current starved VCO

A ring oscillator is composed of no of inverter or delay stages, the output of first stage is connected to the input of preceding delay stage and the output of last stage is connected to the input of first stage. the requirements to get oscillations for the oscillator are the first ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. This current starved VCO is same as that of ring oscillator in its operation.

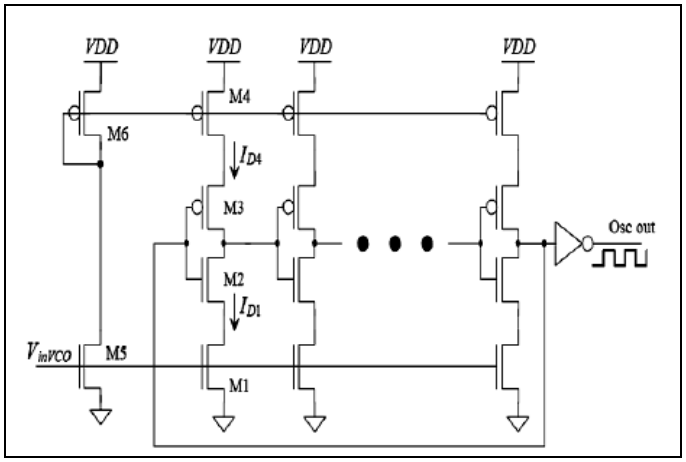

Figure 8: voltage controlled oscillator

Figure shows a current starved VCO, here from figure the transistors M2 & M3operates as inverter and Transistors M1 & M4 operates as current sources and these MOSFET's M1 & M4 limits the currents available to the inverter which is stated as inverter is starved for the current. The current in M5 &M6 are mirrored in each inverter/current source stage. In the upper PMOS MOSFET's the gates are shorted to drain. Input to the VCO is applied at the gate of M5.

3.5. Frequency Sampler

The main idea or theme of a high speed sampler depends on sense amplifying f/f (SAFF), In SRAM implementation a sense amplifier is commonly used because it can probe a subtle voltage difference.

By making use of sense amplifier in addition with CMOS differential logic structure, can significantly minimize delay between the input and reference, size and power consumption.

SAFF can be used in digital as well as analog implementations for example, digital sampler and divider respectively, in both the cases it functions accordingly.

Generally, during the pre-charge period only the SAFF will function properly at highest frequency, so we need to find out pre-charge phase. Pre-charge phase of SAFF is figured out by sample frequency when it is applied as a digital sampler and in case of divider pre-charge phase of SAFF is figured out by VCO, because it should match every edge of the VCO output.

In comparison with the TFF which is designed under same conditions in 90nm process it gives a frequency of 5GHz while using this SAFF structure we can make it to reach more than 70GHz operating frequency in the intended ALL architecture design.

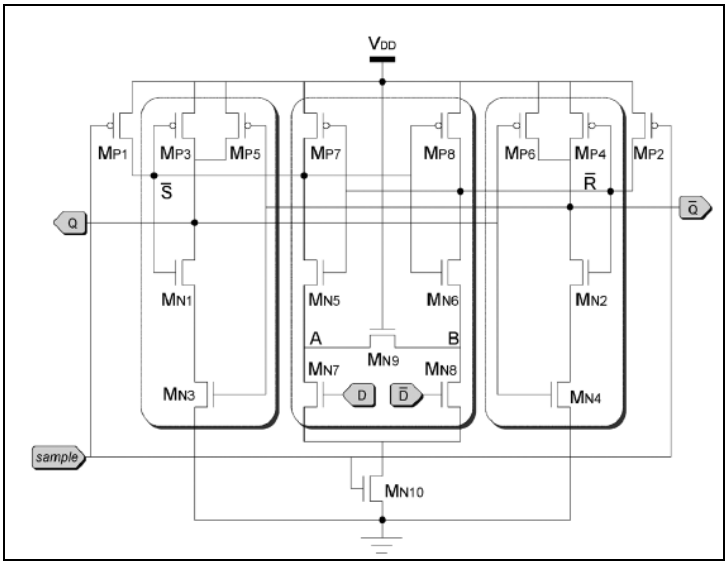

Figure 9: Sense-amplifying flip-flop based sampling circuit. The first stage (in the center) senses a differential input, while the second stage (on either side) provides a full-swing output signal.

Figure shown above consists of two cascaded latches first one is sense amplifying master latch consists of NMOS transistors Mn5 toMn9 and PMOS transistors Mp7,Mp8 with dynamic logic and this dynamic logic has two phases pre-charge phase and evaluation phase. Pre-charge phase when clock is low and here Mp1,Mp2 turn on and Mn10 turn off. Because of Mn9 always turns on during

pre-charge phase the nodes Sbar, Rbar, A & B are all charged to high. And in the evaluation phase reverse will happen Mn10 turns on and Mp1,Mp2 turns off.
The differential input voltage of D and Dbar confirms that A & B have different voltages before they are completely discharged. During this small discharge time delay on Mn9 the state of the i/p is latched.
In every clock cycle, regardless of whichever state of input data the cross transistor Mn9 forces or troops the whole differential tree pre-charge and discharge in a rapid manner. Therefore delay of which will affect the speed of latching. With any sampler differential input offset error less than the VCO signal in, the falias signal will continue to be produced, despite its being with an asymmetric duty cycle. The asymmetric duty cycle occurs as a constant phase offset at the active edge of sampler at its output compared to an ideal sampler, which would not affect the loop behavior.
The output of the sense amplifier should produce stable latched differential data, i.e., before applying it to the divider / PFD. so we need to check or condition the Q & Qbar signals with a NAND RS latch because these nodes may stay high during pre-charge phase.
Here fs I lower than the VCO outputs (i.e., D &Dbar) which are applied as i/p to the sampler. The VCO output frequency which is divided by the i/p sample frequency is reflected into the o/p of the sampler because sampling occurs at the rising edges of the sample clock.

3.6. Tspc (True single phase clocking) Clock Divider
For clock generation, mostly reference frequencies are limited by the maximum frequency decided by a crystal frequency reference, (mostly in the range of 10 MHz), the divider‘s purpose is to scale down the frequency from the output of the voltage controlled oscillator so that the system can operate at a higher frequency than the reference signal Thus the VCO has to be designed such that the output of VCO is = N times the reference frequency. So the output of the VCO is passed through a divide by N-counter and feedback to the input.

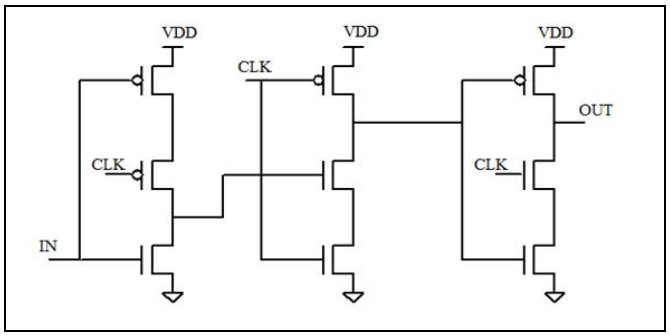

Figure 10: TSPC divider

This topology achieves relatively high speeds with low power dissipation, but requires rail-to-rail clock swings for proper operation.
The circuit consumes no static power and as a dynamic logic topology, the divider fails at very low clock frequencies due to the leakage of the transistors..

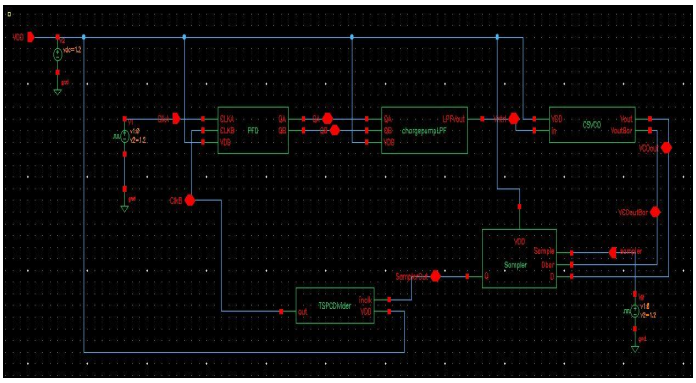
Figure 11: Proposed ALL Architecture

4. Simulation and Discussion
Here in this section simulation results are reported to show the proposed ALL design is able to synthesize the desired frequencies.
An example is given to illustrate how the architecture works.
Power calculations
At 1GHz reference input frequency with a voltage of 1.8v ALL consumes 0.371mw and at a voltage of 1.2v it consumes 0.107mw.
At 1.2v lock range for ALL is 200MHz to 8.5GHz and at 1.8v lock range is from 200MHz to 12.5GHz.

Delay times for reference clock and falias
Reference clock – 494.11ps
Falias clock – 12.04ns\

Control vtg	Trace Timings	VCO frequency
1.704	0.251ns	3.984GHz
1.608v	0.252ns	3.968GHz
1.408v	0.256ns	3.906GHz
1.204v	0.258ns	3.875GHz
1v	0.276ns	3.623GHz
0.8v	0.327ns	3.058GHz
0.6v	0.46ns	2.173GHz
0.413v	0.91ns	1.098GHz
0.35v	1.053n	946MHz

Table 1: VCO output frequency range

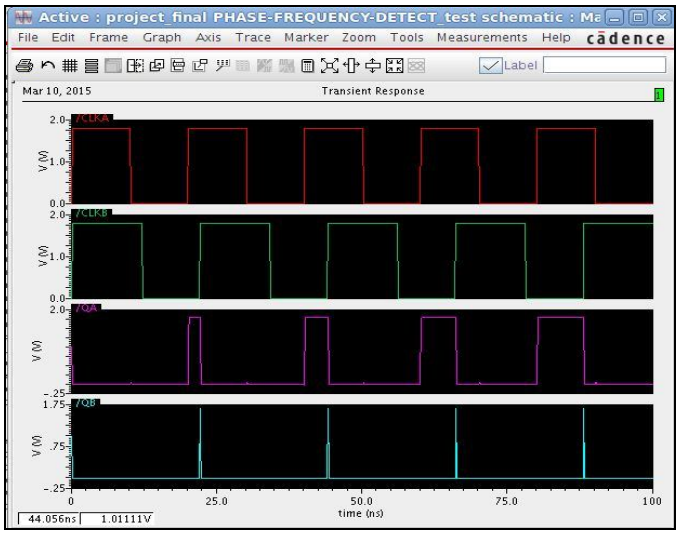

Figure 12: simulation result of PFD

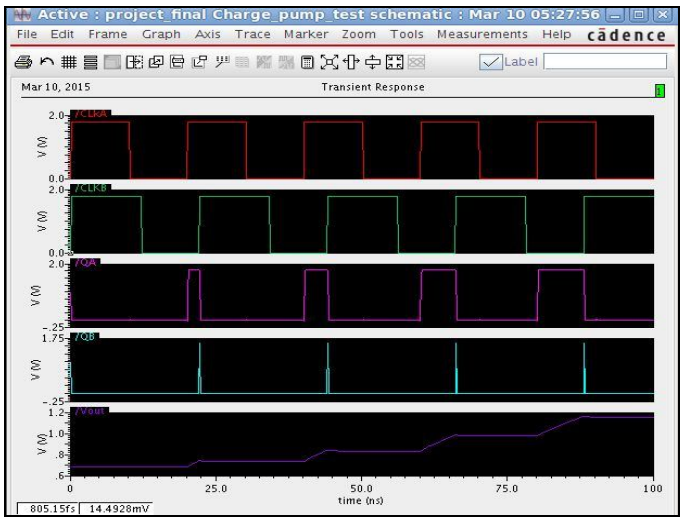

Figure 13: simulatin result of PFD with Charge Pump

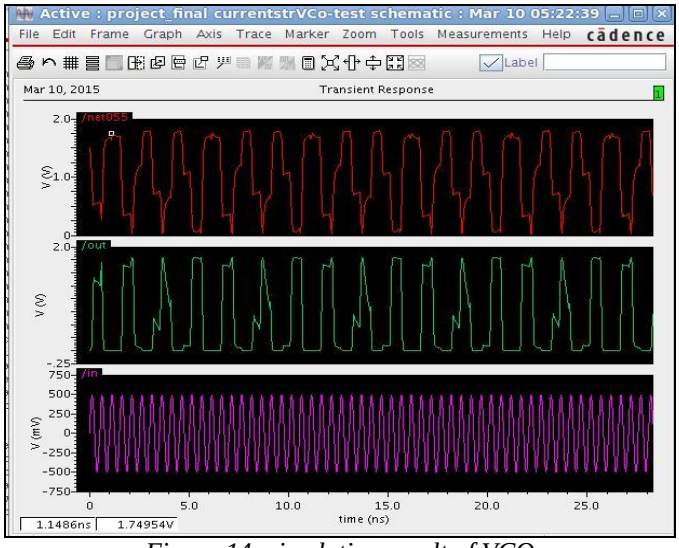

Figure 14: simulation result of VCO

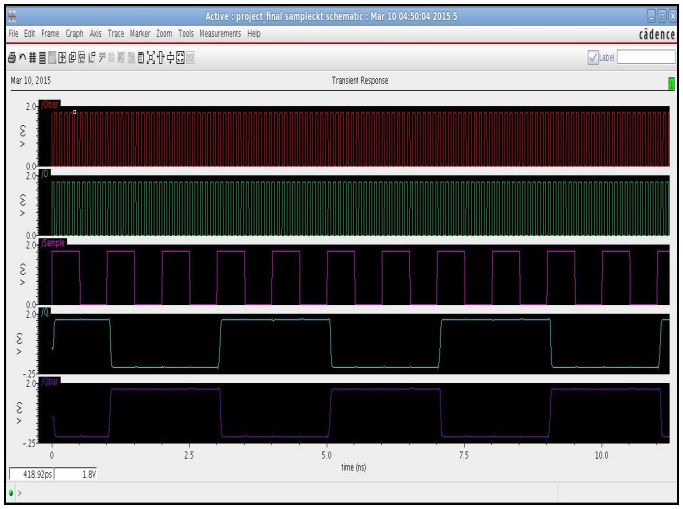

Figure 15: simulation result of Sampler

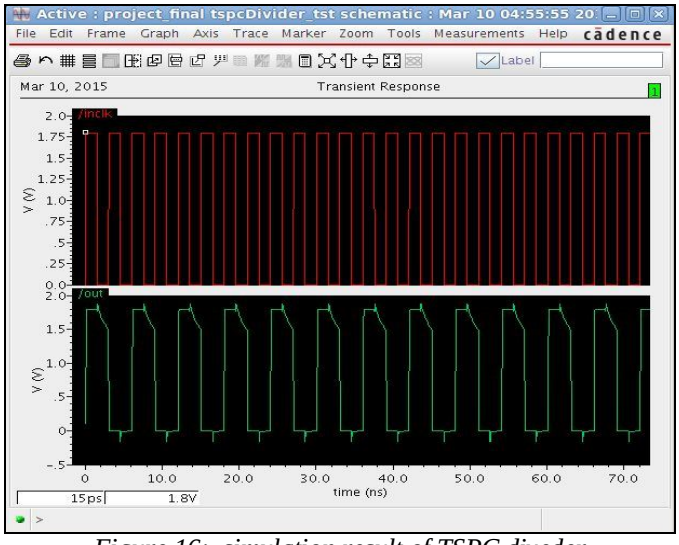

Figure 16: simulation result of TSPC diveder

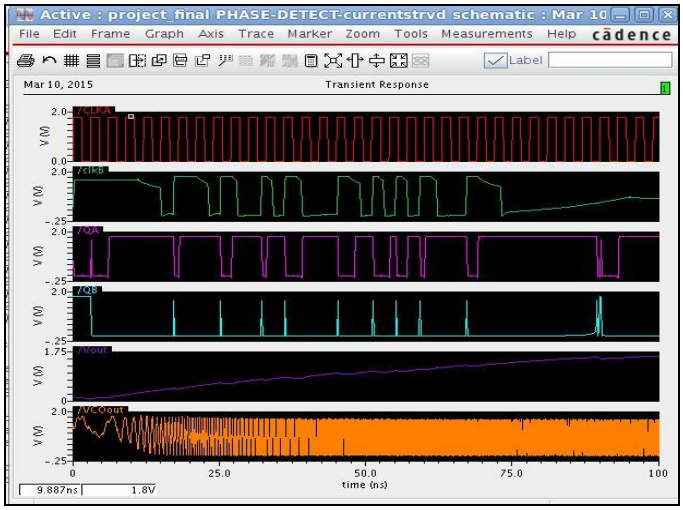

Figure 17: simulation result of proposed ALL

5. Conclusion

Here I have designed and simulated a high frequency alias-locked loop with a novel oscillator in a 90 nm CMOS process.

It is capable of oscillating much faster than an inverter-based ring oscillator. The proposed Alias locked loop architecture locks in the range of frequency 200MHz to 12.5GHz.

The high speed digital sampler in the feedback path provides wide range control of frequency without the need of a flip-flop or counter clocked by. This will be particularly important for millimeter wave communications and radar circuits.

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