INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN 2278 – 0211 (Online)

An Improved DSTATCOM Topology with Reduced VSI Rating, DC Link Voltage and Filter Size

K. Haritha
P.G. Scholar, EEE, KEC Kuppam, JNTUA, India
S. Kumar
M. Tech. Associate Professor, KEC Kuppam, JNTUA, India
Dr. Venugopal N.
Ph. D. Professor, HOD EEE, KEC kuppam, JNTUA, India
Ch. Jayavardhana Rao
M. Tech. Associate Professor, EEE, KEC Kuppam, JNTUA, India
P. Raju
M. Tech. Associate Professor, EEE, KEC Kuppam, JNTUA, India

Abstract:
This paper proposes an improved hybrid distribution static compensator (DSTATCOM) topology to compensate reactive and non linear loads with reduced VSI rating, DC link voltage and filter size. An LCL filter with small value of inductor compared to traditional L filter has been used at the front end of a voltage source inverter (VSI), which provides the elimination of switching harmonics. Voltage of the DSTATCOM can be reduced with capacitor to be connected in series with an LCL filter. Consequently the power rating of the voltage source inverter has been decreased. With reduced dc-link voltage, the voltage across the shunt capacitor of the LCL filter will be also less. It will reduce the power losses in the damping resistor as compared with the traditional LCL filter with passive damping. Therefore, the proposed DSTATCOM topology will have reduced weight, cost, rating, and size with improved efficiency and current compensation capability compared with the traditional topology. A systematic procedure to design the components of the passive filter has been presented. The effectiveness of the proposed DSTATCOM topology over traditional topologies is validated through simulation.

Keywords: *Distribution static compensator (DSTATCOM), Hybrid topology, passive filter, power quality (PQ)*

1. Introduction

An electric power distribution system is the final stage in delivery of electrical power; it carries electricity from transmission system to individual consumers. Except in a very few special situations, electrical energy has been generated, transmitted, distributed, and utilized as alternating current (AC). However, alternating current has several distinct disadvantages. One of these is the necessity of supplying reactive power with active power. Due to stored energy in the load and again send back to source, or presence of non-linear loads that distorts the wave shape of the current drawn from the source, due to this the apparent power will be greater than the real powers, which will effects the power factor. Due to this high currents energy lost in distribution system will increase, further equipment cost will increase. This incremental costs of equipment and wastage of energy causes electrical utilities to charge a higher cost to industries or commercial customers where there is a low power factor. In traditional method, L-type filters with large value of inductance were used to increase the quality of current to be injected. This large value of inductor has low slew rate for tracking the reference currents, and produces large voltage drop across it, intern it requires high value of dc-link voltage for the compensation. Therefore L-filters increases cost, size, and power rating. AN LCL filter is used at the front end of the VSI which will improve the tracking performance, but requires high value of dc-link voltage as that of L filter. In this paper an LCL filter is used to overcome the aforementioned draw backs. Capacitor is used in series with the LCL filter to decrease the voltage of DSTATCOM. This proposed model decreases the size of the passive components, rating of dc-link voltage, rating of VSI. It provides good tracking performance.

2. Principle of DSTATCOM

DSTATCOM is power electronics based power quality improving device, which generates and /or absorbs the reactive power whose output can be varied so as to maintain control of specific parameters of the electric power system. The DSTATCOM comprises of

coupling transformer with internal leakage reactance, a three phase voltage source inverter (VSI) with self commutating switches (GTO/IGBT), and a DC-link capacitor. Fig.1 shows the basic configuration of DSTATCOM.

The VSI converts the dc voltage across the storage device into ac output voltages. These ac voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Inverter is the main component of the DSTATCOM. The objective of a VSI is to produce a sinusoidal AC voltage with minimal harmonic distortion from a DC voltage. The operation of the DSTATCOM is as follows: The voltage is compared with the AC bus voltage system (Vs). When the magnitude of AC bus voltage is above that of the VSI magnitude (Vc), the AC system considered that, DSTATCOM as inductance connected to its terminals. Otherwise if the voltage magnitude of VSI is above that of the AC bus voltage magnitude, the AC system sees the D-STATCOM as capacitance connected to its terminals. If the VSI voltage magnitude is equal to AC bus voltage magnitude, then the reactive power exchange is zero. Suppose DSTATCOM has a DC active element or energy storage elements or devices on its DC side, it can able to deliver real power to the power system. This can be done by varying the phase angle of the DSTATCOM terminals and the phase shift of the AC power system. When VSI phase angle lags phase angle of the AC power system, the DSTATCOM absorbs the real power from the AC system, if the phase angle of VSI leads phase angle of AC power system, the DSTATCOM supplies real power to AC supply mains. The main feature is governing of bus voltage magnitude by dynamically absorbing or generating reactive power.

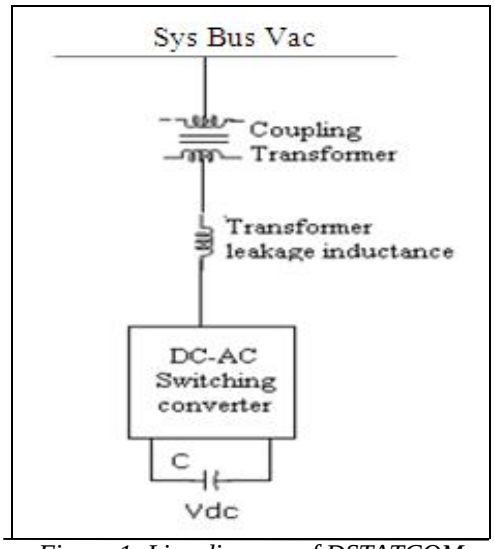

Figure 1: Line diagram of DSTATCOM

3. Proposed DSTATCOM with LCL-Filter and Series Capacitance

The proposed DSTATCOM three-phase equivalent circuit diagram is shown below in fig.2.It is realized by using three-phase four-wire two-level neutral-point-clamped VSI. An LCL filter is connected at the front end of voltage source inverter with series capacitance C_{se} .

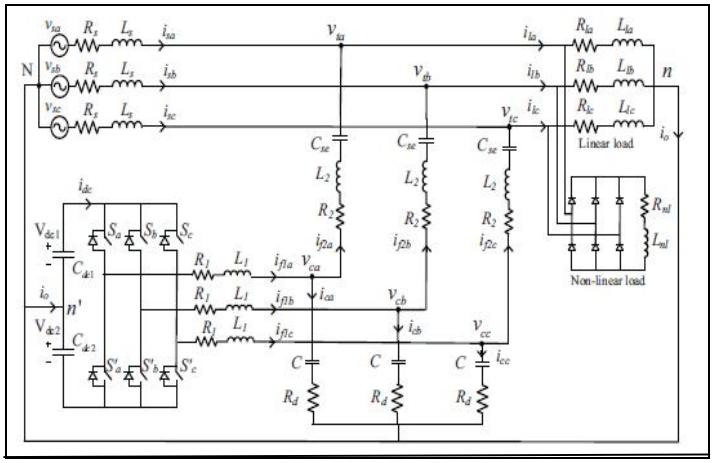

Figure 2: equivalent circuit of DSTSTATCOM

This LCL filter reduces the size of the passive components required and capacitance will reduce the DC-link voltage and hence power rating of voltage source inverter.

Here L_1 and R_1 represent resistance and inductance at VSI side; L_2 and R_2 represents inductance and resistance at load end side of the system. C is filter capacitance which forms LCL filter in all three phases. Rd is damping resistance used in series with the capacitance C, provides passive damping of the overall system and damp out the resonance. Here i_{f1a} and i_{f2a} are filter currents in phase-a and similar in all three phases. v_{sha} is voltage across LCL filter and i_{sha} is current through LCL filter, this is similar for other two phases. The voltage across the DC_link capacitors are maintained constant i.e. $V_{dc1}=V_{dc2}=V_{dcref}$. The source and load of DSTATCOM are connected to a common point called point of common coupling (PCC).

4. Control of DSTATCOM

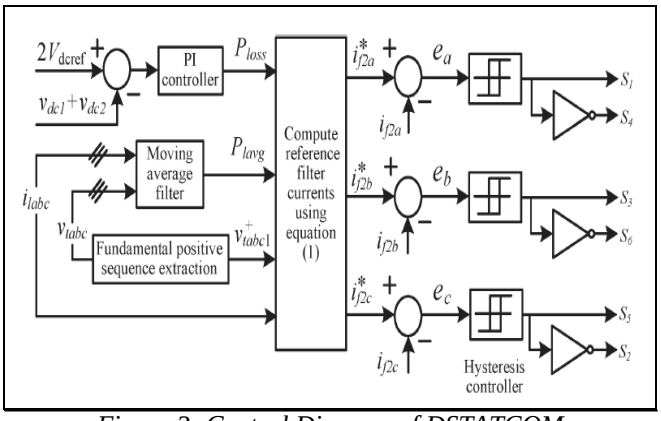

Figure 3: Control Diagram of DSTATCOM

The DSTATCOM is controlled, such that all source currents are balanced, sinusoidal, and in phase with the terminal voltages. In voltage source inverter losses and load power are supplied by the source. Control diagram is as shown in fig.3. Here source is considered to be no stiff, therefore the voltages to calculate reference filter currents will not provide satisfactory operation with the direct use of terminal current. And hence the fundamental positive sequence component of three-phase voltages are used to generate reference filter currents $(i^{*}_{f2a}, i^{*}_{f2b}, i^{*}_{f2c})$ based on symmetrical component theory. These currents are written as below. In (1) v^{+}_{ta1}, v^{+}_{tb1} and v^{+}_{tc1} are fundamental positive sequence voltages at the load terminal. Here P_{lavg} and P_{loss} represent the average load power and the total losses in the VSI, and $\Delta^{+}_{1} = (v^{+}_{ta1})^2 + (v^{+}_{tb1})^2 + (v^{+}_{tc1})^2$ respectively.

$$i^{*}_{f2a} = i_{1a} - i^{*}_{sa} = i_{1a} - \frac{v^{+}_{ta1}}{\Delta^{+}_{1}}(P_{1avg} + P_{loss})$$

$$i^{*}_{f2b} = i_{1b} - i^{*}_{sb} = i_{1b} - \frac{v^{+}_{tb1}}{\Delta^{+}_{1}}(P_{1avg} + P_{loss})$$

$$i^{*}_{f2c} = i_{1c} - i^{*}_{sc} = i_{1c} - \frac{v^{+}_{tc1}}{\Delta^{+}_{1}}(P_{1avg} + P_{loss}) \quad (1)$$

At any arbitrary time $t1$, average power can be computed as

$$P_{lavg} = \frac{1}{T}\int_{t_1-T}^{t_1}(v_{ta}i_{ta} + v_{tb}i_{tb} + v_{tc}i_{tc})dt \quad (2)$$

The total losses in VSI can be computed by using proportional-integral controller at the positive zero crossing of phase-a voltage.

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc}\, dt \quad (3)$$

Here K_p, K_i are proportional, integral gains and e_{vdc} represents voltage error of the PI controller and it is written as $e_{vdc} = 2V_{dcref} - (V_{dc1} + V_{dc2})$. The current error e_{abc} can be obtained by subtracting the actual filter current from the reference filter current.

5. Simulation Verification

This proposed topology uses lower rating VSI and smaller value of filter inductor, reduces the damping power loss and provides good current compensation. This effectiveness of DSTATCOM can be verified by simulation. The simulation diagram is shown below in fig (4). In Fig (5) (a) and (b) shows, the three-phase source current waveforms and PCC voltages are shown before compensation same as load currents, these currents are unbalanced and distorted due to the presence of unbalanced linear and nonlinear loads.

The traditional method simulation results were presented in Fig (6).The three phase source currents are shown in fig 6(a) which are balanced and sinusoidal. Fig 6(b) shows the PCC voltages. From both the wave forms it contains switching frequencies. Fig 6(c) shows the three phase filter currents. Voltage across upper capacitor, lower capacitor and total DC link voltages are shown in Fig 6(d). The Voltage across upper capacitor and lower capacitor maintained at 520V and total DC link voltage is at 1040V with PI controller.

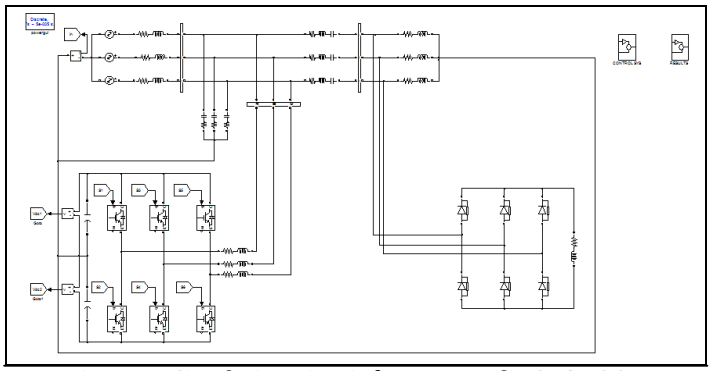

Figure 4: Simulation circuit for proposed DSTATCOM

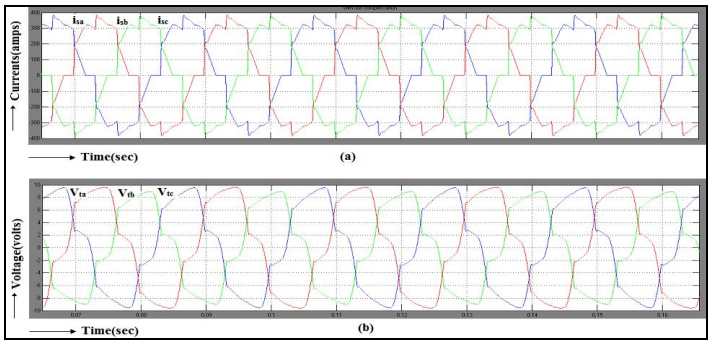

Figure 5: Simulation result without compensation (a) Source Current and (b) PCC voltage

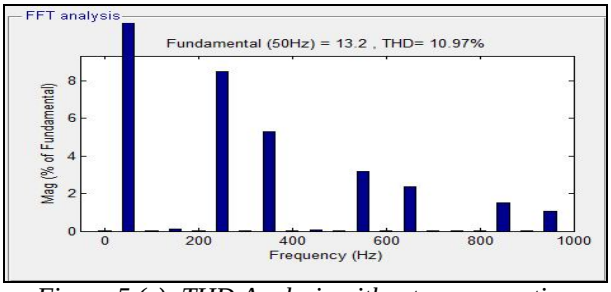

Figure 5 (c): THD Analysis without compensation

Fig 5 (c) shows that total harmonic distortion without compensation the percentage of total harmonic distortion is 10.97%.

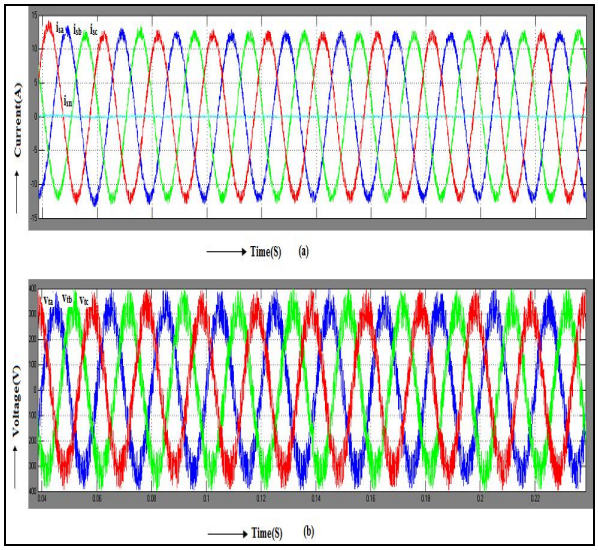

Figure 6: Simulation Result for traditional tropology (a) Source currents (b) PCC Voltages

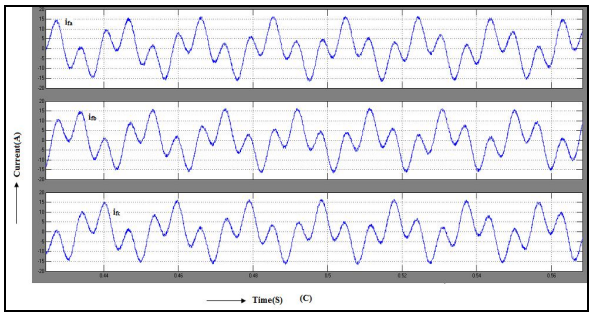

Figure 6 (c): Filter Currents

The filter currents, as shown in Fig. 6(c), have smaller ripples as compared with that of the traditional topology. The voltages across each capacitor and the total dc-link voltage are shown in Fig. 6(d), having maintained at 110 and 220 V, respectively.

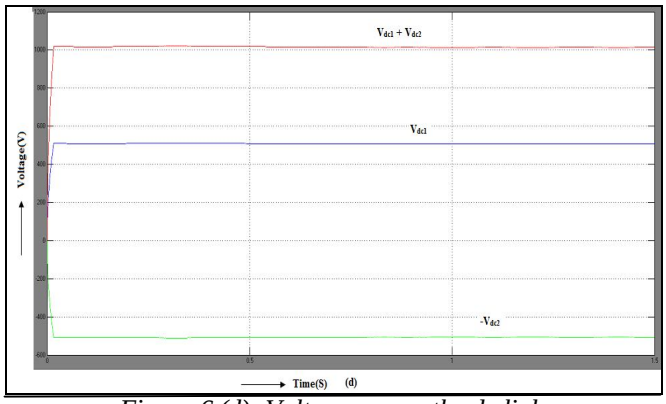

Figure 6 (d): Voltage across the dc link.

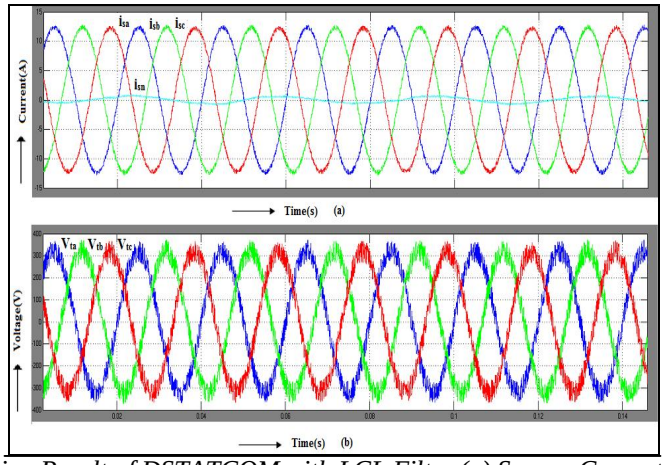

Figure 7: Simulation Result of DSTATCOM with LCL Filter (a) Source Current (b) PCC Voltages

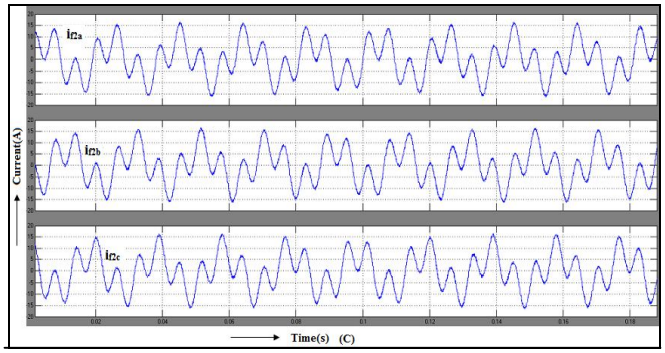

Figure 7 (c): Filter Currents

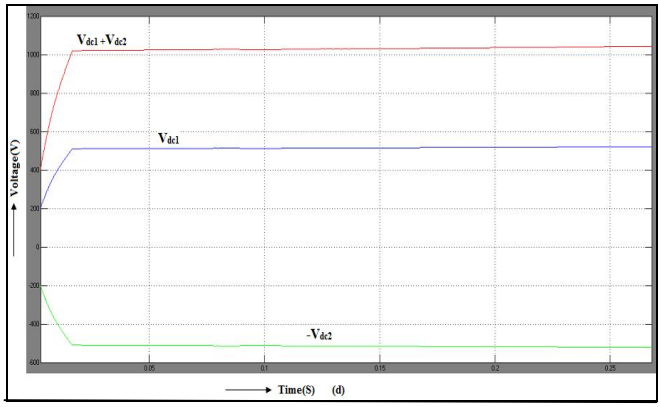

Figure 7 (d): Voltage across dc link

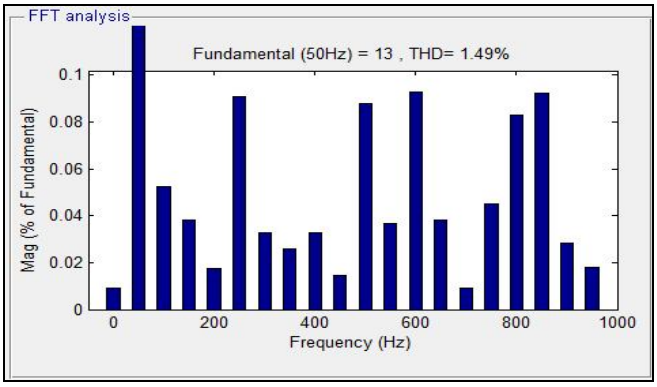

Figure 7 (e): THD analysis with LCL filter

The simulation results with LCL filter is presented in Fig (7). Here source currents, PCC voltages are sinusoidal and balanced, contains switching harmonics. Fig(e) shows the THD result of DSTATCOM with LCL filter and with LCL filter THD is 1.49%.

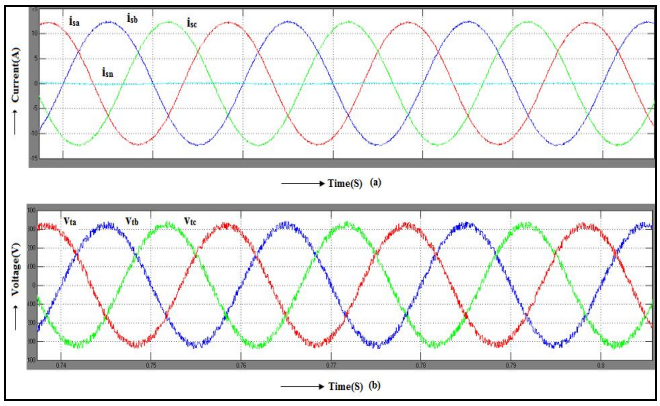

Figure 8: Simulation Result of proposed DSTATCOM (a) Source Current (b) PCC Voltages

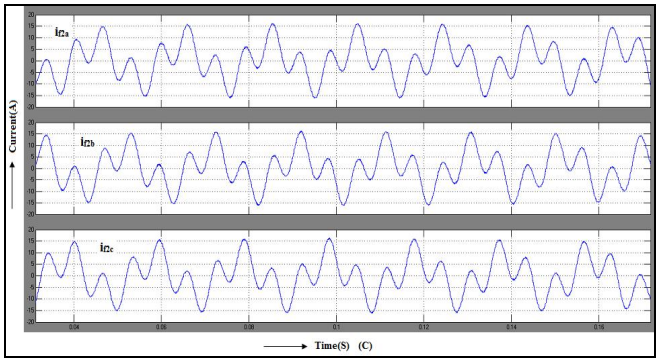

Figure 8 (c): Filter Currents

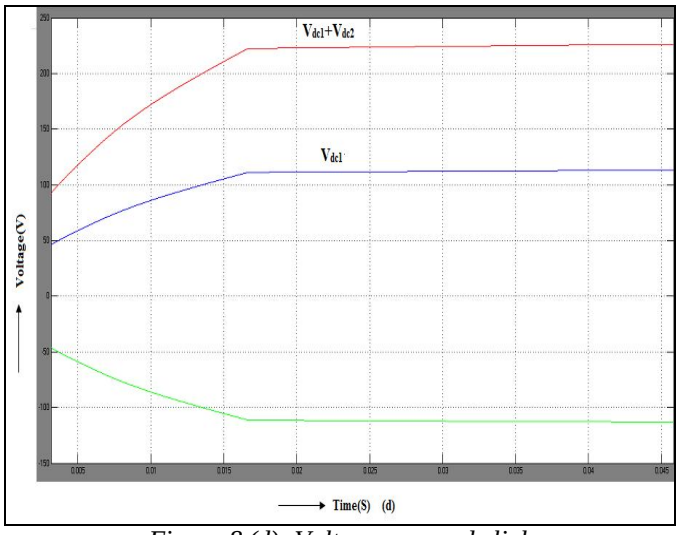

Figure 8 (d): Voltage across dc link

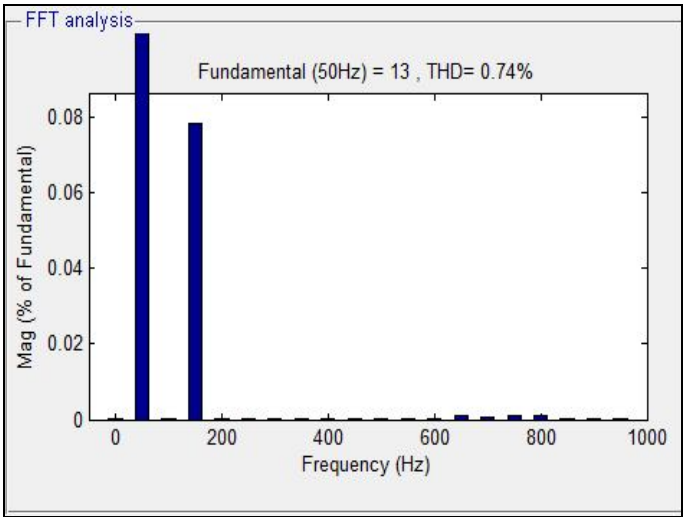

Figure 8 (e): THD analysis of proposed DSTATCOM

Simulation result of the proposed topology is shown in fig(8).Fig(8) (a) and (b) Presented three phase source currents and PCC voltages, which are balanced and sinusoidal and having neglecting switching losses.The filter currents, as shown in Fig 8(c), have smaller ripples as compared with that of the traditional topology. The voltages across each capacitor and the total dc-link voltage are shown in Fig 8(d), having maintained at 110 and 220 V, respectively.

The performance of the proposed topology is compared with that of traditional DSTATCOM topologies, simulation parameters and corresponding percentage THDs in voltages and currents are illustrated in Table I. It is clear from Table I that the percentage THDs in three-phase source currents and in PCC voltages are considerably lesser in the proposed topology. Moreover, these confirm that the reduced dc-link voltage is sufficient for the DSTATCOM to achieve its current compensation performance.

DSTATCOM TOPOLOGY	Inductor Value	Voltage at dc link	Energy stored in passive components
Traditional	26mH	1040V	811.2 J
With LCL	7.5mH	1040V	811.2 J
proposed	2.1mH	220V	36.3 J

Table 1

Simulation result for the proposed topology with RC load is presented in fig (9). With highly distorted load currents the source currents are sinusoidal with negligible harmonic losses as shown in fig 9(a). PCC voltages are shown in fig 9(b) are sinusoidal and balanced with less ripple content. The voltage across each capacitor is maintained at 110V, it is shown in fig 9(d). The total DC link voltage is 220V. The filter currents are presented in fig 9 (c).

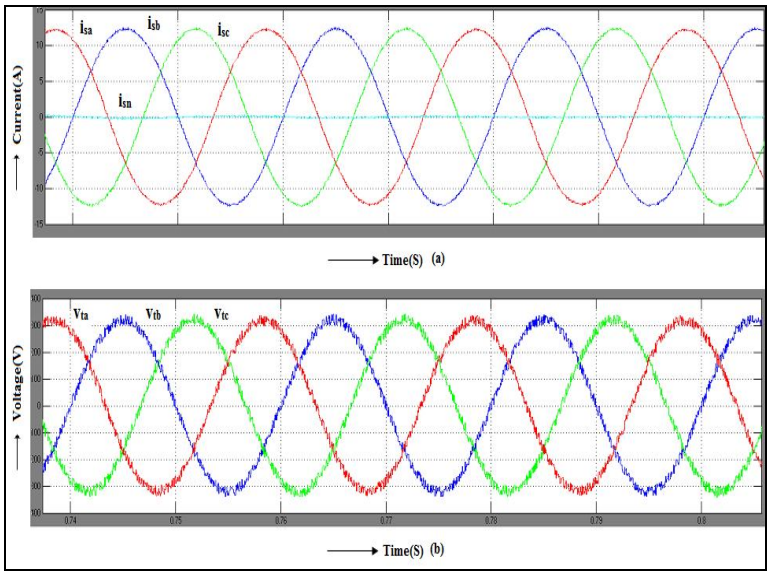

Figure 9: Simulation Result of DSTATCOM with RC nonlinear load (a) Source Current (b) PCC Voltages

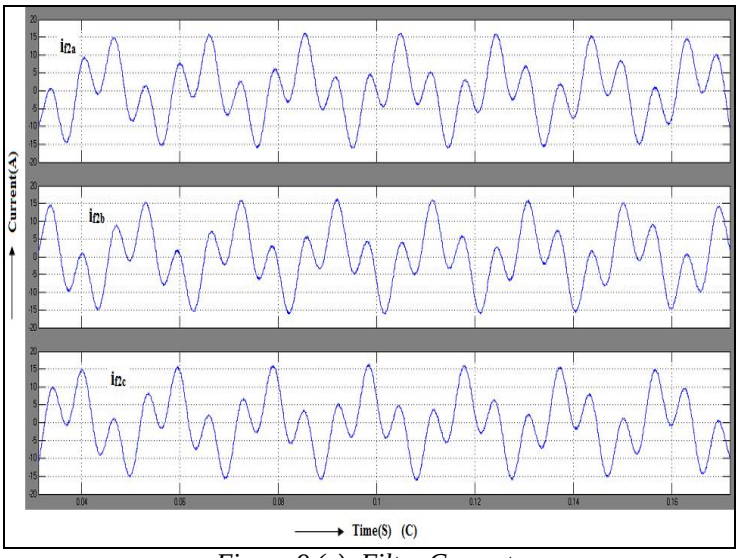

Figure 9 (c): Filter Currents

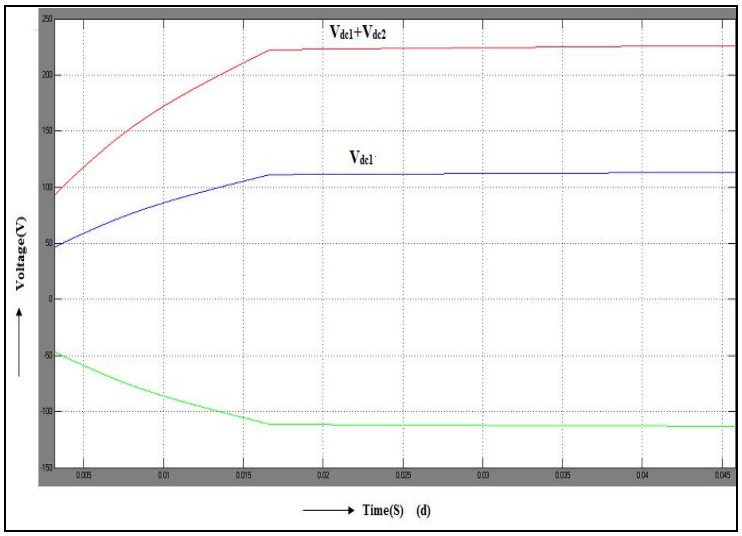

Figure 9 (d): Voltage across dc link

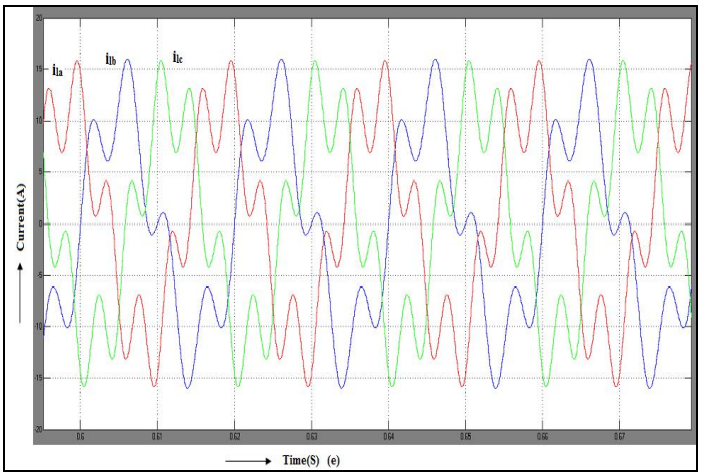

Figure 9 (e): Load Currents

Thus the reduced compensated voltage is sufficient to run the nonlinear RC load. And it is shown in fig 9(e).

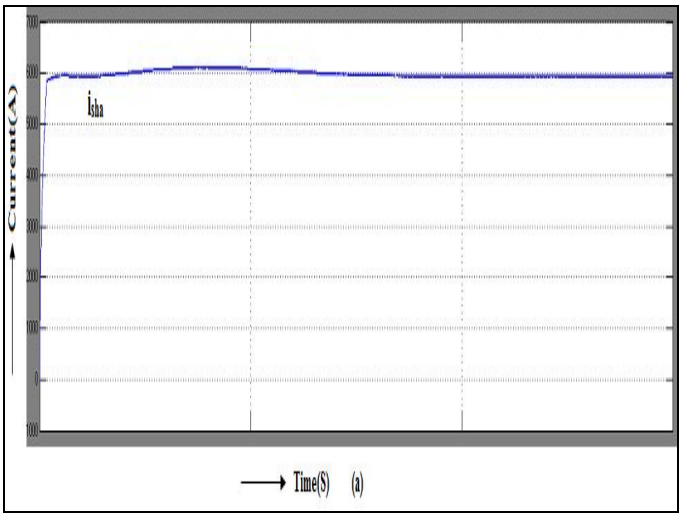

Figure 10: Damping RMS Currents (a) With LCL filter

The damping filter current in phase 'a' with LCL filter is shown in fig.5.7 (a). The current through the damping resistor is found to be 4.5A. And it is steady state rms value.

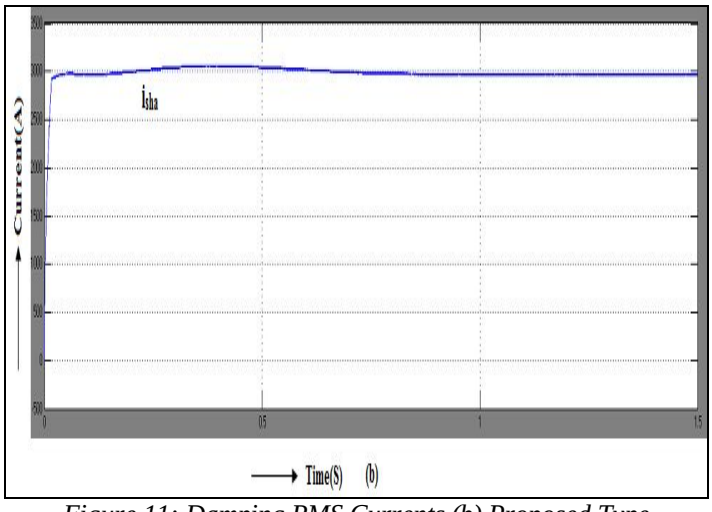

Figure 11: Damping RMS Currents (b) Proposed Type

Loss of power in damping resistor is given as

$$P_{loss1} = 3I_{sh}^2 R_d \quad (4)$$

$$3x\ (4.5)^2 x15 = 911.25W$$

The damping filter current in phase 'a' with proposed filter is shown in fig.5.7 (b). From the wave forms the reduced steady state value of damping current is 1.05A. Then the power loss can be given as

$$P_{loss2}=3x1.05^2x15=48.61W \quad (5)$$

The ratio of power loss with both LCL filter and proposed method is given as

$$\frac{P_{loss1}}{P_{loss2}} = \frac{48.61}{911.25} = 0.0533 \quad (6)$$

From this we can conclude that the power loss in proposed topology is 5.33% as compared with DSTATCOM with LCL filter.

6. Conclusion

The simulation results given that reduction of dc-link voltage, filter inductance, current through the shunt capacitor and damping power loss are reduced with DSTATCOM with LCL filter followed by series capacitance. This contribution shows reduction in cost, weight, size, and power rating of the traditional DSTATCOM topology. Effectiveness of the proposed topology has been validated through extensive computer simulation.

7. References

i. C. Schauder, "STATCOM for Compensation of Large Electric Arc Furnace Installations," Proceedings of the IEEE PES Summer Power Meeting, Edmoton, Alberta, July 1999, pp.1109-1112.

ii. G. Reed, J. Paserba, T. Croasdaile, M.Takeda, Y. Hamasaki, T. Aritsuka, N. Morishima, S.Jochi, I. Iyoda, M. Nambu, N. Toki, L.Thomas, G. Smith, D.LaForest, W. Allard, D.Haas, "The VELCOSTATCOM-BasedTransmission System Project," Proceedings of the 2001 IEEE PES Winter Power Meeting, Columbus,H, January/February 2001.

iii. C. Schauder, "STATCOM for Compensation of Large Electric Arc FurnaceInstallations," Proceedings of the IEEE PES Summer Power Meeting, Edmonon, Alberta, July 1999.pp.1109-1112.

iv. JianyeCuen, ShanSong, Zanjiwang, "Analysisand implement of Thyrister based STATCOM", 2006, International conference On Power System technology.

v. B. Singh and S. Arya, "Implementation of single-phase enhanced phase locked loop-based control algorithm for three-phase DSTATCOM," IEEE Trans. Power Del., vol. 28, no. 3, pp. 1516–1524, Jul. 2013.

vi. J. Liu, P. Zanchetta, M. Degano, and E. Lavopa, "Control design and implementation for high performance shunt active filters in aircraft power grids," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3604–3613, Sep. 2012.

vii. M. Singh, V. Khadkikar, A. Chandra, and R. Varma, "Grid interconnection of renewable energy sources at the distribution level with powerquality improvement features," IEEE Trans. Power Del., vol. 26, no. 1, pp. 307–315, Jan. 2011.

viii. A. Bhattacharya and C. Chakraborty, "A shunt active power filter with Enhanced performance using ANN-based predictive and adaptive controllers,"IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 421–428, Feb. 2011.

ix. R. Inzunza and H. Akagi, "A 6.6-kv transformerless shunt hybrid active filter for installation on a power distribution system," IEEE Trans. Power Electron., vol. 20, no. 4, pp. 893–900, Jul. 2005.

x. B. Singh and S. Sharma, "Design and implementation of four-leg voltagesource-converter-based VFC for autonomous wind energy conversion system," IEEE Trans. Ind. Electron., vol. 59, no. 12, pp. 4694–4703, Dec. 2012.