INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH & DEVELOPMENT

ISSN 2278 – 0211 (Online)

Design of a Power Divider with High Output Power Ratio

Jayati Singh
Student, Department of Electronics and Communication Student
J. K. Institute of Applied Physics and Technology, University of Allahabad, India
Shubham
Student, Department of Electronics and Communication Student
J. K. Institute of Applied Physics and Technology, University of Allahabad, India
Sreejith C. A.
Scientist 'C', LRDE - DRDO, Bangalore, India

Abstract:
The purpose of this research is to fabricate a two-way power divider in the power distribution ratio 1/15 and 14/15. The fabricated power divider has been designed using the T-junction model. The circuits have initially been designed and simulated on the two-dimensional software- Advanced Design System (ADS) followed by a three-dimensional simulation on the software- High Frequency Structural Simulator (HFSS). The results of the design have been analyzed in the form of s- parameter graphs verified for appropriate port losses, 2-D layouts for inspection of feasible fabrication and the corresponding 3-D model for accurate error- correction. The outcome of the above was then processed for fabrication.

Keywords: *2 way power divider, T-junction, s-parameter, port loss*

1. Introduction

Power dividers are passive microwave components used for power division or power combining, In power division, an input signal is divided into two (or more) output signals of lesser power, while a power combiner accepts two or more input signals and combines them at an output port. The divider may have three ports, four ports, or more, and may be (ideally) lossless. Three-port networks take the form of T-junctions and other power dividers, while four-port networks take the form of directional couplers and hybrids. Power dividers usually provide in-phase output signals with an equal power division ratio (3 dB), but unequal power division ratios are also possible.

The commonly used methods to design a power divider are:

1. T- Junction
2. 90 degree hybrid
3. Directional coupler

2. T-Junction Power Divider

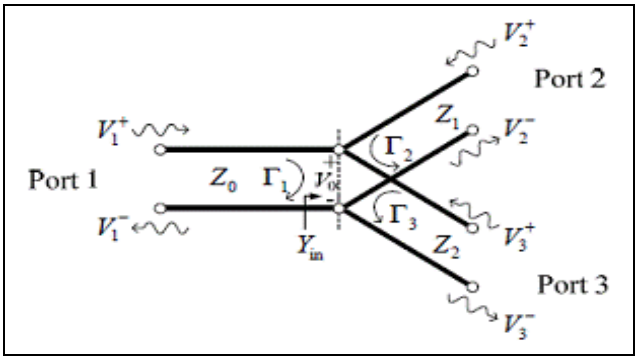

Figure 1

There are basic constraints we need to incorporate into the power divider.

1. The output ports must be matched in phase.
2. The input average power, P_{in}, should be divided between port 2 and 3 in desired ratio.
3. The equations for calculation of TL impedances are
   Z1 = Z0/ (P1/Pin) andZ2 = Z0/(P2/Pin)
4. The equations for calculating the powers at the output ports are

$$P1=\frac{1}{2}(|V0|2)/Z1 \quad \text{and } P2=\frac{1}{2}(|V0|2)/Z2$$

The above equations will be used to design the power divider.

3. Design of Unequal – Split Power Divider

3.1. Problem Statement

Design of a power divider with a power distribution of 1/15 and 14/15 in both the arms with a given input impedance of 50Ω at a frequency of 5.5 GHz.
Specifications:

SL NO.	PARAMETER	SPECIFICATION
1	Power ratio	1:14
2	Frequency	5 to 6 GHz ;Fc=5.5 GHz
3	Input return loss	<-15dB
4	Power at output port 1	-11.7±0.2 dB
5	Power at output port 2	-0.299 ±0.08dB
6	Phase imbalance between the output ports	±5° max
7	Output port impedance	50Ω

Table 1

3 designs have been considered in order for the design of the required power divider. Each one is an improvement over the previous with respect to the 2 essential factors taken into consideration here. They are *return loss, phase matching* and *uniform field distribution*.

3.2. Design 1:

- Calculations:

Given:
A micro-strip line of material RT duroid 5880 and 31 mil in height is used for the design.
Power ratio is 11.4dB.
From Figure 1,
Source/load Impedance (Z_{in}) = 50Ω.
In order to calculate impedances Z1 and Z2 we use the following formula

$$Z1 = (P_{in}/P1)*Z_{in} = 750\Omega$$
$$Z2 = (P_{in}/P2)*Z_{in} = 53.57\Omega$$

These two impedances are used to match TL 1 with the impedance of the output ports.
Using the LinCalc tool in ADS, the widths of the transmission lines were calculated according to the given impedances.
For Z1 = 750Ω, width is calculated as 2.18169 mm.
For Z2 = 53.57Ω, width is calculated as 0.0005 mm

3.3. 2-D Simulation of T-Junction:

The schematic diagram is drawn in ADS and the corresponding layout of the T-junction for the given power division ratio is:

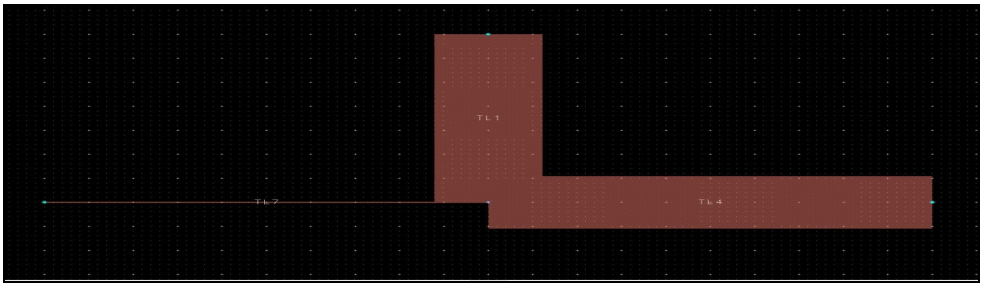

Figure 2

The above design of the T-junction power divider is not practically feasible because the minimum practical realizable width of transmission line is 0.2 mm whereas the above design presents a width of 0.0005 mm.

3.4. Design 2:

Using ADS (Modified T-junction diagram): In this modified version, sections of impedance matching quarter-wave transmission lines have been used at the output port in order to remove the limitations of the first model and generate a practically feasible layout. Their values have been calculated as follows. Refer to the schematic diagram for location of the transmission lines (TL).

- Calculations:

For output port 2,

Assume Z_{01}=118Ω (arbitrary) - TL 2

Then$Z'out = (Z_{01})^2/Z1$

Z'out = 18.56Ω - TL 4

Again Z'01 = (Z'out*Zout1)0.5

Z'01 = 30.05Ω - TL 7

For output port 3,

Z_{02} = (Z2*Zout2)0.5

Z_{02} = 53.57Ω - TL 3

Using the LinCalc tool, the widths of all the transmission lines were calculated as per their respective calculated impedances as follows.

TRANSMISSION LINE NO.	IMPEDANCE VALUE(OHM)	WIDTH (IN MM)
TL 1	50	2.422
TL 2	118	0.448
TL 3	53.57	2.39
TL 4	30.05	5

Table 2

As it can be observed from the table, the widths obtained from this design are practically feasible.

3.5. Schematic Diagram:

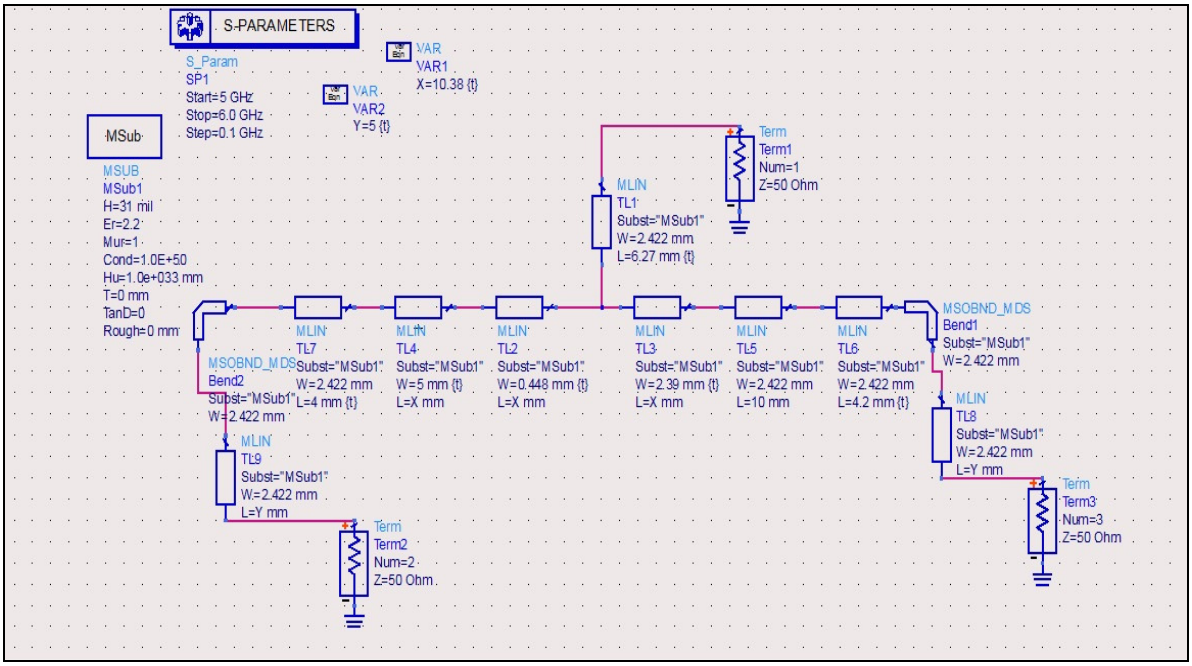

Figure 3

3.6. S –Parameter Graphical Results:

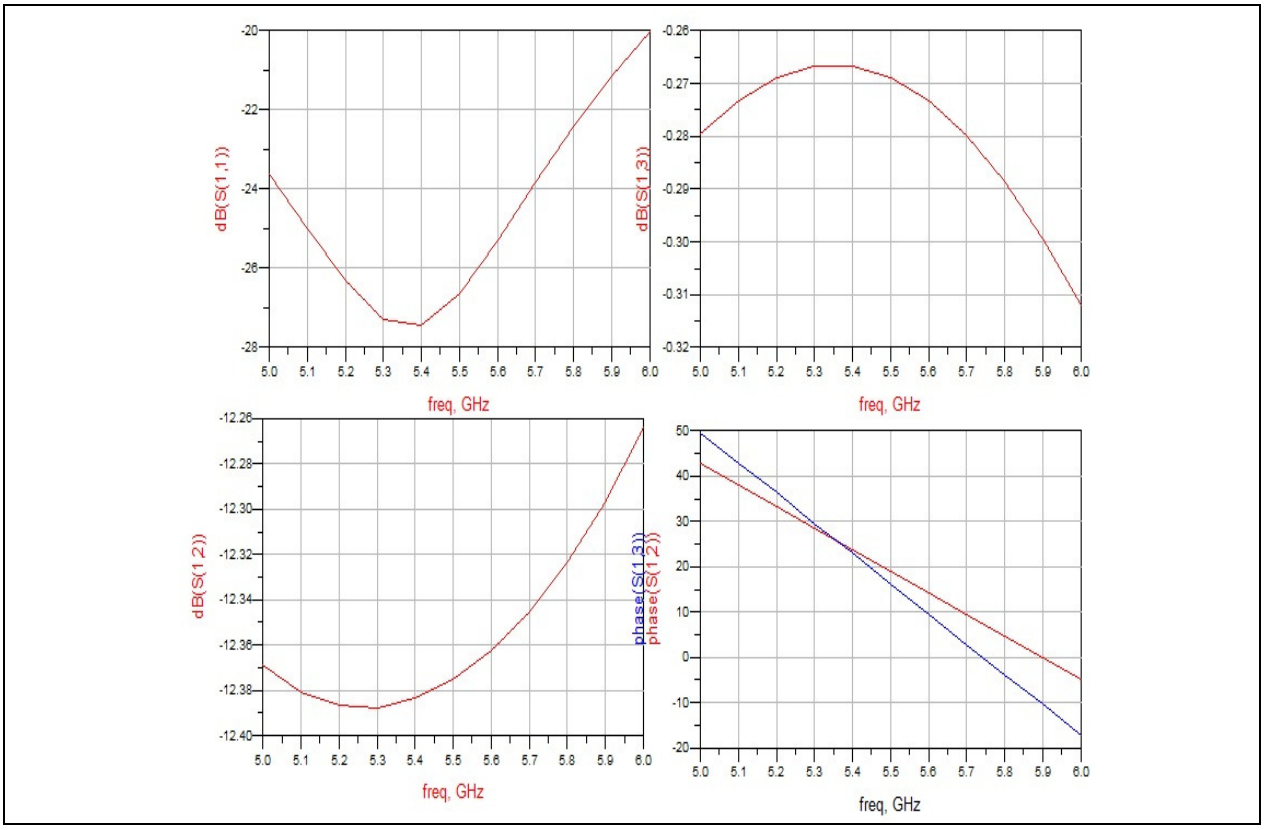

Figure 4

- It can be observed that the value of S(1,1) known as the return loss is less than -20dB at 5.5 GHz as per the required specifications.
- The output powers also meet the calculated power values and the phase at 5.5 GHz is matched.

3.7. 3-D Simulation Using HFSS:

This simulation represents the fabrication of a T junction on a micro-strip line.

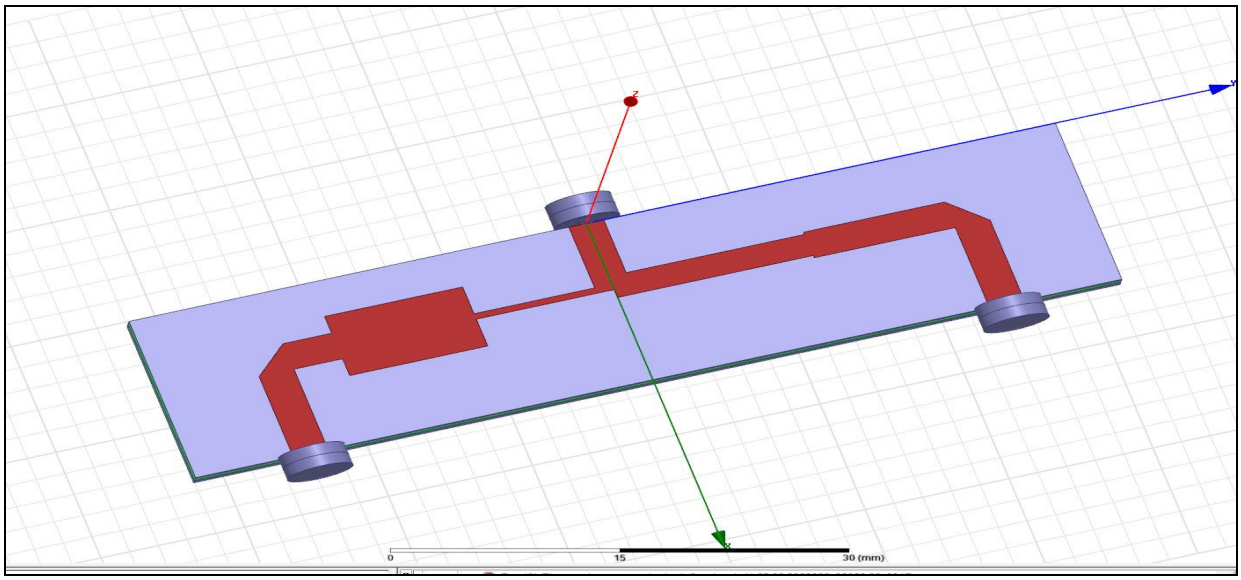

Figure 5

3.8. S(1,1) :

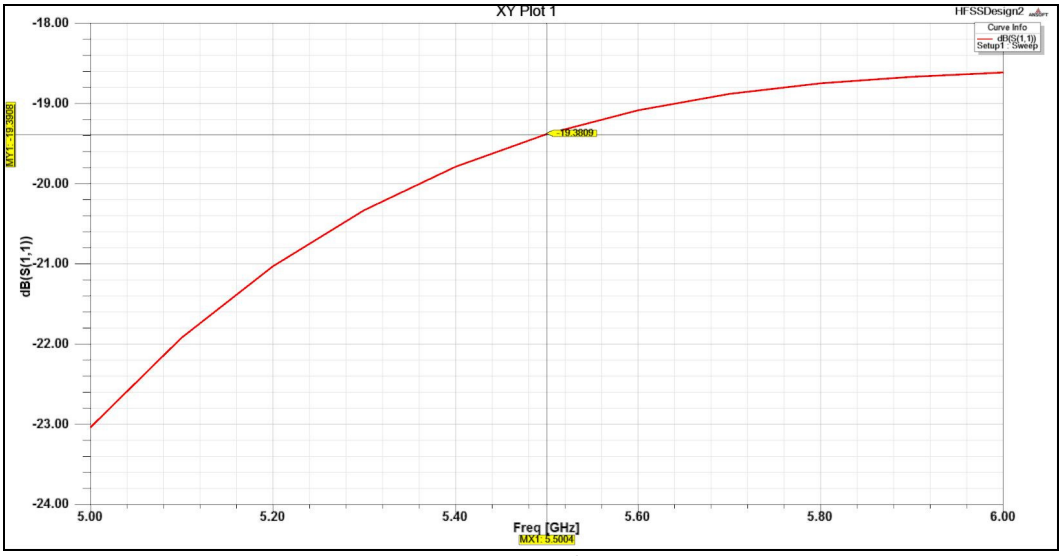

Figure 6

The value of return loss observed in the above graph is high. This is due to the junction effect between the transmission lines. In this effect due to the accumulation of charges at the junction of the transmission lines, a capacitance is created. In order to overcome this effect, a cut is introduced at the junction. This effect had not been captured in the 2-D simulation. Hence 3-D simulation is necessary for accurate results. The modified 3-D model and the corresponding results are given below:

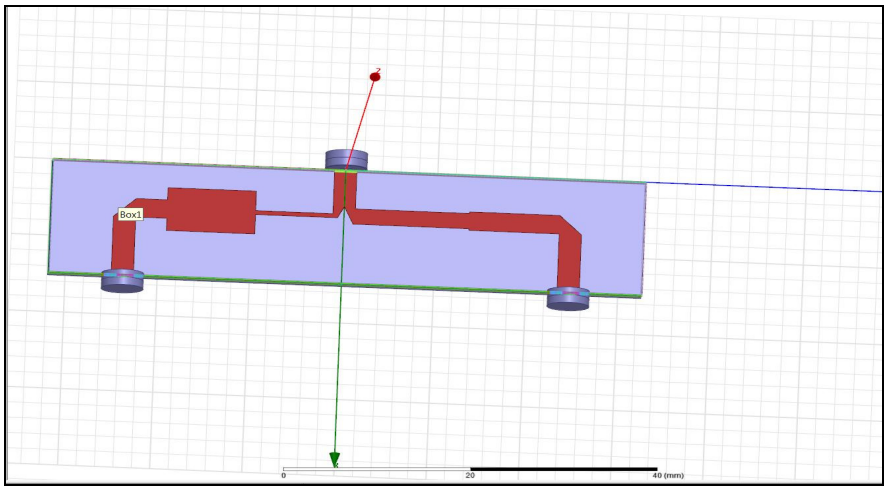

Figure 7

3.9. New S(1,1) :

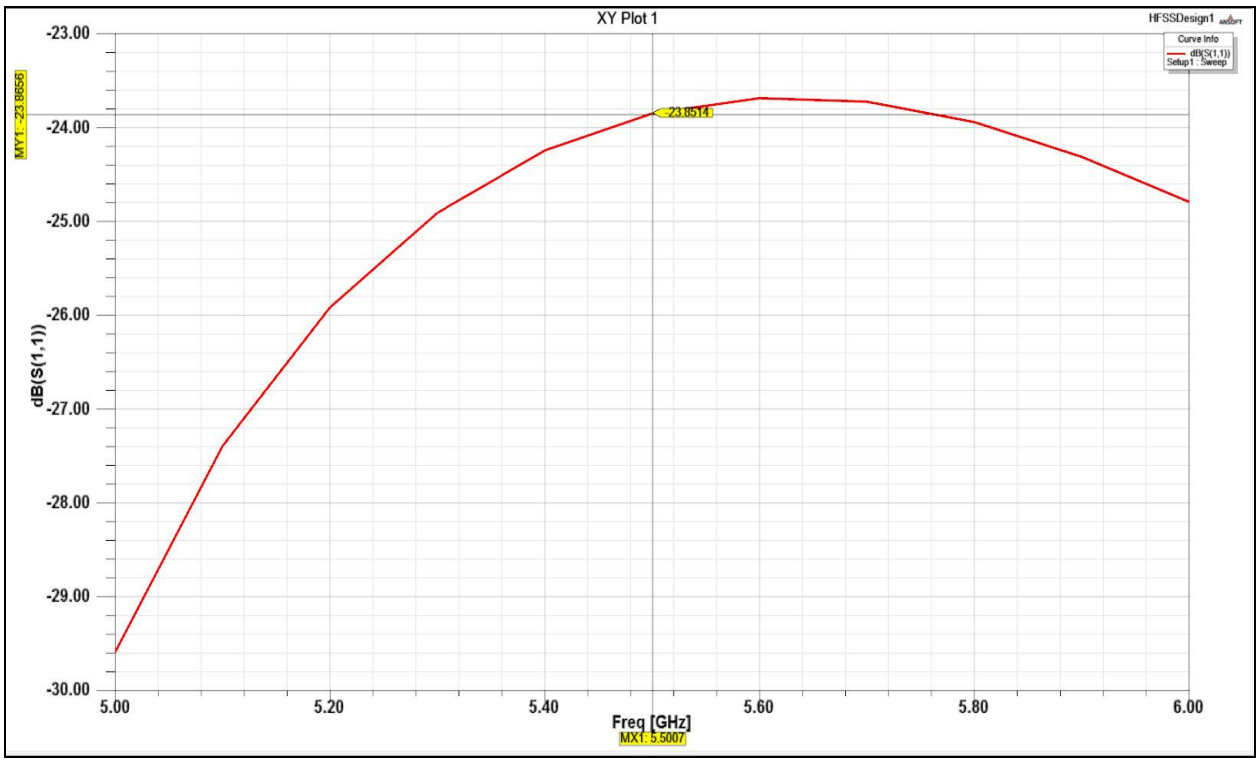

Figure 8

The return loss is improved due to the introduction of the cut at the junction of the transmission lines

3.10. Field Plot:

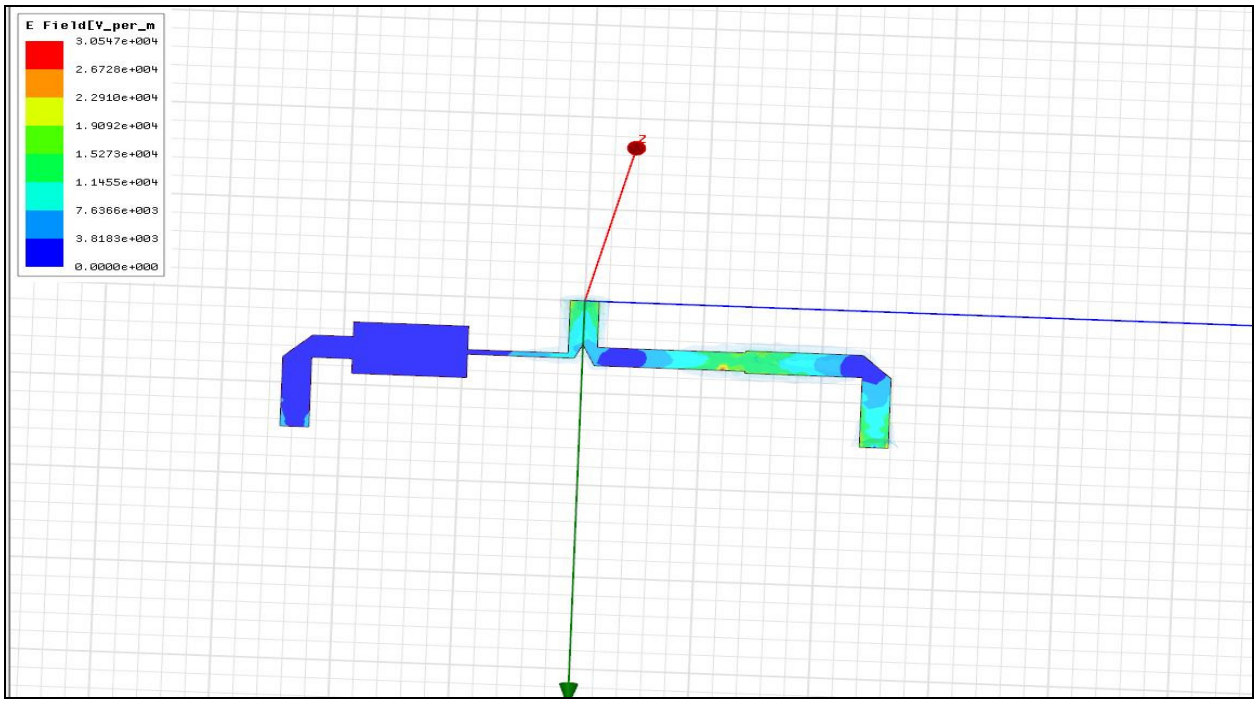

Figure 9

Disadvantages:

- Optimization of the circuit becomes challenging due to the disparity in the fielddistribution shown above.
- Consequently, power division and impedance matching are also affected.
- The values of the output powers at the port and the phase remain consistent with the 2-D simulation results.

In order to overcome the above difficulties, the following T- junction design is preferred.

3.11. Design 3:

This circuit has been designed such that every parameter namely- return loss, phase and power division can be tuned using their respective assigned transmission lines. Hence all the parameters remain independent of each other during tuning of the circuit. This helps in obtaining the accurate port losses and a matched phase between the two output ports easily. Input transformer is used for the adjustment of return loss and QW transformers at the output port are used for power division and impedance matching. Refer to the schematic diagram for location of the TLs.

Calculations:

For input port,

$Z0in = (Z'in*Zin)^{0.5}$

$Z0in = 35.35\Omega$ - TL 1 (for return loss)

For output port 2,

$Z01 = (Z'in*Zout1)^{0.5}$

$Z01 = 137.5\Omega$ - TL 3 (for phase)

For output port 3,

$Z02 = (Z'in*Zout2)^{0.5}$

$Z02 = 36.5\Omega$ - TL 4 (for power division)

TRANSMISSION LINE NO.	IMPEDANCE VALUE(OHM)	WIDTH (IN MM)
TL 1	35.35	3.954
TL 2	50	2.422
TL 3	137.5	0.2528
TL 4	36.5	4.04

Table 3

3.12. Schematic Diagram:

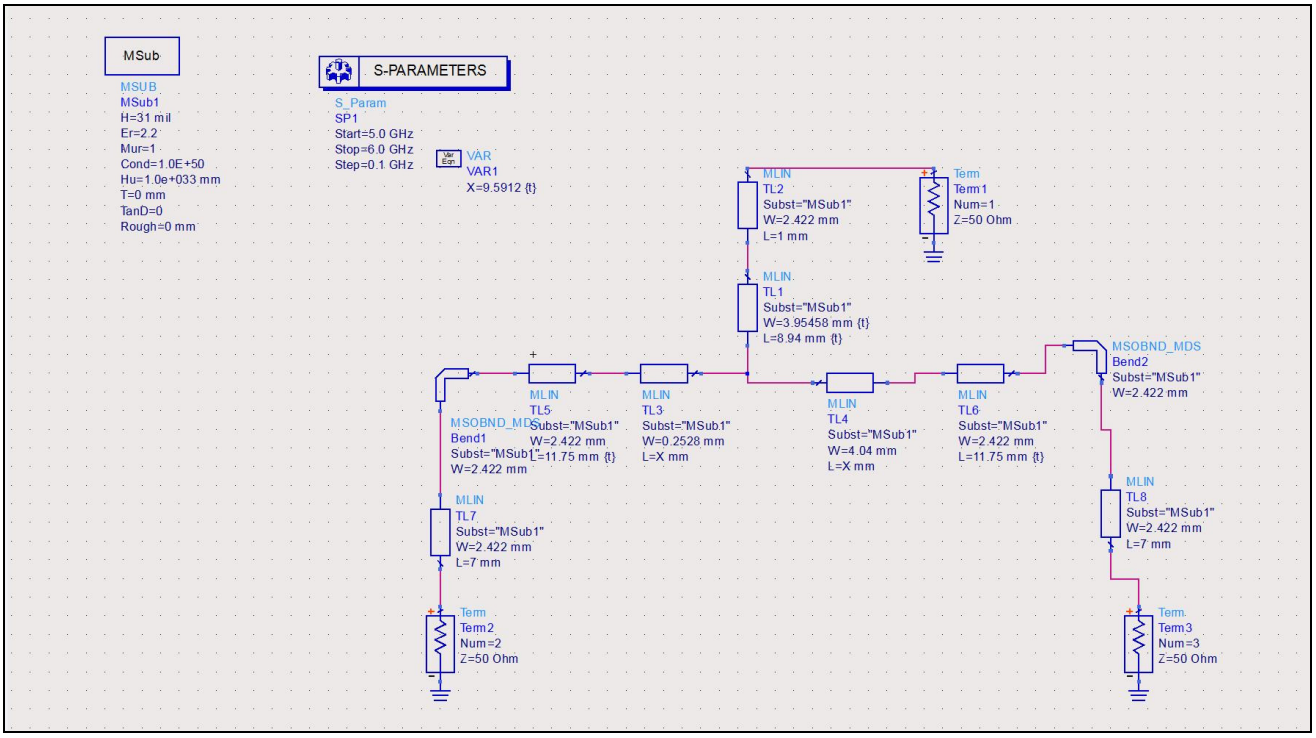

Figure 10

3.13. S -Parameter Results:

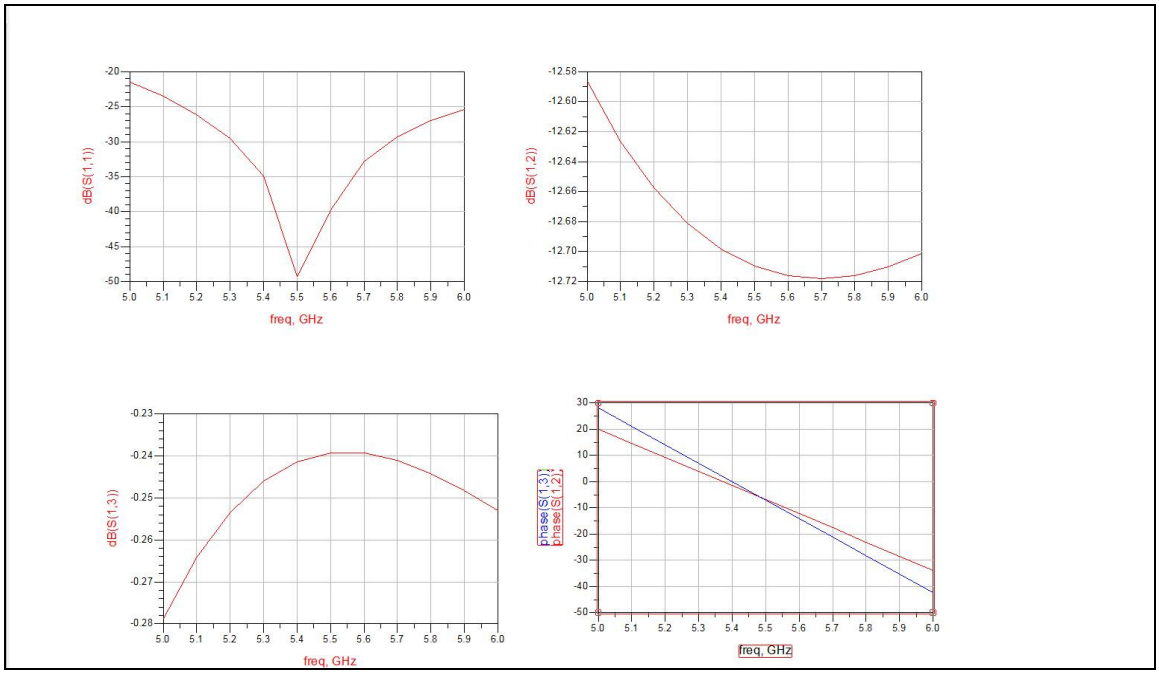

Figure 11

The return loss and the port losses are within the defined limits. Also, the phase remains matched.

3.14. 3-D Simulation Using HFSS – Results:
S(1,1):

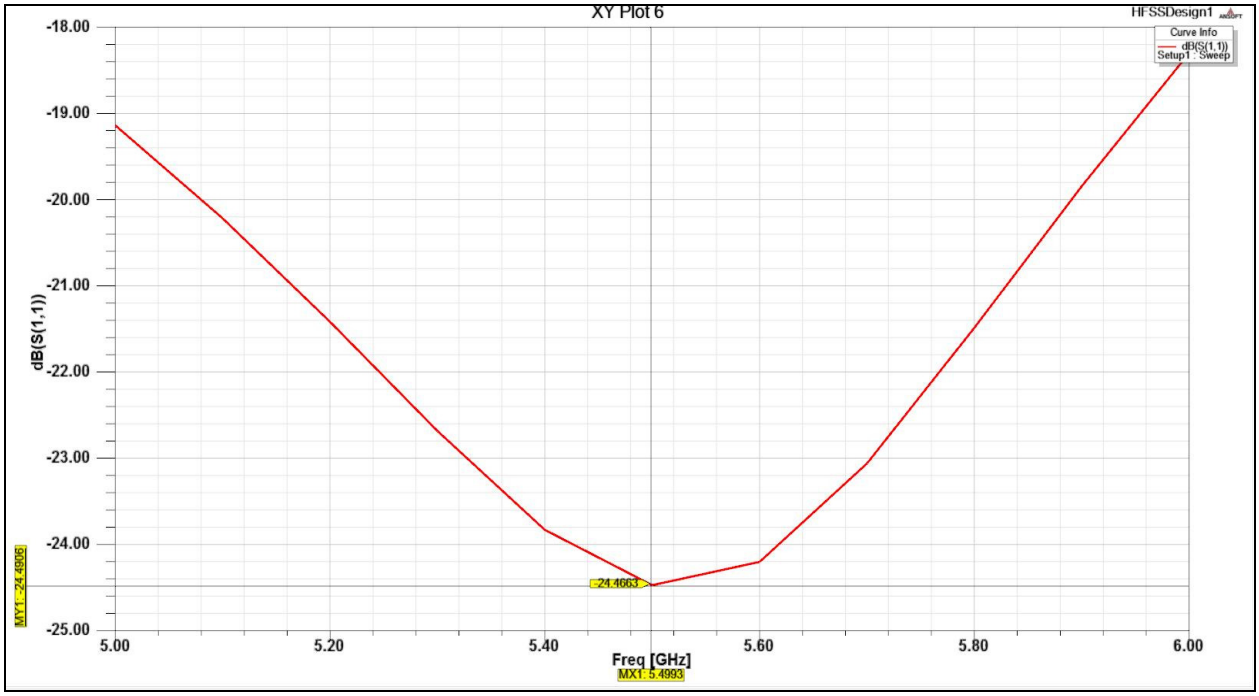

Figure 12

The return loss is better than that observed in the previous model.

3.13. Field Plot:

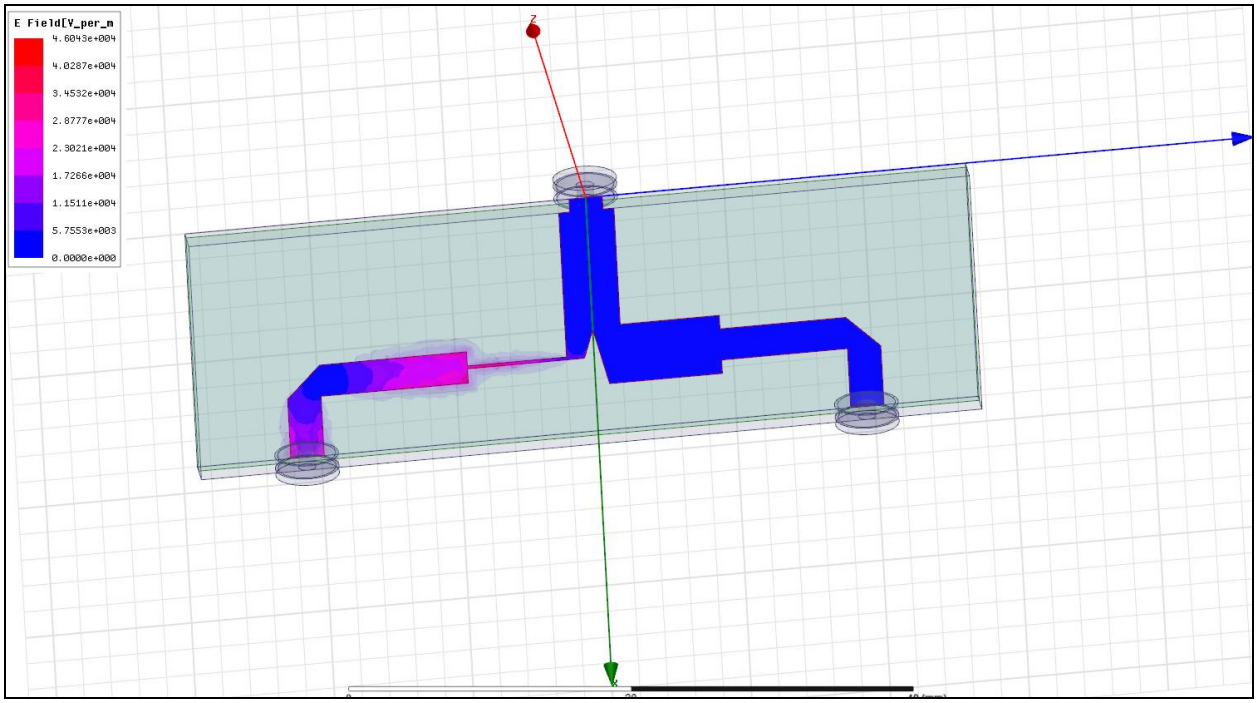

Figure 13

It can be observed from the field plot that power loss has reduced in comparison to the field lines of the previous model.
Hence this is the eventual design processed for fabrication with optimum transmission line width, minimum return loss and matched output ports.

4. Conclusion

An unequal power divider of the output power ratios 1/15 and 14/15 using T-junction was initially simulated in ADS. The results were analysed in the form of s-parameter (for determining port loss) using circuit simulation of ADS. Since the width of transmission line was practically unfeasible, a modified T- junction model was designed using impedance matching transformers for removal of the above difficulty. Further the layout is imported in full wave simulation software HFSS to validate the ADS results. The S- parameters and E- fields plot are generated which shows complete insight of 2 way unequal power divider. The return loss <-20dB at the input port is achieved in full wave simulation meeting the required specifications.

5. References

i. Microwave Engineering by David M. Pozar - 4th edition Wiley 2012.
ii. Balanis C A, Antenna Theory: Analysis and Design, 3rd edition, John Wiley, New York, 2011.
iii. Keith R. Carver, James W. Mink, Microstrip antenna technology, IEEE transactions on antennas and propagation.