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Comparative Analysis of Ultra Low Power and Ultra Low Voltage CMOS Miller OTA's

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Abstract:
Recently so many portable devices like mobile, laptop, palmtop, digital camera are invented which are battery operated. Due to downscaling of technology and long lasting batteries. The CMOS circuits should be provided with low supply voltage and should also consume low power. The OTA can be designed at a very low supply voltage less than 1 Volts and its power dissipation is also low. Recently, so many improved CMOS Miller OTA architectures are reported. Here, a comparison of a simple Miller OTA and the improved CMOS Miller OTA analog circuits in 45 nm, 90 nm and 180 nm technology is done by using Ngspice Simulator.

Keywords: *CMOS, Miller OTA, Unity Gain Bandwidth, Phase Margin, Open Loop Gain, Power Dissipation*

1. Introduction

The operational transconductance amplifier (OTA) is a voltage controlled current source (VCCS) device. The transconductance of the amplifier is usually controlled by an input current denoted as I_{abc} ("Amplifier Bias Current"). The amplifier's transconductance is directly proportional to this current. The OTA's are used in implementing electronically controlled applications such as variable frequency oscillators, filters and variable gain amplifier stages which are more difficult to implement with standard op-amps, multiplexers, timers, sample and hold circuits.

2. Miller OTA

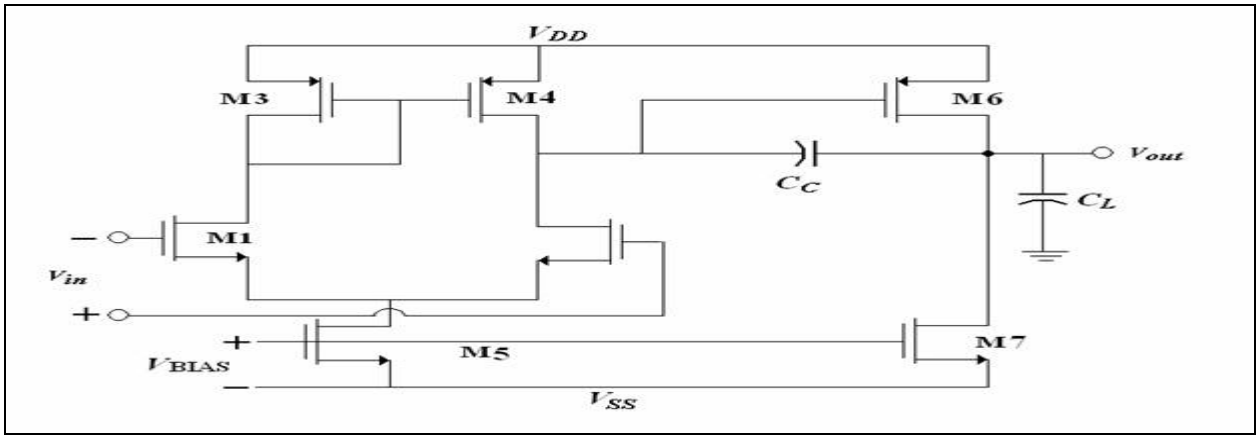

Figure 1: Miller OTA

It consists of differential pair (M1, M2) with transistor loads (M3, M4). It also consists of current mirror sub-circuit (M9, M8, M5, M7) and the output stage (M6, M7). It gains is 74 db in 180 nm technology. Table 1 shows the values when the supply voltage is 2 Volts or 1 Volts for 180 nm technology, but when supply voltage is 0.6 Volts in180 nm technology then only W/L ratio of M5, M7 and M9 will be changed from 1.2u/1u to 3u/1u and all the other W/L ratios will be the same.

$(W/L)_{M1}$ = 5.43u/1u
$(W/L)_{M2}$ = 5.43u/1u
$(W/L)_{M3}$ = 20u/1u
$(W/L)_{M4}$ = 20u/1u
$(W/L)_{M5}$ = 1.2u/1u
$(W/L)_{M6}$ = 60.6u/1u
$(W/L)_{M7}$ = 1.2u/1u
$(W/L)_{M8}$ = 80u/1u
C_c = 0.01 nF

Table 1: Transistor and Other Elements of Miller OTA in 180 nm Technology (2V & 1V Supply Voltage) & 90 nm Technology (1V & 0.6V Supply Voltage)

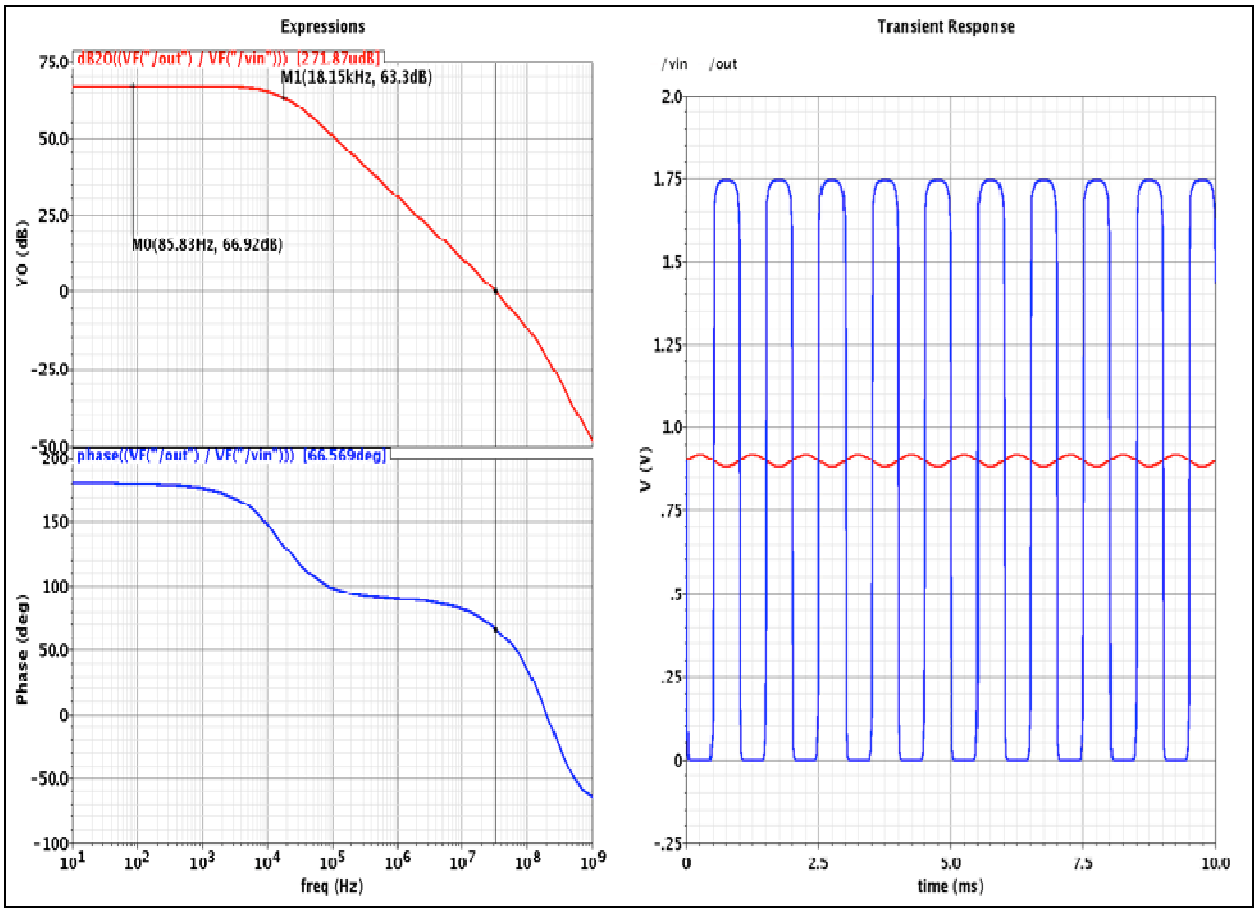

Figure 2: Simulated Open Loop Gain and Phase of Miller OTA

Type of Technology	**180 nm**	**180 nm**	**180 nm**	**90 nm**	**90 nm**	**90 nm**
Power Supply	2 Volts	1 Volts	0.6 Volts	2 Volts	1 Volts	0.6 Volts
Open Loop Gain	74.1 db	73.1 db	70 db	50 db	56.5 db	56.5 db
Unity Gain Frequency	5.1 MHz	813 KHz	577 KHz	511 MHz	316 MHz	304 MHz
Phase Margin	71 Degrees	67 Degrees	65 Degrees	65 Degrees	60 Degrees	67 Degrees
Power Dissipation	533 µW	15 µW	98 nW	22 nW	0.72 mW	26 µW
Slew Rate	5.3 V/µsec	1.68 V/µsec	50 V/µsec	635 V/µsec	152 V/µsec	10 V/µsec

Table 2: Miller OTA Performance Benchmark Indicators

3. Improved Miller OTA

The Bulk Driven Floating Gate Threshold voltage tuning is the best approach for a low voltage CMOS circuit, since it allows a large signal swing without cutting off the transistor. The leakage current is also low in bulk-driven differential pair type of architecture.

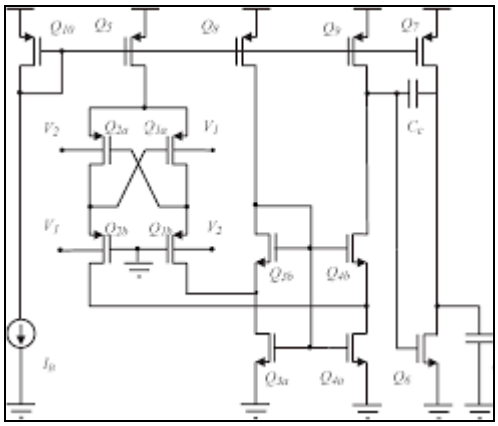

Figure 3: Improved Bulk Driven Miller OTA Circuit

In this architecture, the transistor pair 3a-3b and 4a-4b form the composite transistors. They allow the differential pair active load and the common gate amplifier to be biased by the same potential without the use of additional biasing sources [3].

$(W/L)_{M1}$ = 126.5u/1u
$(W/L)_{M2}$ = 126.5u/1u
$(W/L)_{M3}$=20u/1u
$(W/L)_{M4a}$ = 20u/1u
$(W/L)_{M4b}$ = 90u/1u
$(W/L)_{M3a}$ = 20u/1u
$(W/L)_{M3b}$ = 90u/1u
$(W/L)_{M5}$ = 94.5u/9u
$(W/L)_{M6}$ = 55.56u/1u
$(W/L)_{M7}$ = 180u/9u
$(W/L)_{M8}$ = 17.5u/9u
$(W/L)_{M9}$ = 17.5u/9u
R_C=5K

Table 3: Transistors and Other Elements of Improved Miller OTA in 180 nm & 90 nm Technology

$(W/L)_{M1}$ = 143.44u/1u
$(W/L)_{M2}$ = 143.44u/1u
$(W/L)_{M3a}$ = 77.18u/1u
$(W/L)_{M4a}$ = 77.18u/1u
$(W/L)_{M3b}$ = 174.34u/1u
$(W/L)_{M4b}$ = 174.34u/1u
$(W/L)_{M5}$ = 177.45u/9u
$(W/L)_{M6}$ = 4.65u/1u
$(W/L)_{M7}$ = 10.91u/9u
$(W/L)_{M8}$ = 92.33u/9u
$(W/L)_{M9}$ = 92.33u/9u
$(W/L)_{M10}$ = 140.92u/9u
C_c = 4F
I_{ref} = 27u
R_C = 34 K
C_L = 1F

Table 4: Transistor and Other Elements of Improved Miller OTA in 45 nm Technology

Type of Technology	[3]	180 nm	90 nm	45 nm
Power Supply	0.6 Volts	0.6 Volts	0.6 Volts	0.6 Volts
Open Loop Gain	69.4 db	71.0 db	77.9 db	73.4 db
Unity Gain Frequency	11.35KHz	683 KHz	26 MHz	142 MHz
Phase Margin	65.1 Degrees	72.7 Degrees	71.2 Degrees	65.4 Degrees
Power Dissipation	550 nW	11 µW	77 µW	50 µW
Slew Rate	14.6 V/msec	200 V/msec	500 V/ msec	280 V/msec

Table 5: Improved Miller OTA Performance Benchmark Indicators

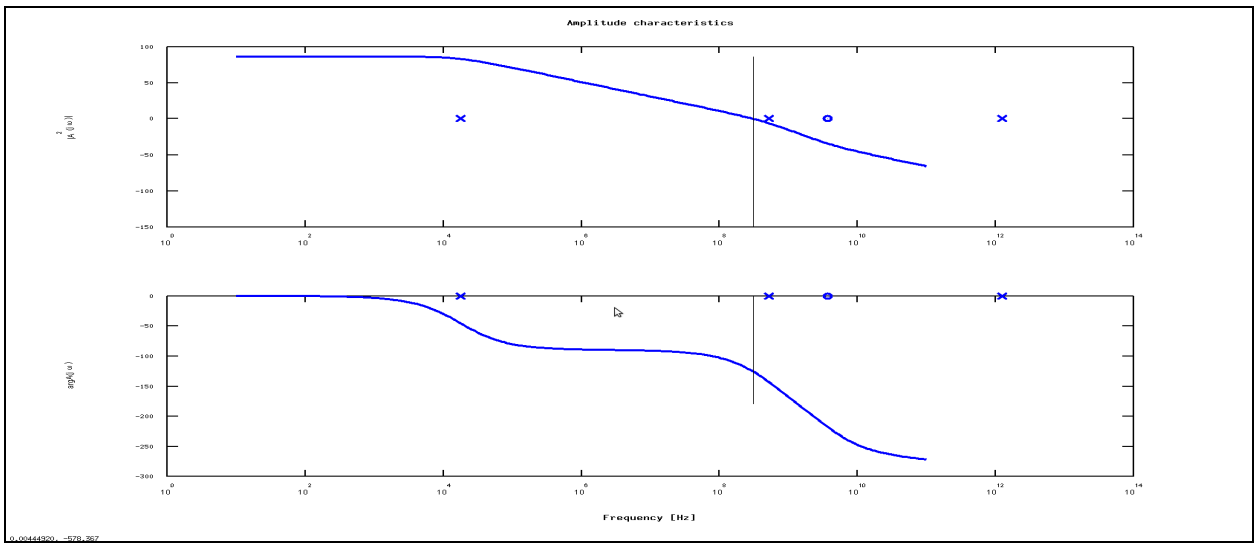

Figure 4: Gain-Phase Plot of Improved Miller OTA at 45 nm

4. Most Recent Improved Miller OTA

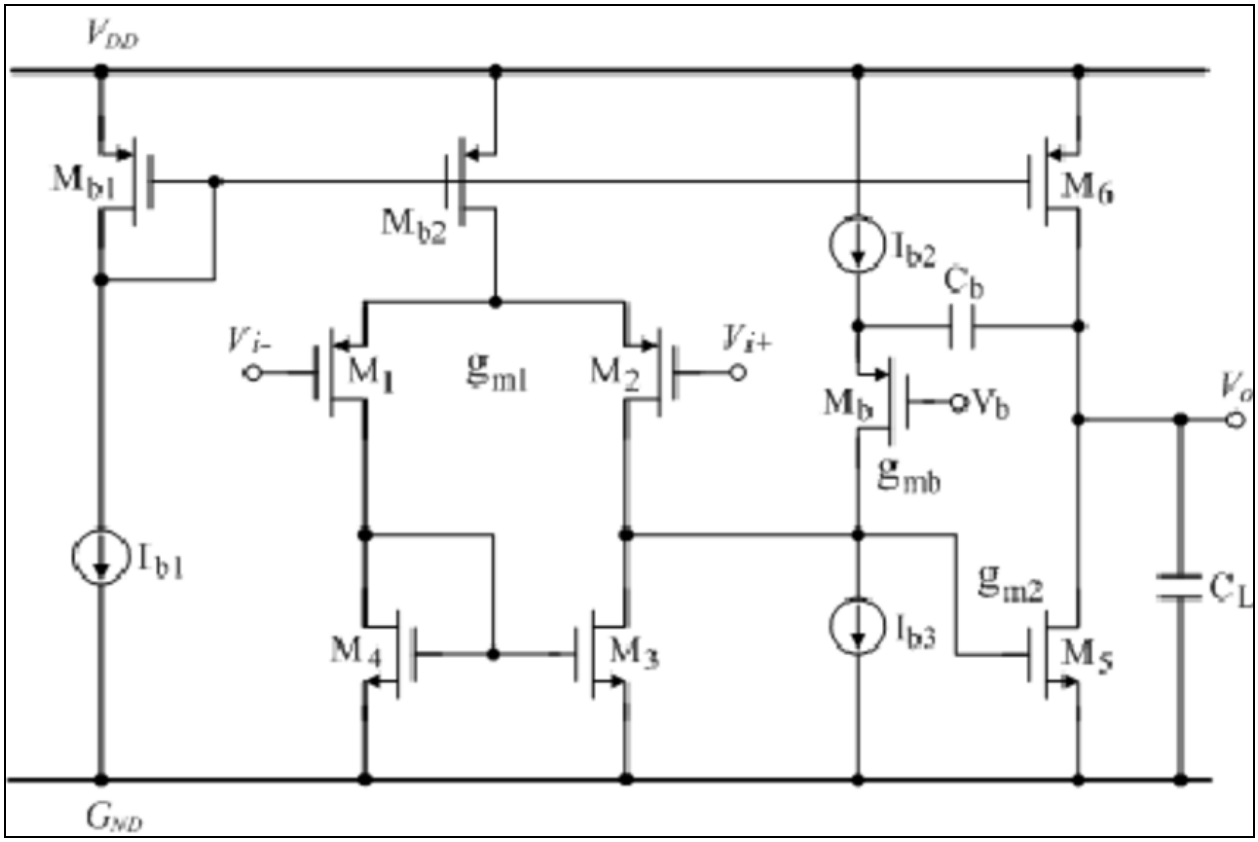

Figure 5: Most Recent Improved Miller OTA

The proposed topology based on a bulk-driven input differential pair employed is a gain stage in the Miller capacitor feedback path in order to improve the "pole-splitting" effect [4].

Type of Technology	[4]	180 nm	90 nm
Power Supply	0.5 Volts	0.5 Volts	0. 5 Volts
Open Loop Gain	88.5 db	75 db	71 db
Unity Gain Frequency	83.88 KHz	607 KHz	296 KHz
Phase Margin	66.3 Degrees	72.2 Degrees	74.5 Degrees
Power Dissipation	1.02 µW	0.77 µW	2.9 µW
Slew Rate	52 V/msec	100 V/ msec	20 V/msec

Table 6: Miller OTA Performance Benchmark Indicators

5. References

i. Design of CMOS OTA Core for Practical Education
ii. Fabian Khateb, Dalibor Biolek, Nabhan Khatib, "Utilizing the Bulk-Driven Technique in Analog Circuit Design", ISSN-ISBN No: 978-1-4244-6613-9/10, 2010, IEEE.
iii. Luis H. C. Ferreria, T. C. Pimenta and R. L. Moreno, "An Ultra Low Voltage Ultra Low Power CMOS Miller OTA with Rail to Rail Input/Output Swing", IEEE Transactions, Volume 549-7747, October 2007.
iv. Milad Razzaghpuor, Abbas Golmakani, "An Ultra Low Voltage Ultra Low Power OTA with Improved Gain-Bandwidth Product",ISSN/ISBNNo: 1-4244-2370-5, 2008, IEEE.