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Novel Design of Cascaded Multilevel Inverter with Reduced THD for Solar Applications

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Abstract:
The consumption of fossil fuels is at higher rate, but fossil fuels are non-renewable energy sources will not be available forever, they will not satisfy our demands for longer period and also they are not eco friendly. Hence renewable energy sources are gaining more importance in generating power, particularly solar energy because, this solar energy is available in abundance from sun and also pollution free. Photovoltaic Cells (PV) are used to generate electricity from sun light, the power generated in DC form from PV cell is fed to DC-DC converter. The DC-DC converter will increase the voltage to a particular level, the output of DC-DC converter is given to input of inverter, which will supply power to AC applications. Hence inverter plays a very important role in supplying good quality of power for AC applications. Multilevel Inverters (MLI) are used to produce fine quality of AC power since, in MLI as number of output levels increases Total Harmonic Distortion (THD) decreases. The proposed cascaded asymmetrical MLI circuit consists of 15 switches, used for power conversion with 100 output levels. The THD of proposed MLI circuit is just 3.79%, and this is an asymmetrical type of MLI. Simulation of proposed circuit is performed using MATLAB/SIMULINK.

Keywords: *Multilevel Inverter (MLI), Total Harmonic Distortion (THD), Photo Voltaic (PV), DC-DC Converter, DC to AC*

1. Introduction

As the population goes on increasing, the demand of electricity also goes on increasing. To fulfill this demand of electricity huge power has to be generated by the generating stations. Due to the usage of fossil fuels to generate the power, the environment is getting highly polluted because of the emission of carbon dioxide gases. It also leads to global warming, acid rain which causes huge losses to humans and even damage plants. Hence for survival of mankind and nature, there is a need to generate power from renewable energy sources, which is eco-friendly and pollution free.

In this renewable energy sources, solar energy can be used to generate power by utilizing PV cells, which converts sunlight directly in to electricity. PV cells generate DC voltage. By using an inverter this DC is converted in to AC and used for AC applications. For this conversion purpose initially conventional inverters were used, but this conventional type of inverters had many limitations like high THD in output voltage, EMI problems, switching stress was high, and not suitable for applications which require huge power.

As a result of research on inverters, MLI were invented. This MLI will produce AC output in many levels, which helps in reducing THD. When there is an increase in output levels the THD decreases. Most widely used MLI is H-bridge type of inverter. MLI can be used with lower switching frequencies due to which switching losses are also reduced and also it can be used for high power applications. In this paper novel cascaded multilevel inverter with reduced THD for solar applications is proposed, which can be used to produce good quality of power supply for AC applications.

2. Fundamental Cell of Proposed MLI

Fig 1 shows the fundamental cell of a proposed MLI. Circuit has two input DC sources V_{11} and V_{12}, it consists of four switches S_{11}, S_{12}, S_{13}, S_{14} in H- bridge type of arrangement. Switch S_{15} is a selection switch, which is used to increase output voltage by selecting suitable input DC sources. And also circuit contains four anti parallel diodes near switch S_{15}. Fundamental cell of proposed MLI converts DC input in to five levels AC output by using 5 switches.

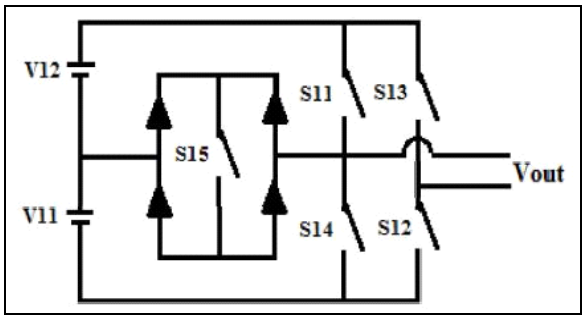

Figure 1: Fundamental cell of proposed MLI

S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	Output yield
0	0	0	0	0	0
0	1	0	0	1	V_{dc}
1	1	0	0	0	$2V_{dc}$
0	1	0	0	1	V_{dc}
0	0	0	0	0	0
0	0	1	0	1	$-V_{dc}$
0	0	1	1	0	$-2V_{dc}$
0	0	1	0	1	$-V_{dc}$

Table 1: Switching sequence of five switches

Table 1 shows the switching sequence of switches S_{11}, S_{12}, S_{13}, S_{14} and S_{15}. It consists of 5 levels of switching sequences for positive cycle of AC output, and 5 levels of switching sequences for negative cycle of AC output. There are two zero voltage level switching sequences which is common to both positive and negative cycles of AC output. In table 1 rationale '1' denotes 'ON' condition and rationale '0' denotes 'OFF' condition of switches.

3. Proposed Cascaded Multilevel Inverter

Fig 2 shows the proposed cascaded cell of MLI, this proposed circuit consists of three cascaded fundamental cells.

It has total six input DC sources, and 15 switches S_{11}, S_{12}, S_{13}, S_{14}, S_{15}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{31}, S_{32}, S_{33}, S_{34}, S_{35} are used. While Switch S_{15}, S_{25}, S_{35} is a selection switch of first, second, third fundamental cells respectively, which is used to increase output voltage by selecting suitable input DC sources, this circuit produces 100 output levels.

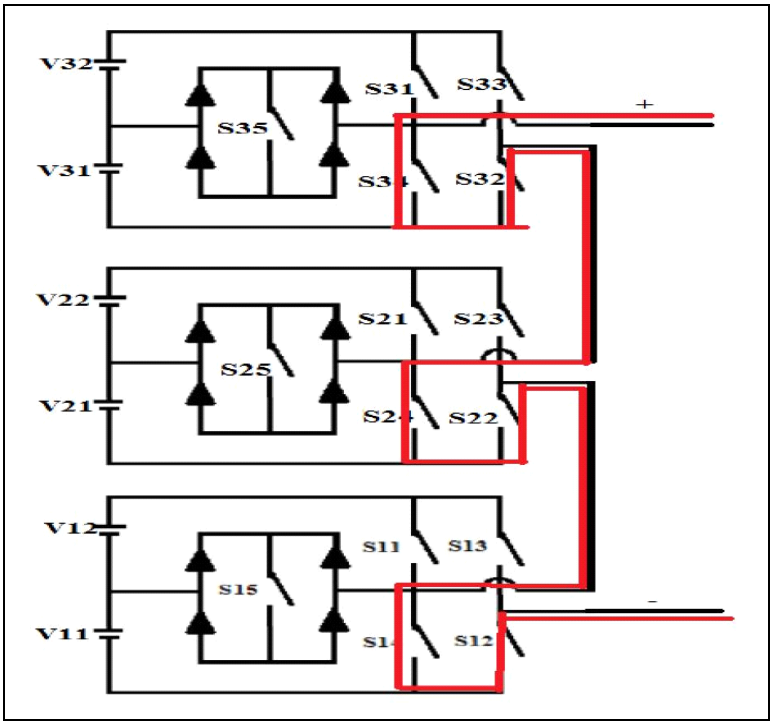

Figure 2: Proposed cascaded multilevel inverter

Proposed circuit consist of three sets of anti parallel diodes. Four diodes in each cell, total 12 diodes are used. Diodes gives the path for current to flow. This circuit is called as asymmetrical type of multilevel inverter because, voltage sources of three basic cell is not equal.

From above proposed cascaded multilevel inverter,

$V11 = V12 = V_{dc}$

$V21 = V22 = \frac{Vdc}{5}$

$V31 = V32 = \frac{Vdc}{20}$

4. Operation of Proposed MLI

The proposed MLI produces 100 levels AC output. The switching sequences of all the 15 switches to produce 100 levels output is shown in table 2, there are two zero voltage switching sequence common to both positive and negative cycle AC output. Switching sequences for 100 level output is found by tracing the current path through circuit.

Input DC voltages are,

$V_{11} = V_{12} = 120V$, $V_{21} = V_{22} = 24V$, $V_{31} = V_{32} = 6V$

The total output voltage of proposed cascaded MLI is the sum of voltages of three individual fundamental cells. Given by,

$V_{output} = V_{01} + V_{02} + V_{03}$

Levels	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{21}	S_{22}	S_{23}	$S2_4$	S_{25}	S_{31}	S_{32}	S_{33}	S_{34}	S_{35}	Output voltage
1	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0
	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	0
2	0	1	0	1	0	0	1	0	1	0	0	1	0	0	1	6
3	0	1	0	1	0	0	1	0	1	0	1	1	0	0	0	12
4	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	18
5	0	1	0	1	0	0	1	0	0	1	0	1	0	1	0	24
6	0	1	0	1	0	0	1	0	0	1	1	1	0	1	0	30
7	0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	36
8	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	42
9	0	1	0	1	0	1	1	0	0	0	0	1	0	1	0	48
10	0	1	0	1	0	1	1	0	0	0	0	1	0	0	1	54
11	0	1	0	1	1	1	1	0	0	0	1	1	0	0	0	60
12	0	1	0	0	1	0	0	1	1	0	0	0	1	0	1	66
13	0	1	0	0	1	0	0	1	1	0	0	1	0	1	0	72
14	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	78
15	0	1	0	0	1	0	0	1	1	0	1	1	0	0	0	84
16	0	1	0	0	1	0	0	1	0	1	0	0	1	0	1	90
17	0	1	0	0	1	0	0	1	0	1	0	1	0	1	0	96
18	0	1	0	0	1	0	0	1	0	1	0	1	0	0	1	102
19	0	1	0	0	1	0	0	1	0	1	1	1	0	0	0	108
20	0	1	0	0	1	0	1	0	1	0	0	0	1	0	1	114
21	0	1	0	0	1	0	1	0	1	0	0	1	0	1	0	120
22	0	1	0	0	1	0	1	0	1	0	0	1	0	0	1	126
23	0	1	0	0	1	0	1	0	0	1	0	0	0	1	1	132
24	0	1	0	0	1	0	1	0	0	1	0	0	1	0	1	138
25	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	144
26	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	150
27	0	1	0	0	1	1	1	0	0	0	0	0	1	1	0	156
28	0	1	0	0	1	1	1	0	0	0	0	0	1	0	1	162
29	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	168
30	0	1	0	0	1	1	1	0	0	0	0	1	0	0	1	174
31	0	1	0	0	1	1	1	0	0	0	1	1	0	0	0	180
32	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	186
33	1	1	0	0	0	0	0	1	1	0	0	1	0	1	0	192
34	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	198
35	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	204
36	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	210
37	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	216
38	1	1	0	0	0	0	0	1	0	1	0	1	0	0	1	222
39	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	228
40	1	1	0	0	0	0	1	0	1	0	0	0	1	0	1	234
41	1	1	0	0	0	0	1	0	1	0	0	1	0	1	0	240
42	1	1	0	0	0	0	1	0	1	0	0	1	0	0	1	246
43	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	252
44	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	258
45	1	1	0	0	0	0	1	0	0	1	0	1	0	1	0	264
46	1	1	0	0	0	0	1	0	0	1	0	1	0	0	1	270
47	1	1	0	0	0	0	1	0	0	1	1	1	0	0	0	276
48	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	282
49	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	288

50	1	1	0	0	0	1	1	0	0	0	0	1	0	0	1	294
51	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	300
52	1	1	0	0	0	1	1	0	0	0	0	1	0	0	1	294
53	1	1	0	0	0	1	1	0	0	0	0	1	0	1	0	288
54	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	282
55	1	1	0	0	0	0	1	0	0	1	1	1	0	0	0	276
56	1	1	0	0	0	0	1	0	0	1	0	1	0	0	1	270
57	1	1	0	0	0	0	1	0	0	1	0	1	0	1	0	264
58	1	1	0	0	0	0	1	0	0	1	0	0	1	0	1	258
59	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	252
60	1	1	0	0	0	0	1	0	1	0	0	1	0	0	1	246
61	1	1	0	0	0	0	1	0	1	0	0	1	0	1	0	240
62	1	1	0	0	0	0	1	0	1	0	0	0	1	0	1	234
63	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	228
64	1	1	0	0	0	0	0	1	0	1	0	1	0	0	1	222
65	1	1	0	0	0	0	0	1	0	1	0	1	0	1	0	216
66	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	210
67	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	204
68	1	1	0	0	0	0	0	1	1	0	0	1	0	0	1	198
69	1	1	0	0	0	0	0	1	1	0	0	1	0	1	0	192
70	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	186
71	0	1	0	0	1	1	1	0	0	0	1	1	0	0	0	180
72	0	1	0	0	1	1	1	0	0	0	0	1	0	0	1	174
73	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	168
74	0	1	0	0	1	1	1	0	0	0	0	0	1	0	1	162
75	0	1	0	0	1	1	1	0	0	0	0	0	1	1	0	156
76	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	150
77	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	144
78	0	1	0	0	1	0	1	0	0	1	0	0	1	0	1	138
79	0	1	0	0	1	0	1	0	0	1	0	0	0	1	1	132
80	0	1	0	0	1	0	1	0	1	0	0	1	0	0	1	126
81	0	1	0	0	1	0	1	0	1	0	0	1	0	1	0	120
82	0	1	0	0	1	0	1	0	1	0	0	0	1	0	1	114
83	0	1	0	0	1	0	0	1	0	1	1	1	0	0	0	108
84	0	1	0	0	1	0	0	1	0	1	0	1	0	0	1	102
85	0	1	0	0	1	0	0	1	0	1	0	1	0	1	0	96
86	0	1	0	0	1	0	0	1	0	1	0	0	1	0	1	90
87	0	1	0	0	1	0	0	1	1	0	1	1	0	0	0	84
88	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	78
89	0	1	0	0	1	0	0	1	1	0	0	1	0	1	0	72
90	0	1	0	0	1	0	0	1	1	0	0	0	1	0	1	66
91	0	1	0	1	0	1	1	0	0	0	1	1	0	0	0	60
92	0	1	0	1	0	1	1	0	0	0	0	1	0	0	1	54
93	0	1	0	1	0	1	1	0	0	0	0	1	0	1	0	48
94	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	42
95	0	1	0	1	0	0	1	0	0	1	1	1	0	0	0	36
96	0	1	0	1	0	0	1	0	0	1	1	1	0	1	0	30
97	0	1	0	1	0	0	1	0	0	1	0	1	0	1	0	24
98	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	18
99	0	1	0	1	0	0	1	0	1	0	1	1	0	0	0	12
100	0	1	0	1	0	0	1	0	1	0	0	1	0	0	1	6

Table 2: Switching Sequences of 15 Switches of Proposed Multilevel Inverter

5. Matlab/ Simulink Results

The simulation of proposed MLI is performed using MATLAB/SIMULINK. FFT window is used to find the THD. The simulation circuit parameters are $V_{11} = V_{12} = 120V$, $V_{21} = V_{22} = 24V$, $V_{31} = V_{32} = 6V$. Frequency=50Hz, R=280 Ω, L=10000mH. Switching frequency = 10KHZ.

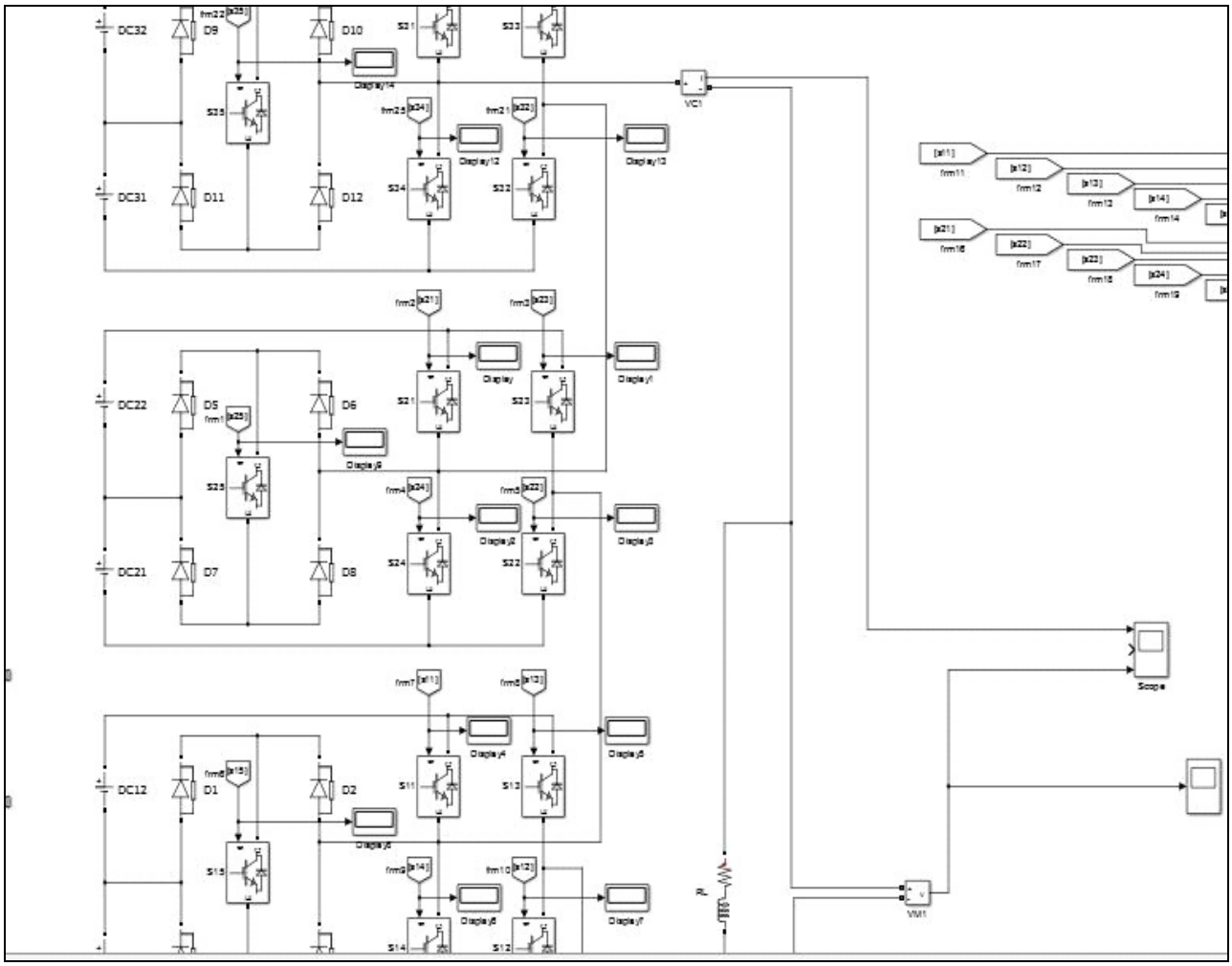

Figure 3: SIMULINK model of proposed topology

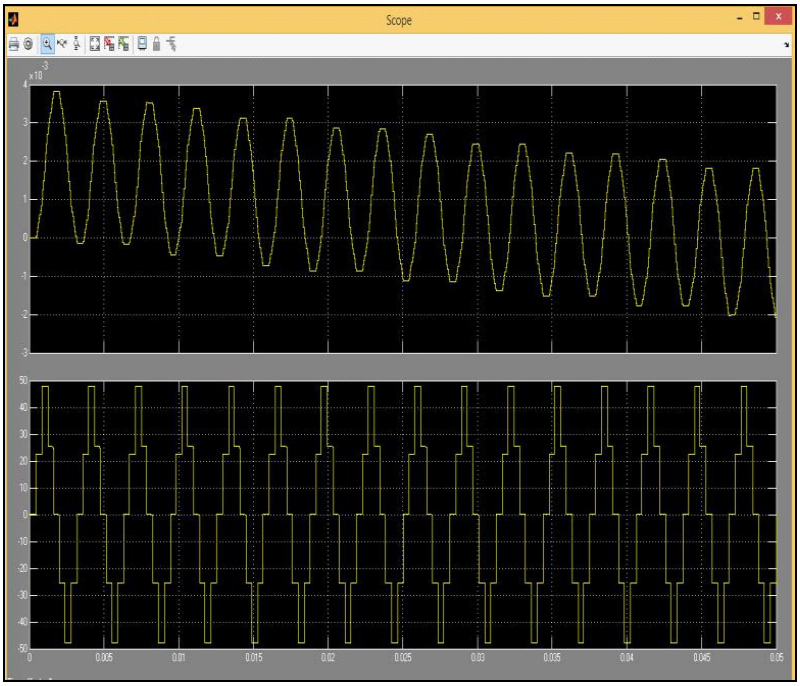

Figure 4: Output voltage of fundamental cell

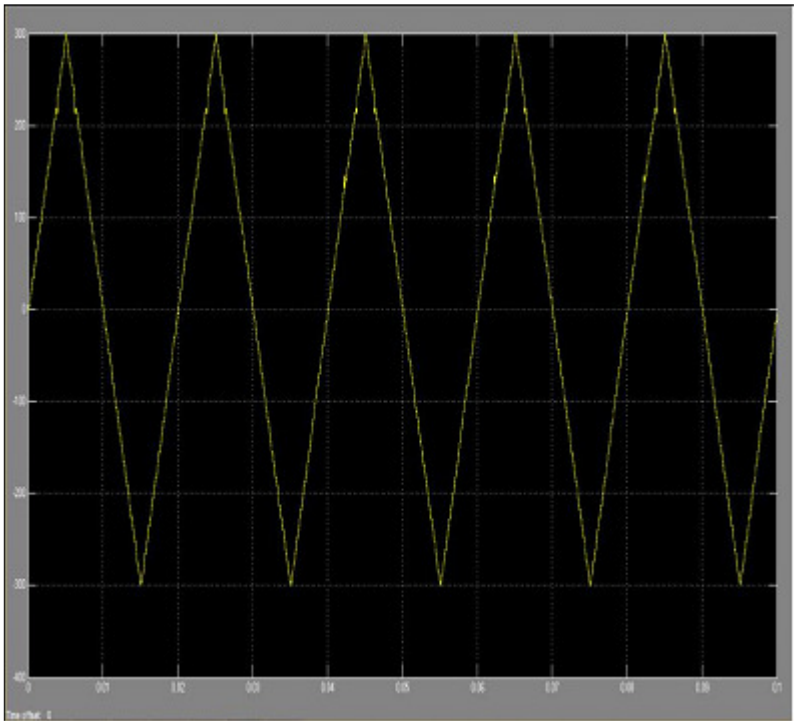

Figure 5: Output voltage of proposed multilevel inverter

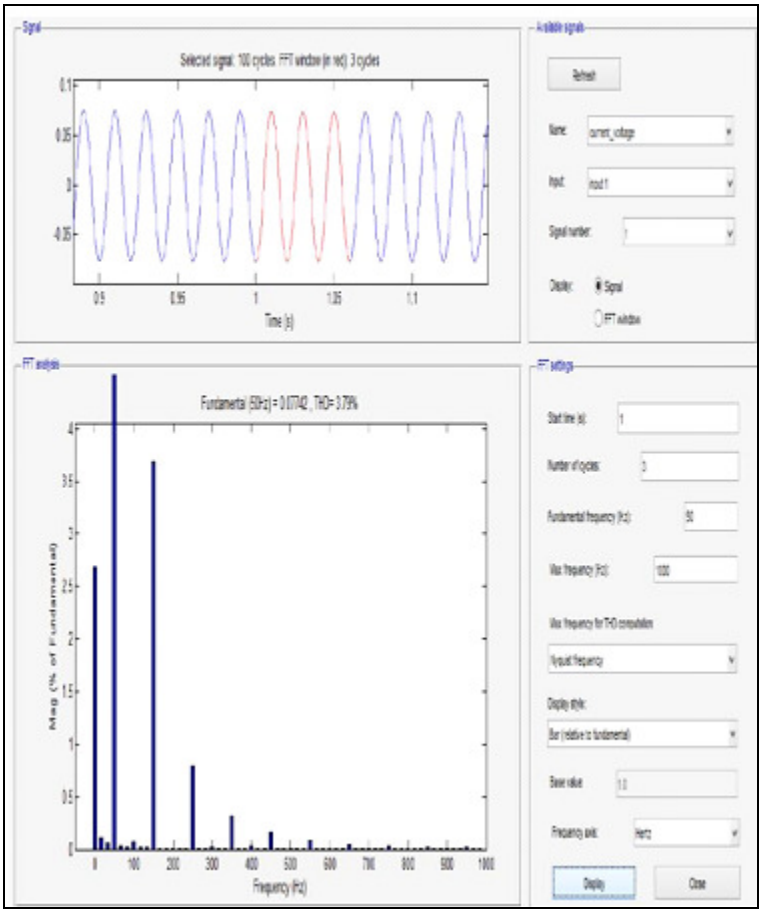

Figure 6: THD of proposed MLI

Fig 3 shows the SIMULINK model of proposed cascaded MLI with 15 switches. Output waveforms using RL load is shown in fig 4 and fig 5. Fig 6 shows the THD of proposed circuit. The THD of proposed circuit is 3.79%.

6. Hardware Topology

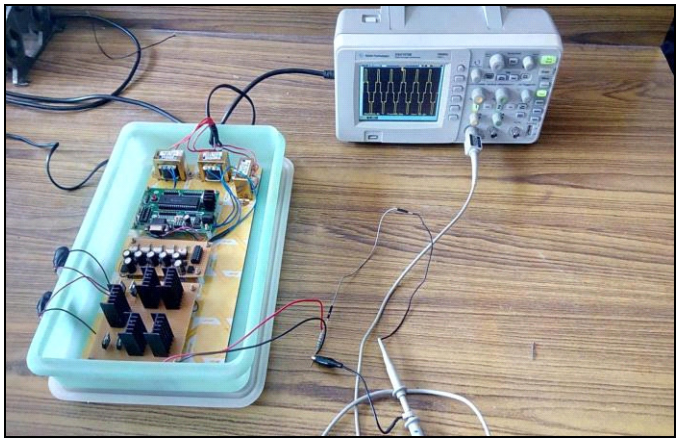

Figure 7: Fundamental Cell Hardware Topology

Fig 7 shows the hardware topology of fundamental cell; it is a five level inverter basic cell. It consists of five IGBTs (Insulated gate bipolar transistor), which are used as switches to convert DC to AC. The IGBTs perform switching operations as per the switching sequences given in table 3. PIC microcontroller kit is used to generate the pulse, Programming is done and uploaded to PIC microcontroller IC, which produces five pulses to drive five IGBTs through TLP 250 driver IC, which helps in fast switching operation. This basic cell has two equivalent input DC sources, 9V battery is connected to both the inputs individually. Finally, this fundamental cell inverter of 5 switches converts 18v DC supply in to 36V (p-p) 5 level AC.

S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	Output yield
0	0	0	0	0	0
0	1	0	0	1	V_{dc}
1	1	0	0	0	2_{Vdc}
0	1	0	0	1	V_{dc}
0	0	0	0	0	0
0	0	1	0	1	-Vdc
0	0	1	1	0	-2Vdc
0	0	1	0	1	-Vdc

Table 3: Switching sequence of 5 switches hardware topology

7. Comparison between Previous Work and Proposed Work

Sl. No	Particulars	Previous Work [1]	Proposed work
1	Number of switches	10	15
2	Number of output levels	25	100
3	THD	4.98%	3.79%
4	Number of basic cells	2	3
5	Hardware topology	Not implemented	Implemented

Table 4

8. Conclusion

In this paper, a novel design of cascade MLI with reduced THD for solar applications is proposed, and successfully implemented using MATLAB/SIMULINK software, and also a hardware topology of fundamental cell of 5 level AC output is successfully demonstrated. The proposed circuit produces 100 levels AC output with very less THD of 3.79%. The output of proposed circuit is near to sinusoidal waveform. Hence this cascaded MLI supplies a good quality of power supply for AC applications and overcomes the limitations of conventional inverter and can be used for applications which require huge power for their working.

9. References

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